150V N-CHANNEL ENHANCEMENT MODE MOSFET
PowerDI5060-8

Product Summary

BV_{DSS}	$R_{DS(ON)}$ Max	I_D Max T_C = +25°C
150V	17.5mΩ @ V_{GS} = 10V	58A
	25.5mΩ @ V_{GS} = 4.5V	48A

Features

- 100% Unclamped Inductive Switching (UIS) Test in Production – Ensures More Reliable and Robust End Application
- Thermally Efficient Package-Cooler Running Applications
- High Conversion Efficiency
- Low $R_{DS(ON)}$ – Minimizes On-State Losses
- Low Input Capacitance
- Fast Switching Speed
- <1.1mm Package Profile – Ideal for Thin Applications (PowerDI®)
- **Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

Description

This new generation N-Channel Enhancement Mode MOSFET is designed to minimize $R_{DS(ON)}$ yet maintain superior switching performance. This device is ideal for use in notebook battery power management and load switch.

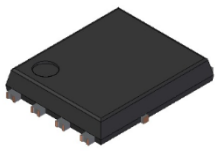
Applications

- Synchronous Rectification
- Power Switching
- Class D Audio Amplifier

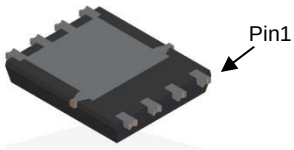
Mechanical Data

- Case: PowerDI5060-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram Below
- Terminal Finish - Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.097 grams (Approximate)

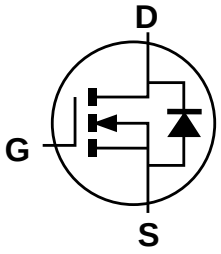
PowerDI5060-8 (SWP) (Type UX)



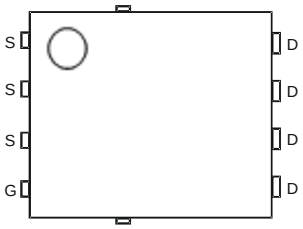
Top View



Bottom View



Internal Schematic



Top View
Pin Configuration

Ordering Information (Note 4)

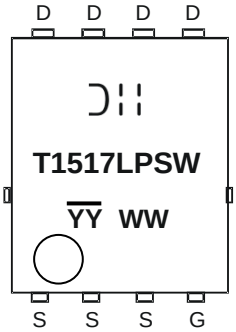
Part Number	Case	Packaging
DMT15H017LPSW-13	PowerDI5060-8 (SWP) (Type UX)	2,500 / Tape & Reel

Notes:
1. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

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Marking Information



= Manufacturer's Marking
T1517LPSW = Product Type Marking Code
YYWW = Date Code Marking
YY = Last Two Digits of Year (ex: 21 = 2021)
WW = Week Code (01 to 53)

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	150	V
Gate-Source Voltage			V_{GSS}	±20	V
Continuous Drain Current V_{GS} = 10V (Note 6)	Steady State	T_A = +25°C	I_D	9.4	A
		T_A = +70°C		7.5	
Continuous Drain Current V_{GS} = 10V (Note 7)	Steady State	T_C = +25°C	I_D	58	A
		T_C = +70°C		46	
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)			I_{DM}	230	A
Maximum Continuous Body Diode Forward Current			I_S	74	A
Pulsed Body Diode Current (10µs Pulse, Duty Cycle = 1%)			I_{SM}	230	A
Avalanche Current (Note 8), L = 3mH			I_{AS}	14.5	A
Avalanche Energy (Note 8), L = 3mH			E_{AS}	315.4	mJ

Thermal Characteristics

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)	T_A = +25°C	P_D	1.3	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{\theta JA}$	99	°C/W
Total Power Dissipation (Note 6)	T_A = +25°C	P_D	2.3	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	53	°C/W
Total Power Dissipation (Note 7)	T_C = +25°C	P_D	89	W
Thermal Resistance, Junction to Case (Note 7)		$R_{\theta JC}$	1.4	°C/W
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Notes: 5. Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate.
7. Thermal resistance from junction to soldering point (on the exposed drain pad).
8. I_{AS} and E_{AS} ratings are based on low frequency and duty cycles to keep T_J = +25°C.

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Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 9)						
Drain-Source Breakdown Voltage	BV_{DSS}	150	—	—	V	V_{GS} = 0V, I_D = 10mA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	μA	V_{DS} = 120V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 9)						
Gate Threshold Voltage	$V_{GS(TH)}$	1.3	—	2.6	V	V_{DS} = V_{GS}, I_D = 250μA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	14	17.5	mΩ	V_{GS} = 10V, I_D = 20A
		—	18	25.5		V_{GS} = 4.5V, I_D = 20A
Diode Forward Voltage	V_{SD}	—	0.8	1.2	V	V_{GS} = 0V, I_S = 20A
DYNAMIC CHARACTERISTICS (Note 10)						
Input Capacitance	C_{iss}	—	3369	—	pF	V_{DS} = 75V, V_{GS} = 0V f = 1MHz
Output Capacitance	C_{oss}	—	211	—		
Reverse Transfer Capacitance	C_{rss}	—	6.7	—		
Gate Resistance	R_g	—	1.9	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge	Q_g	—	50	—	nC	V_{DD} = 75V, I_D = 20A, V_{GS} = 10V
Gate-Source Charge	Q_{gs}	—	12.8	—		
Gate-Drain Charge	Q_{gd}	—	9.4	—		
Turn-On Delay Time	$t_{D(ON)}$	—	10.5	—	ns	V_{DD} = 75V, V_{GS} = 10V, I_D = 20A, R_g = 6Ω
Turn-On Rise Time	t_R	—	16.3	—		
Turn-Off Delay Time	$t_{D(OFF)}$	—	44.6	—		
Turn-Off Fall Time	t_F	—	17.7	—		
Reverse Recovery Time	t_{RR}	—	72	—	ns	I_F = 20A, di/dt = 100A/μs
Reverse Recovery Charge	Q_{RR}	—	215	—	nC	

Notes: 9. Short duration pulse test used to minimize self-heating effect.
10. Guaranteed by design. Not subject to product testing.

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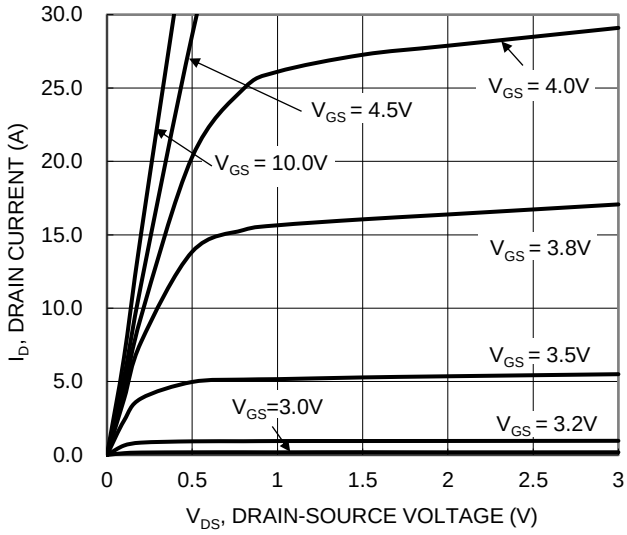


Figure 1. Typical Output Characteristic

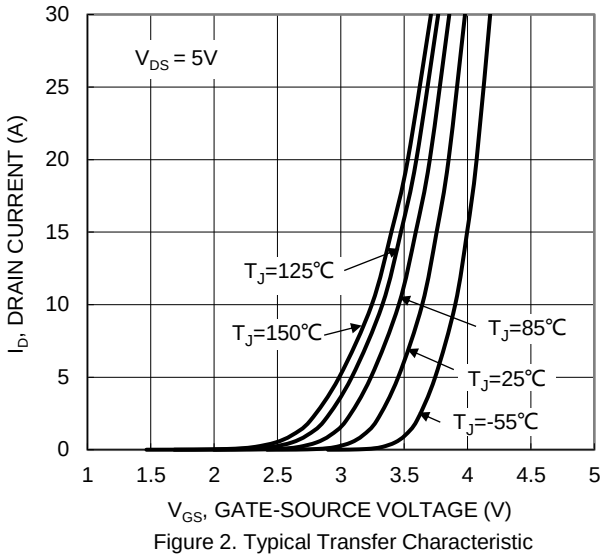


Figure 2. Typical Transfer Characteristic

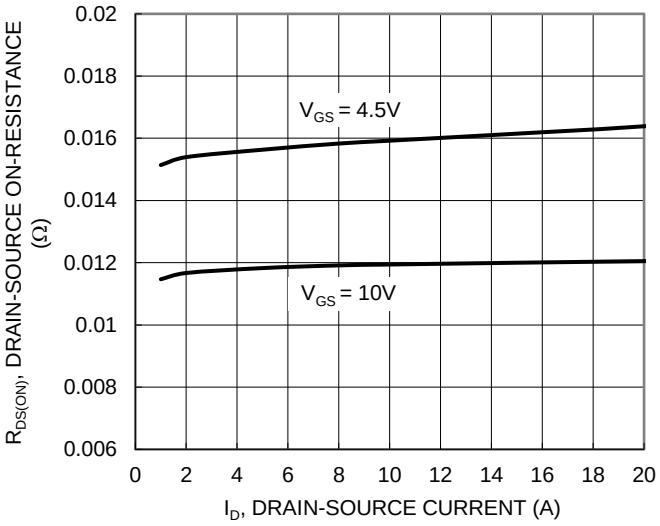


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

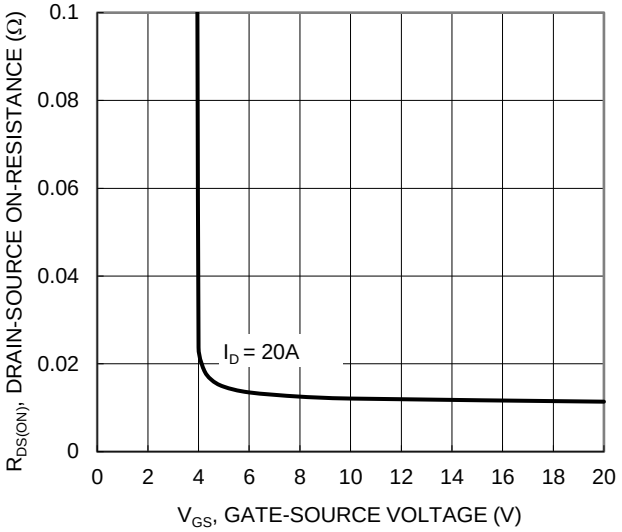


Figure 4. Typical Transfer Characteristic

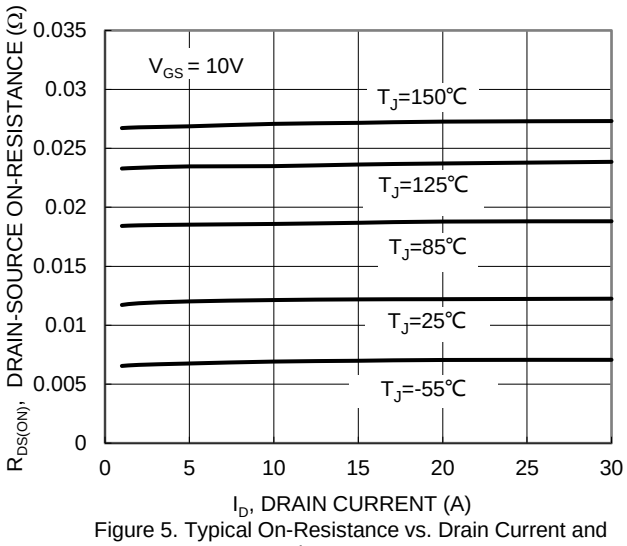


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

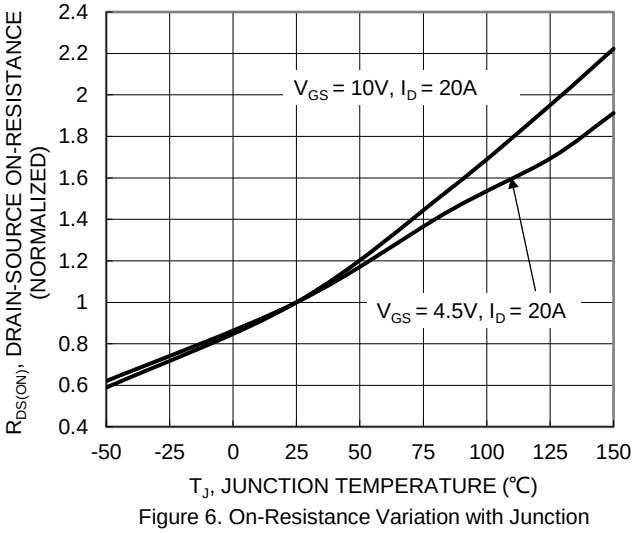


Figure 6. On-Resistance Variation with Junction Temperature

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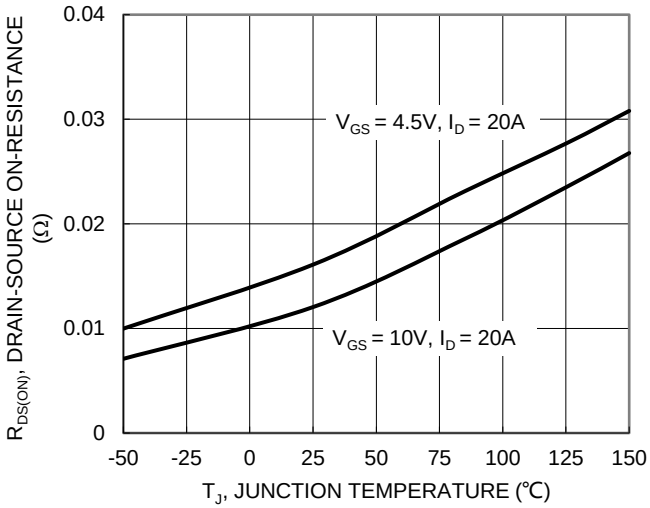


Figure 7. On-Resistance Variation with Junction Temperature

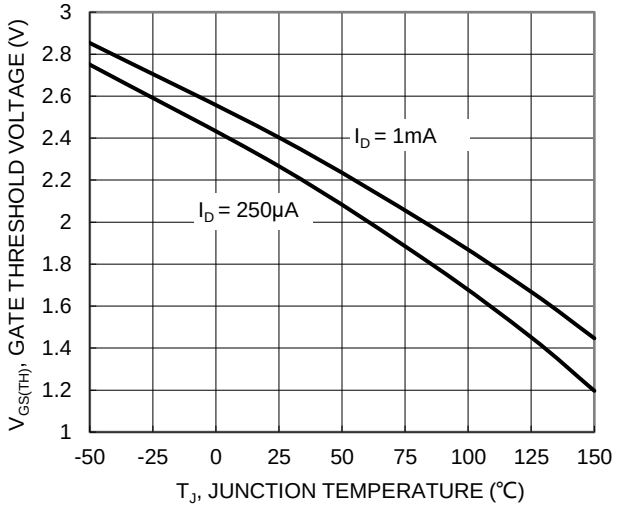


Figure 8. Gate Threshold Variation vs. Junction Temperature

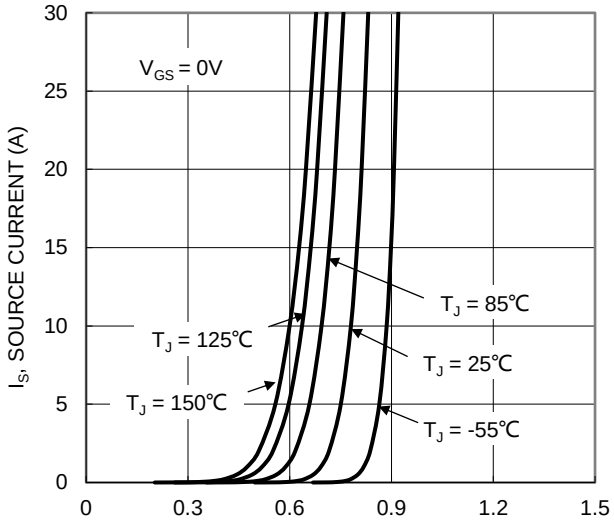


Figure 9. Diode Forward Voltage vs. Current

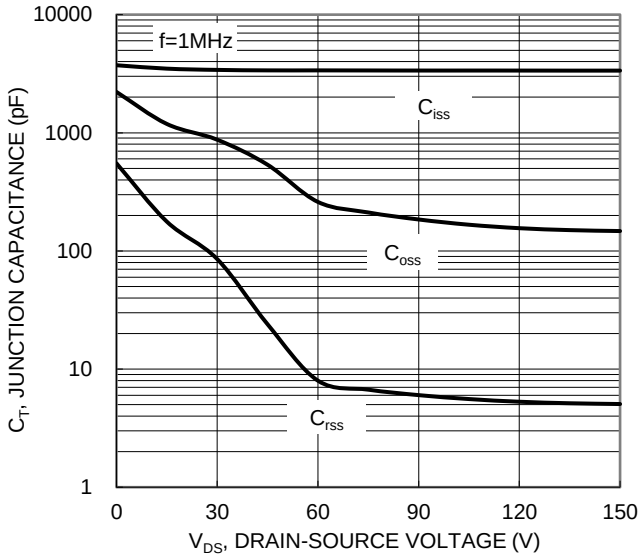


Figure 10. Typical Junction Capacitance

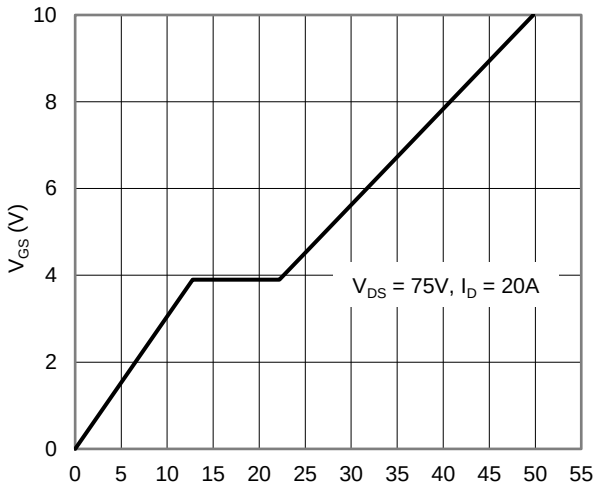


Figure 11. Gate Charge

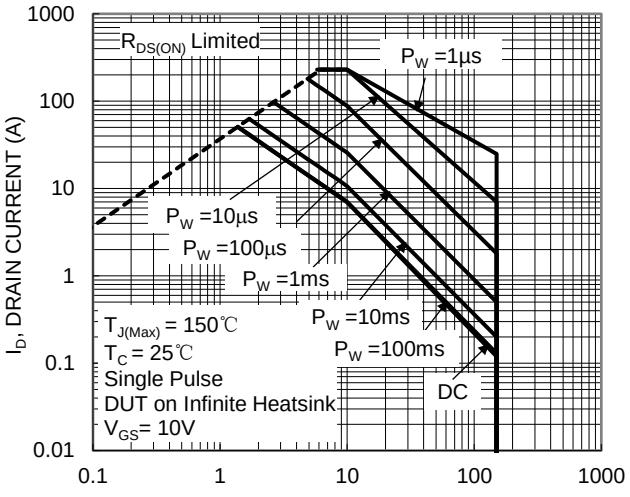


Figure 12. SOA, Safe Operation Area

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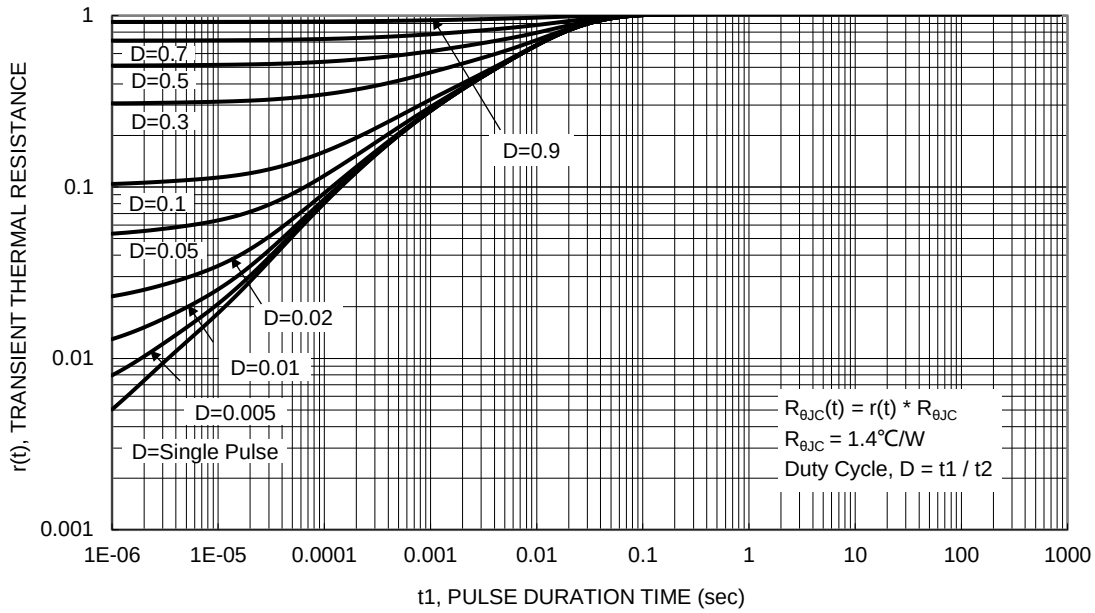


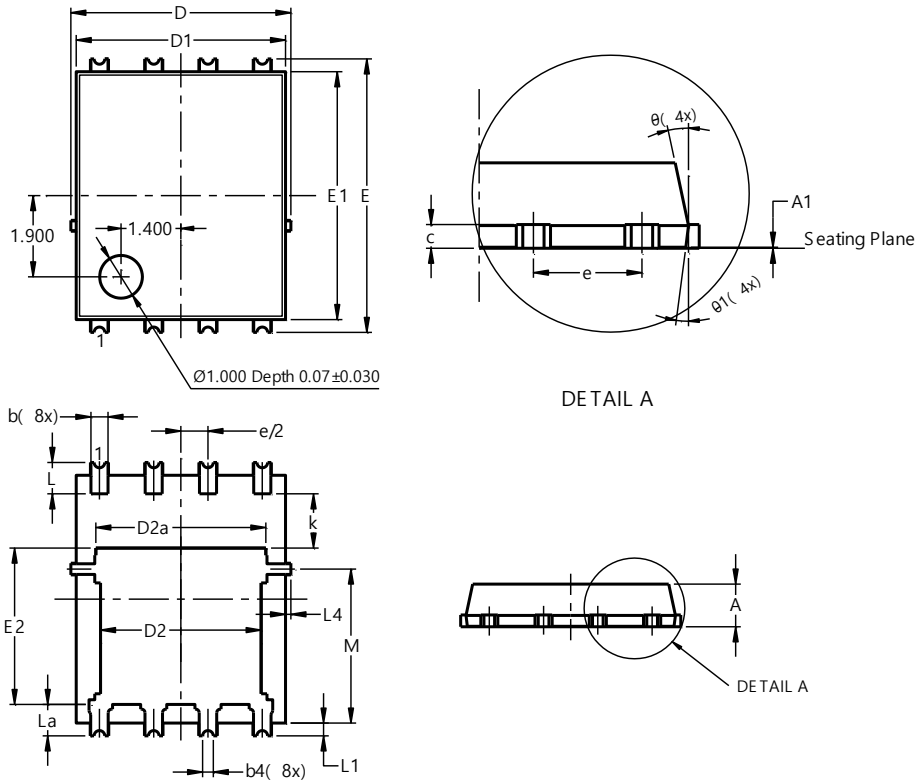
Figure 13. Transient Thermal Resistance

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Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI5060-8 (SWP) (Type UX)

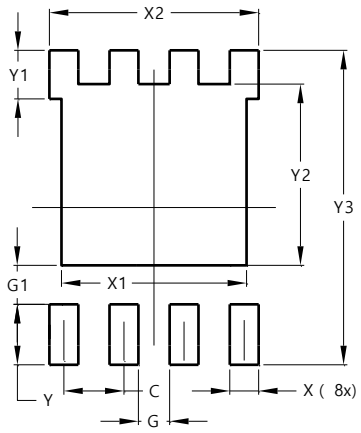


PowerDI5060-8 (SWP) (Type UX)			
Dim	**Min**	**Max**	**Typ**
A	0.90	1.10	1.00
A1	0	0.05	--
b	0.30	0.50	0.41
b2	0.20	0.35	0.25
b4	0.25REF		
c	0.230	0.330	0.277
D	5.15 BSC		
D1	4.70	5.10	4.90
D2	3.56	3.96	3.76
D2a	3.78	4.18	3.98
E	6.40 BSC		
E1	5.60	6.00	5.80
E2	3.46	3.86	3.66
E2a	4.195	4.595	4.395
e	1.27BSC		
k	1.05	--	--
L	0.635	0.835	0.735
La	0.635	0.835	0.735
L1	0.200	0.400	0.300
L1a	0.050REF		
L4	0.025	0.225	0.125
M	3.205	4.005	3.605
θ	10°	12°	11°
θ1	6°	8°	7°
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI5060-8 (SWP) (Type UX)



Dimensions	Value (in mm)
C	1.270
G	0.660
G1	0.820
X	0.610
X1	4.100
X2	4.420
Y	1.270
Y1	1.020
Y2	3.810
Y3	6.610

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