30V N-CHANNEL ENHANCEMENT MODE MOSFET
PowerDI3333-8

Product Summary

BV_{DSS}	$R_{DS(ON)}$ Max	I_D Max T_C = +25°C
30V	6mΩ @ V_{GS} = 10V	60A
	9mΩ @ V_{GS} = 4.5V	48A

Features

- Low $R_{DS(ON)}$ – Ensures On-State Losses are Minimized
- Small Form Factor Thermally Efficient Package Enables Higher Density End Products
- Occupies just 33% of the Board Area Occupied by SO-8 Enabling Smaller End Product
- 100% Unclamped Inductive Switching (UIS) Test in Production – Ensures More Reliable and Robust End Application
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

Description

This MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$) yet maintain superior switching performance, making it ideal for high efficiency power management applications.

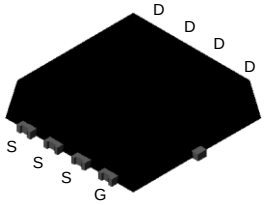
Applications

- Power Management Functions
- Analog Switch

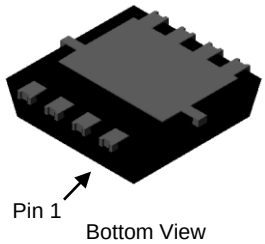
Mechanical Data

- Case: PowerDI®3333-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See Diagram
- Terminals: Finish — Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.03 grams (Approximate)

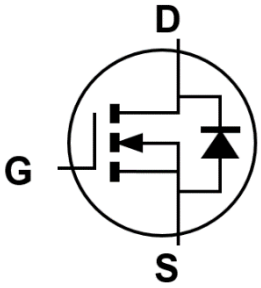
PowerDI3333-8 (SWP) (Type UX)



Top View



Bottom View



Equivalent Circuit

Ordering Information (Note 4)

Part Number	Case	Packaging
DMT35M4LFVW-7	PowerDI3333-8 (SWP) (Type UX)	2,000/Tape & Reel
DMT35M4LFVW-13	PowerDI3333-8 (SWP) (Type UX)	3,000/Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information



SH4 = Product Type Marking Code
YYWW = Date Code Marking
YY = Last Two Digits of Year (ex: 20 = 2020)
WW = Week Code (01 to 53)

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Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	30	V
Gate-Source Voltage			V_{GSS}	±20	V
Continuous Drain Current, V_{GS} = 10V (Note 6)	Steady State	T_A = +25°C T_A = +70°C	I_D	16 13	A
	Steady State	T_C = +25°C T_C = +70°C	I_D	60 48	A
Maximum Body Diode Forward Current (Note 6)			I_S	2.3	A
Pulsed Drain Current (380µs Pulse, Duty Cycle = 1%)			I_{DM}	110	A
Pulsed Drain Body Diode Forward Current (380µs Pulse, Duty Cycle = 1%)			I_{SM}	110	A
Avalanche Current (L = 0.1mH) (Note 8)			I_{AS}	22	A
Avalanche Energy (L = 0.1mH) (Note 8)			E_{AS}	25	mJ

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)		P_D	1.5	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{\theta JA}$	83.3	°C/W
Total Power Dissipation (Note 6)		P_D	2.2	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	55	°C/W
Thermal Resistance, Junction to Case (Note 7)		$R_{\theta JC}$	3.9	
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 9)						
Drain-Source Breakdown Voltage	BV_{DSS}	30	—	—	V	V_{GS} = 0V, I_D = 250µA
Zero Gate Voltage Drain Current T_J = +25°C	I_{DSS}	—	—	1	µA	V_{DS} = 24V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 9)						
Gate Threshold Voltage	$V_{GS(TH)}$	1.15	—	2.5	V	V_{DS} = V_{GS}, I_D = 250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	4.6	6	mΩ	V_{GS} = 10V, I_D = 20A
			6.5	9		V_{GS} = 4.5V, I_D = 15A
Diode Forward Voltage	V_{SD}	—	0.7	1	V	V_{GS} = 0V, I_S = 1A
DYNAMIC CHARACTERISTICS (Note 10)						
Input Capacitance	C_{iss}	—	982	—	pF	V_{DS} = 15V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	—	903	—		
Reverse Transfer Capacitance	C_{rss}	—	27	—		
Gate Resistance	R_g	—	2.2	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1.0MHz
Total Gate Charge (V_{GS} = 4.5V)	Q_g	—	7.9	—	nC	V_{DD} = 15V, I_D = 9A
Total Gate Charge (V_{GS} = 10V)	Q_g	—	16.1	—		
Gate-Source Charge	Q_{gs}	—	3.6	—		
Gate-Drain Charge	Q_{gd}	—	1.2	—		
Turn-On Delay Time	$t_{D(ON)}$	—	8.1	—	ns	V_{DD} = 15V, V_{GS} = 10V, R_g = 3Ω, I_D = 9A
Turn-On Rise Time	t_R	—	2.2	—		
Turn-Off Delay Time	$t_{D(OFF)}$	—	16.8	—		
Turn-Off Fall Time	t_F	—	5.7	—		

Notes:
5. Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate.
7. Thermal resistance from junction to soldering point (on the exposed drain pad).
8. I_{AS} and E_{AS} ratings are based on low frequency and duty cycles to keep T_J = +25°C.
9. Short duration pulse test used to minimize self-heating effect.
10. Guaranteed by design. Not subject to product testing.

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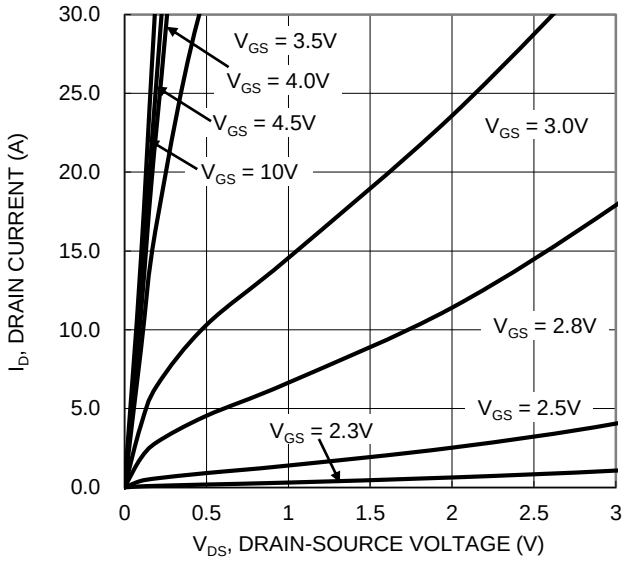


Figure 1. Typical Output Characteristic

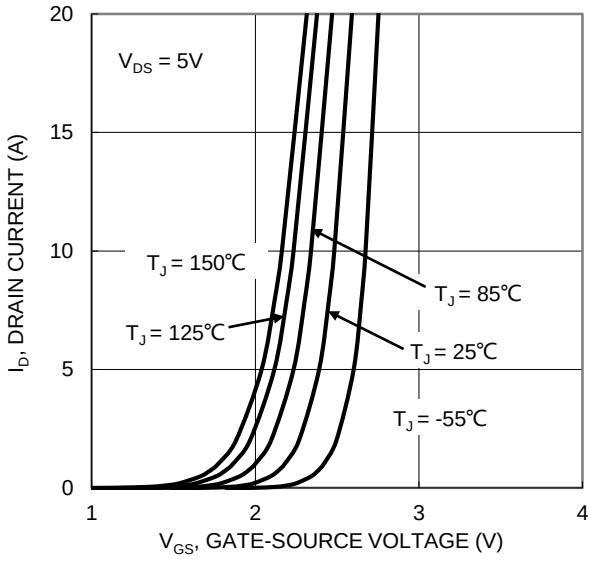


Figure 2. Typical Transfer Characteristic

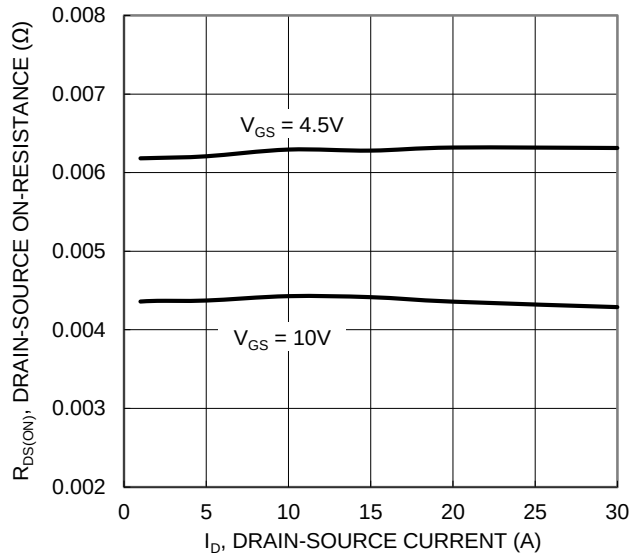


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

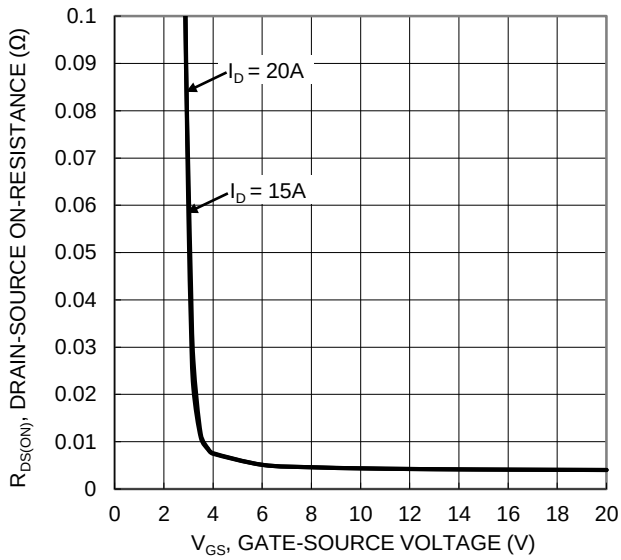


Figure 4. Typical Transfer Characteristic

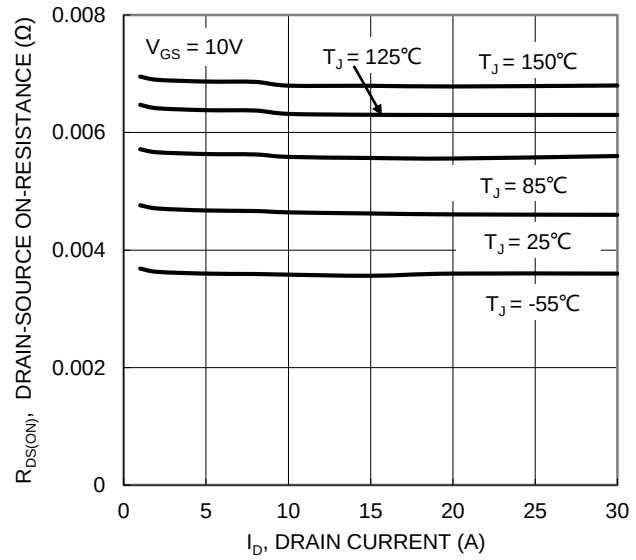


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

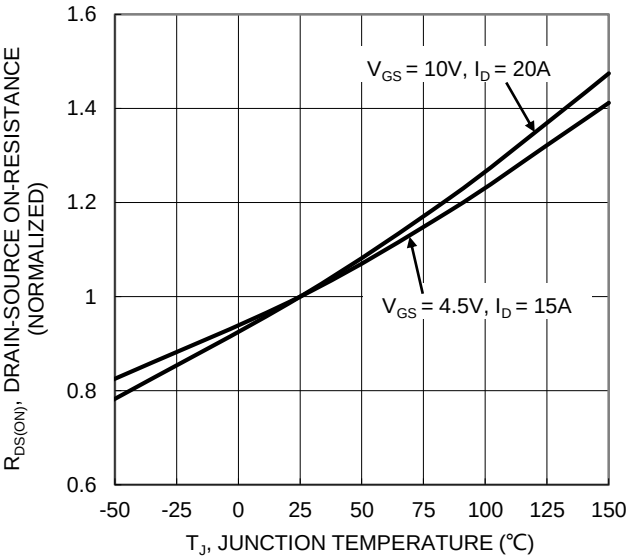


Figure 6. On-Resistance Variation with Junction Temperature

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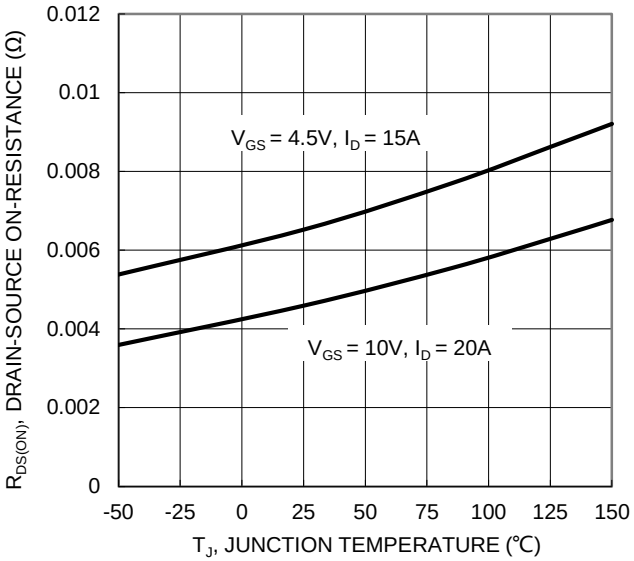


Figure 7. On-Resistance Variation with Junction Temperature

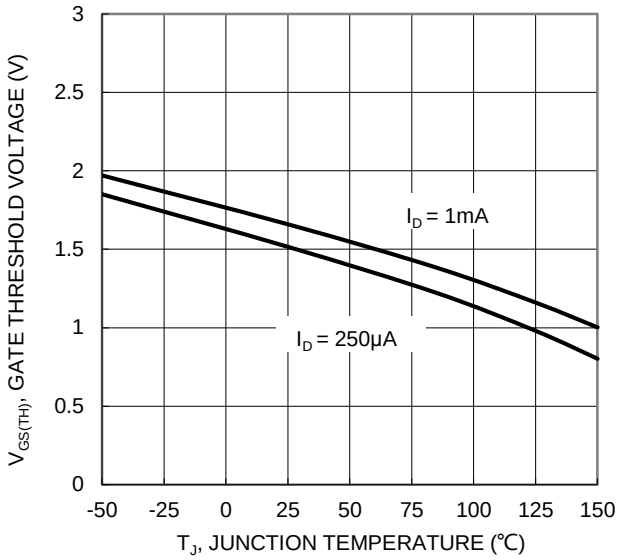


Figure 8. Gate Threshold Variation vs. Junction Temperature

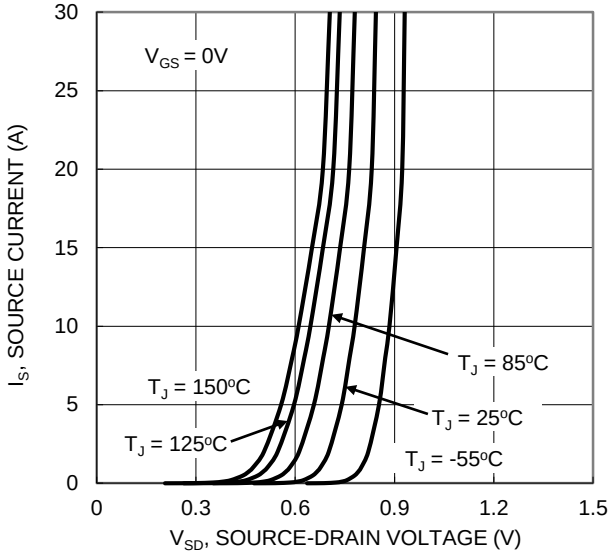


Figure 9. Diode Forward Voltage vs. Current

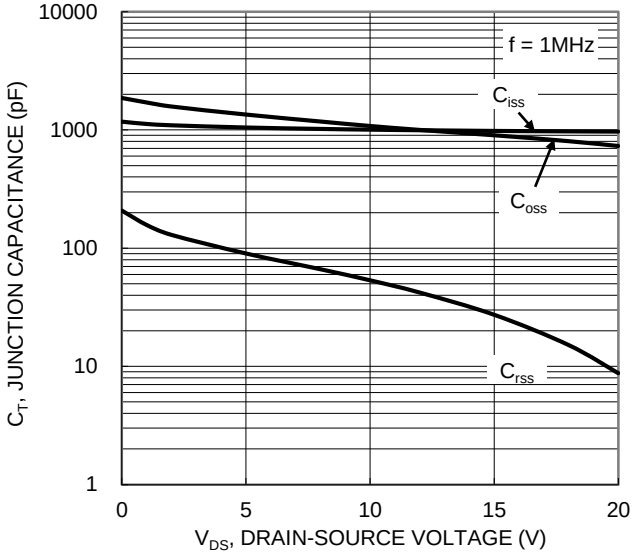


Figure 10. Typical Junction Capacitance

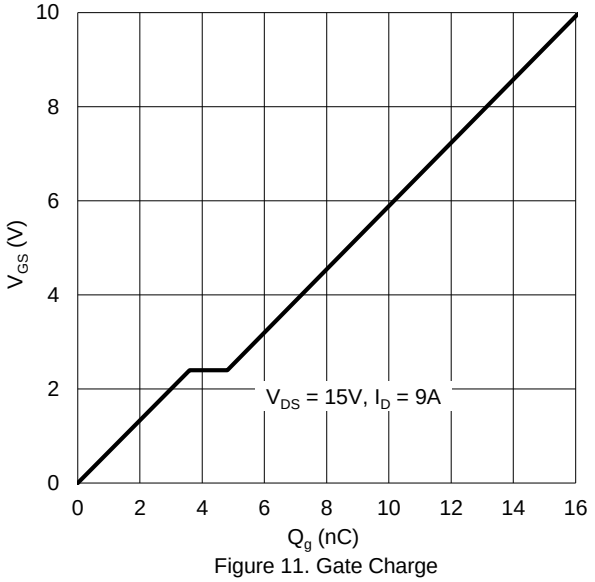


Figure 11. Gate Charge

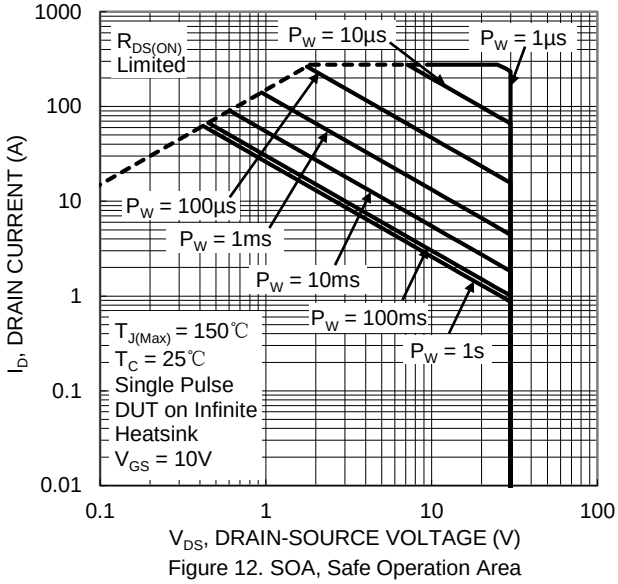


Figure 12. SOA, Safe Operation Area

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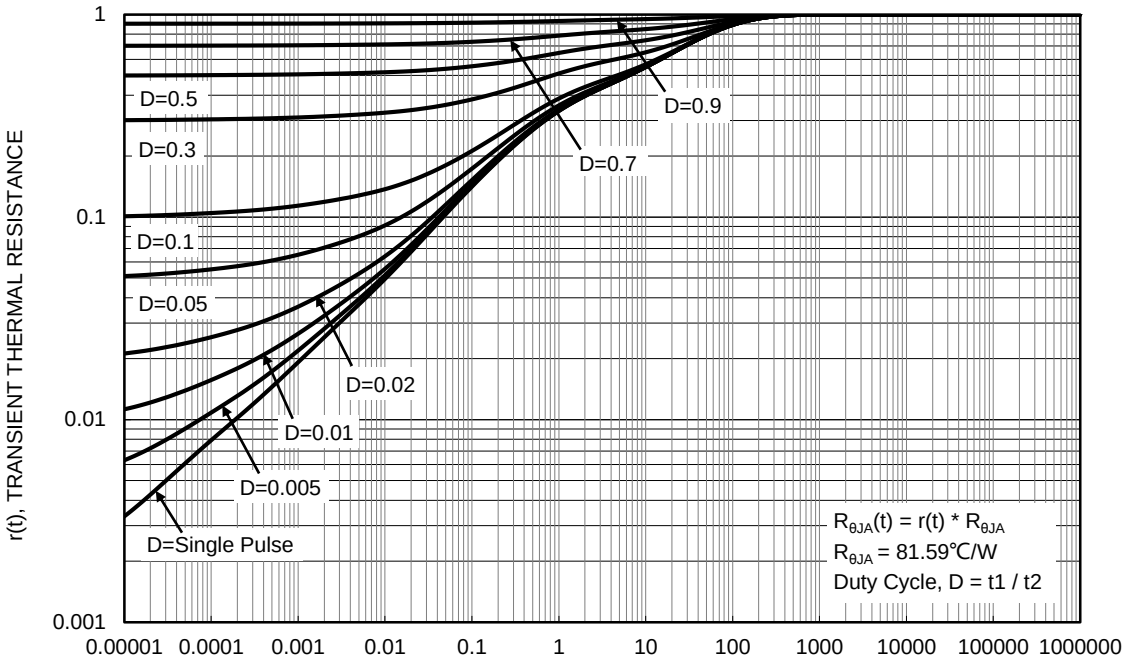


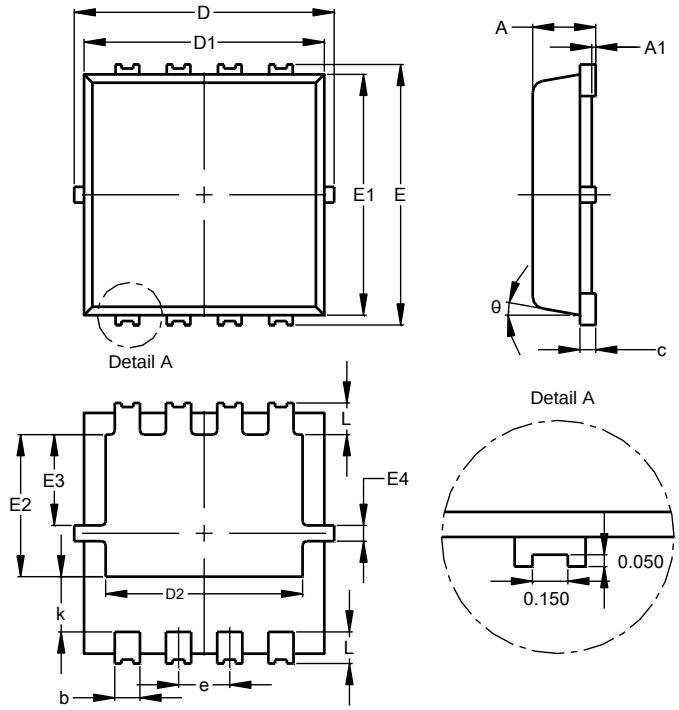
Figure 13. Transient Thermal Resistance

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Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI3333-8 (SWP) (Type UX)

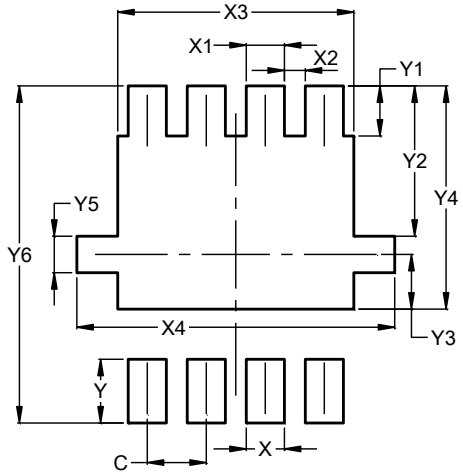


PowerDI3333-8 (SWP) (Type UX)			
Dim	**Min**	**Max**	**Typ**
A	0.75	0.85	0.80
A1	0.00	0.05	--
b	0.25	0.40	0.32
c	0.10	0.25	0.15
D	3.20	3.40	3.30
D1	2.95	3.15	3.05
D2	2.30	2.70	2.50
E	3.20	3.40	3.30
E1	2.95	3.15	3.05
E2	1.60	2.00	1.80
E3	0.95	1.35	1.15
E4	0.10	0.30	0.20
e	–	–	0.65
k	0.50	0.90	0.70
L	0.30	0.50	0.40
θ	0°	12°	10°
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI3333-8 (SWP) (Type UX)



Dimensions	Value (in mm)
C	0.650
X	0.420
X1	0.420
X2	0.230
X3	2.600
X4	3.500
Y	0.700
Y1	0.550
Y2	1.650
Y3	0.600
Y4	2.450
Y5	0.400
Y6	3.700

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