Product Summary

BV_{DSS}	$R_{DS(ON)}$ Max	I_D T_C = +25°C
60V	5.7mΩ @ V_{GS} = 10V	64.6A
	8.1mΩ @ V_{GS} = 4.5V	54.2A

Features and Benefits

- 100% Unclamped Inductive Switching (UIS) Test in Production – Ensures More Reliable And Robust End Application
- High Conversion Efficiency
- Low $R_{DS(ON)}$ – Minimizes On State Losses
- Low Input Capacitance
- Fast Switching Speed
- ESD Protected Gate
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Description and Applications

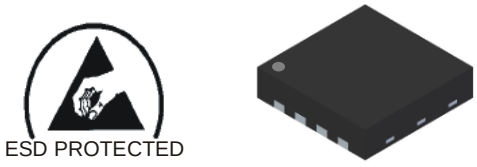
This new generation N-channel enhancement mode MOSFET is designed to minimize $R_{DS(ON)}$ and yet maintain superior switching performance. This device is ideal for use in Notebook battery power management and load switch.

- Synchronous Rectifier
- Power Management Functions
- DC-DC Converters

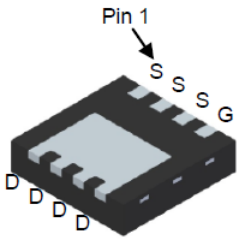
Mechanical Data

- Case: V-DFN3333-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See Below Diagram
- Terminals: Finish—NiPdAu over Copper Leadframe. Solderable per MIL-STD-202, Method 208 e4
- Weight: 0.027 grams (Approximate)

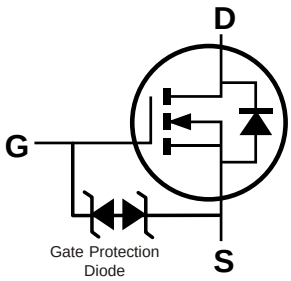
V-DFN3333-8 (Type B)



Top View



Bottom View



Equivalent Circuit

Ordering Information (Note 4)

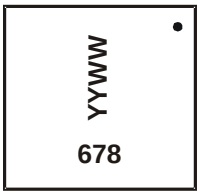
Part Number	Case	Packaging
DMT67M8LCG-7	V-DFN3333-8 (Type B)	2,000/Tape & Reel
DMT67M8LCG-13	V-DFN3333-8 (Type B)	3,000/Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

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Marking Information

Site1:



678 = Product Type Marking Code
YYWW = Date Code Marking
YY = Year (ex: 19 = 2019)
WW = Week (01 to 53)

Site2:



678 = Product Type Marking Code
YWX = Date Code Marking
Y = Year (ex: 9 = 2019)
W = Week (ex: a = week 27; z Represents Week 52 and 53)
X = Internal Code (ex: U = Monday)

Date Code Key

Year	2017	2018	2019	2020	2021	2022	2023	2024	2025
Code	7	8	9	0	1	2	3	4	5

Week	1-26	27-52	53
Code	A-Z	a-z	z

Internal Code	Sun	Mon	Tue	Wed	Thu	Fri	Sat
Code	T	U	V	W	X	Y	Z

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Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Drain-Source Voltage		V_{DSS}	60	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current, V_{GS} = 10V (Note 6)	T_A = +25°C T_A = +70°C	I_D	16 12.8	A
Continuous Drain Current, V_{GS} = 10V (Note 7)	T_C = +25°C T_C = +70°C	I_D	64.6 51.7	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)		I_{DM}	256	A
Maximum Continuous Body Diode Forward Current (Note 6)		I_S	64	A
Pulsed Body Diode Forward Current (10µs Pulse, Duty Cycle = 1%)		I_{SM}	256	A
Avalanche Current, L=0.3mH		I_{AS}	23.7	A
Avalanche Energy, L=0.3mH		E_{AS}	84.5	mJ

Thermal Characteristics

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)	T_A = +25°C	P_D	0.9	W
Thermal Resistance, Junction to Ambient (Note 5)		$R_{\theta JA}$	138	°C/W
Total Power Dissipation (Note 6)	T_A = +25°C	P_D	2.2	W
Thermal Resistance, Junction to Ambient (Note 6)		$R_{\theta JA}$	57	°C/W
Thermal Resistance, Junction to Case (Note 7)		$R_{\theta JC}$	3.5	°C/W
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV_{DSS}	60	—	—	V	V_{GS} = 0V, I_D = 1mA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	µA	V_{DS} = 48V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±10	µA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	$V_{GS(TH)}$	1.2	—	2.5	V	V_{DS} = V_{GS}, I_D = 250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	4.3	5.7	mΩ	V_{GS} = 10V, I_D = 20A
		—	6.1	8.1		V_{GS} = 4.5V, I_D = 18A
Diode Forward Voltage	V_{SD}	—	0.8	1.2	V	V_{GS} = 0V, I_S = 13.5A
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C_{iss}	—	2130	—	pF	V_{DS} = 30V, V_{GS} = 0V, f = 1MHz
Output Capacitance	C_{oss}	—	786	—		
Reverse Transfer Capacitance	C_{rss}	—	70	—		
Gate Resistance	R_g	—	0.6	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge (V_{GS} = 4.5V)	Q_g	—	20	—	nC	V_{DS} = 30V, I_D = 20A
Total Gate Charge (V_{GS} = 10V)	Q_g	—	37.5	—		
Gate-Source Charge	Q_{gs}	—	5.4	—		
Gate-Drain Charge	Q_{gd}	—	9.5	—		
Turn-On Delay Time	$t_{D(ON)}$	—	5.5	—	ns	V_{DD} = 30V, V_{GS} = 10V, I_D = 20A, R_G = 3Ω
Turn-On Rise Time	t_R	—	6.8	—		
Turn-Off Delay Time	$t_{D(OFF)}$	—	22.1	—		
Turn-Off Fall Time	t_F	—	10.8	—		
Reverse Recovery Time	t_{RR}	—	26.9	—	ns	I_F = 20A, di/dt = 300A/µs
Reverse Recovery Charge	Q_{RR}	—	56.8	—	nC	

Notes:
5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
7. Thermal resistance from junction to soldering point (on the exposed drain pad).
8. Short duration pulse test used to minimize self-heating effect.
9. Guaranteed by design. Not subject to product testing.

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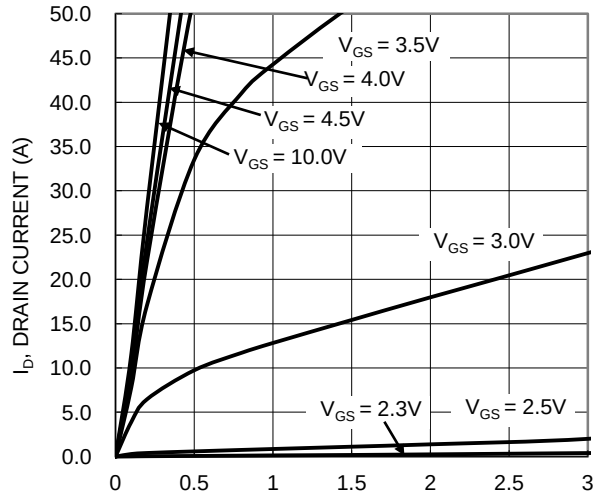


Figure 1.Typical Output Characteristic

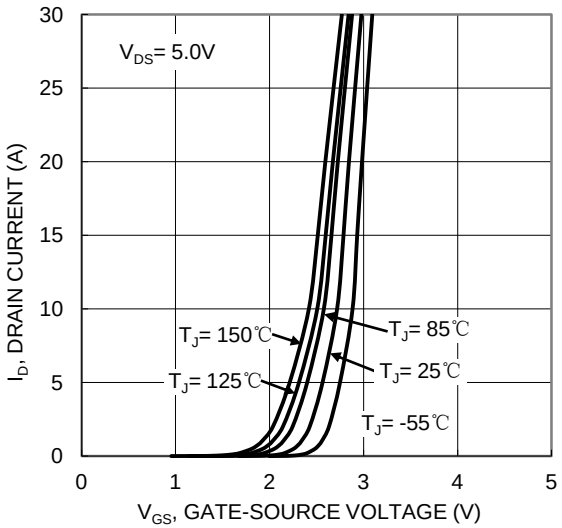


Figure 2. Typical Transfer Characteristic

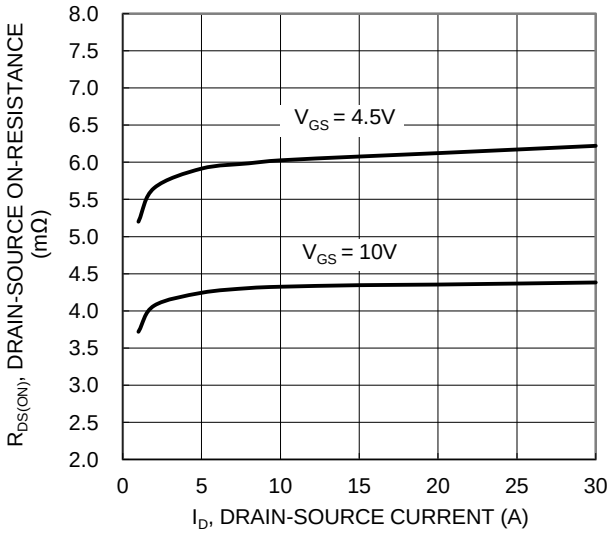


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

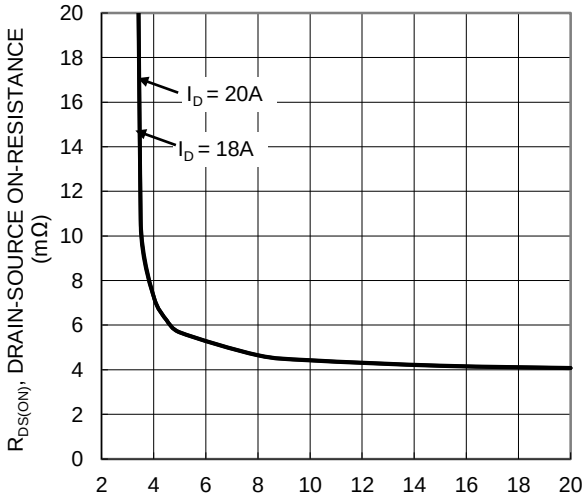


Figure 4. Typical Transfer Characteristic

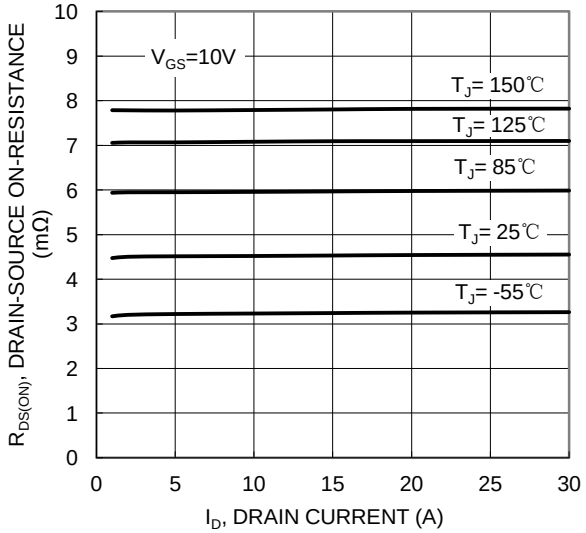


Figure 5. Typical On-Resistance vs. Drain Current and Temperature

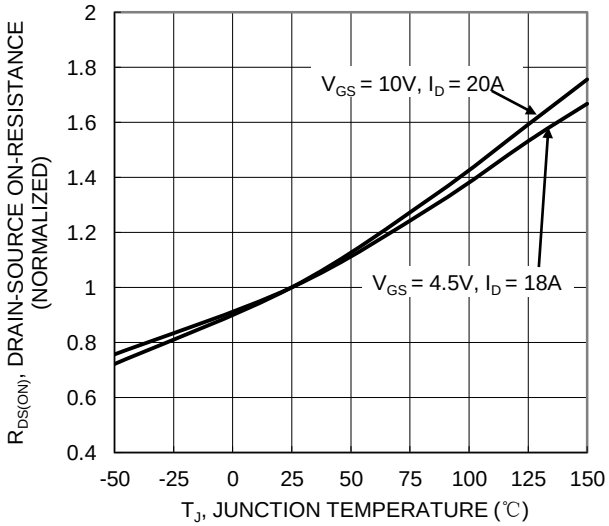


Figure 6. On-Resistance Variation with Temperature

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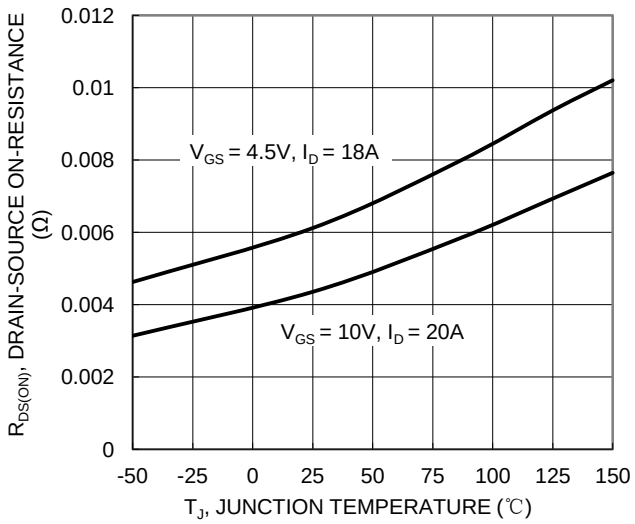


Figure 7. On-Resistance Variation with Temperature

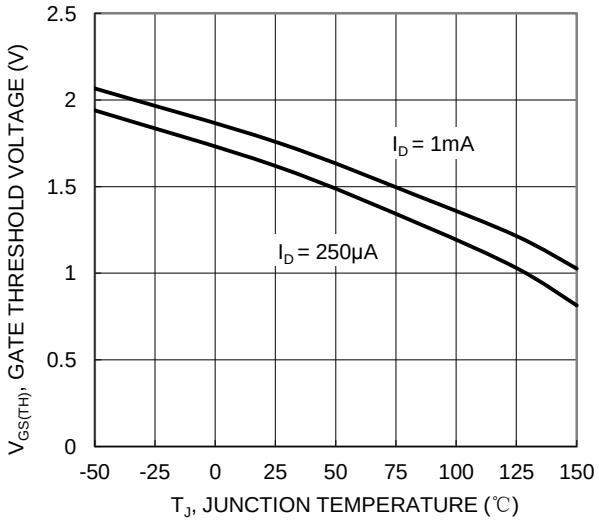


Figure 8. Gate Threshold Variation vs. Temperature

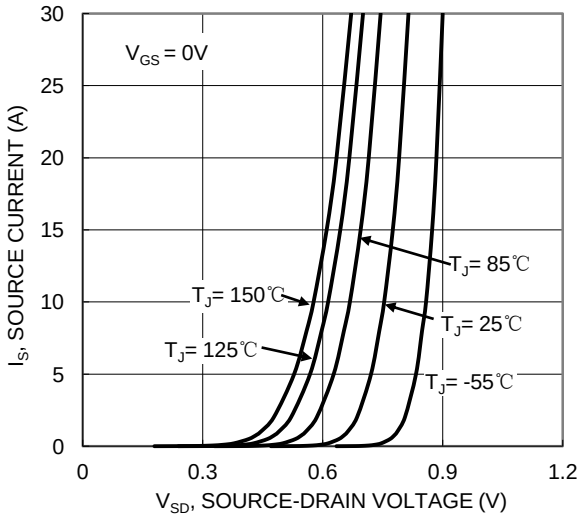


Figure 9. Diode Forward Voltage vs. Current

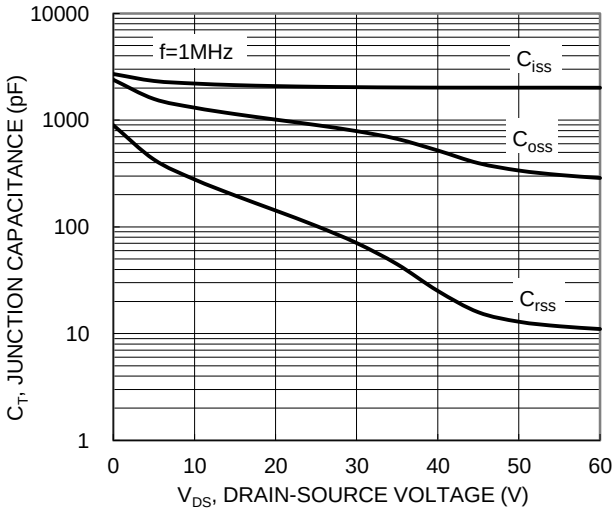


Figure 10. Typical Junction Capacitance

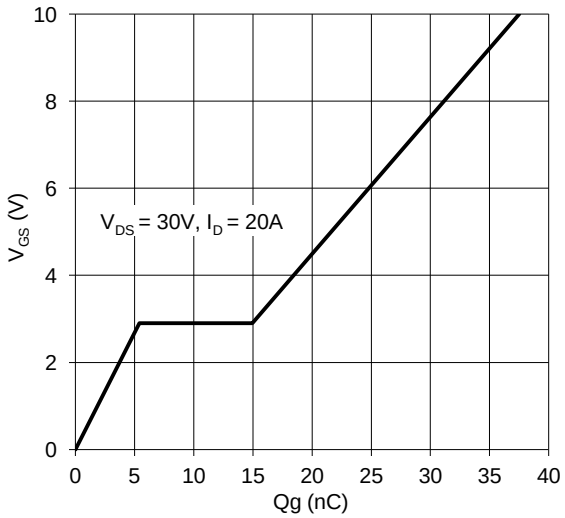


Figure 11. Gate Charge

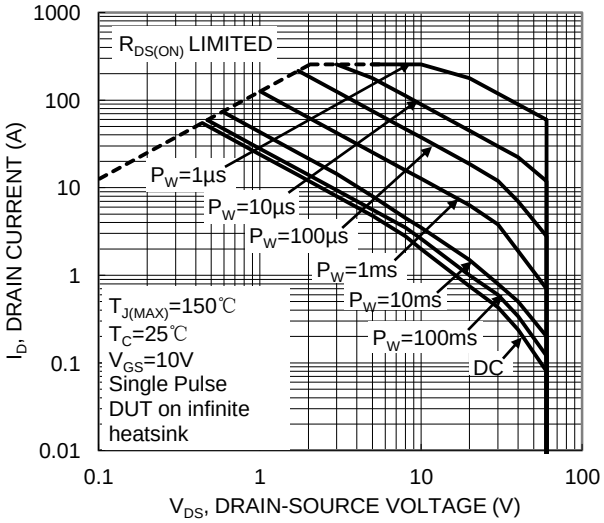


Figure 12. SOA, Safe Operation Area

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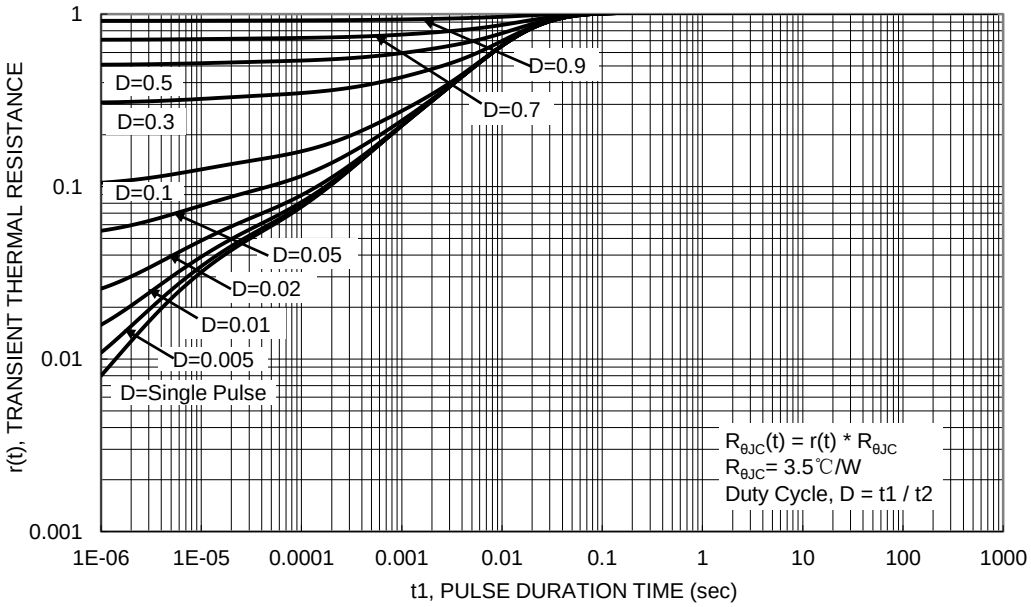


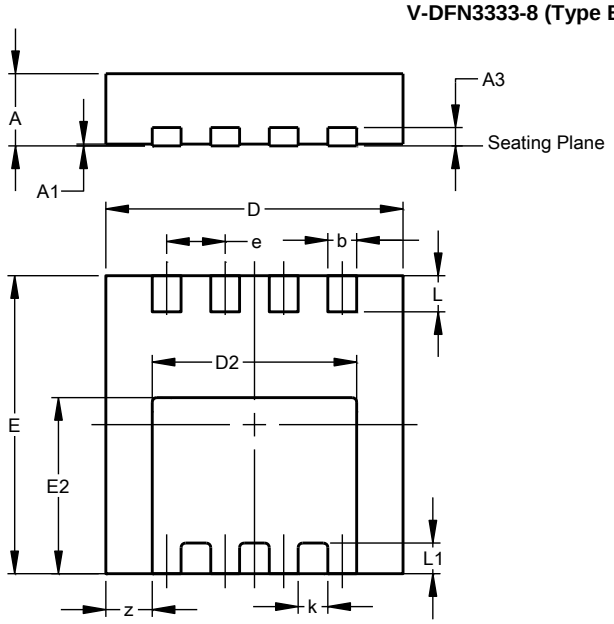
Figure 13. Transient Thermal Resistance

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Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

V-DFN3333-8 (Type B)

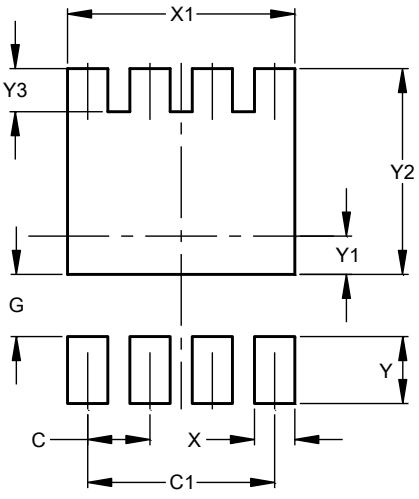


V-DFN3333-8 (Type B)			
Dim	**Min**	**Max**	**Typ**
A	0.75	0.85	0.80
A1	0.00	0.05	0.02
A3	--	--	0.203
b	0.27	0.37	0.32
D	3.25	3.35	3.30
D2	2.17	2.37	2.27
E	3.25	3.35	3.30
E2	1.85	2.05	1.95
e	--	--	0.65
k	--	--	0.33
L	0.35	0.45	0.40
L1	--	--	0.34
z	--	--	0.515
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

V-DFN3333-8 (Type B)



Dimensions	Value (in mm)
C	0.650
C1	1.950
G	0.650
X	0.420
X1	2.370
Y	0.700
Y1	0.400
Y2	2.150
Y3	0.450

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