80V N-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

BV_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX T_A = +25°C
80V	25mΩ @ V_{GS} = 10V	7.5A
	38mΩ @ V_{GS} = 4.5V	6.1A

Description

This new generation MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$) yet maintain superior switching performance, making it ideal for high-efficiency power-management applications.

Applications

- Power-management functions
- Battery operated systems and solid-state relays
- Drivers: relays, solenoids, lamps, hammers, displays, memories, transistors, etc.

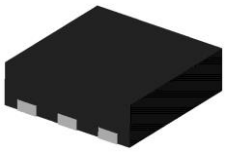
Features and Benefits

- 0.6mm Profile – Ideal for Low Profile Applications
- PCB Footprint of 4mm^2
- Low On-Resistance
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

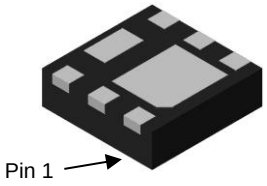
Mechanical Data

- Package: U-DFN2020-6
- Package Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – NiPdAu over Copper Leadframe. Solderable per MIL-STD-202, Method 208 e4
- Weight: 0.0065 grams (Approximate)

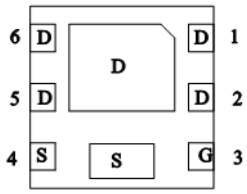
U-DFN2020-6 (Type F)



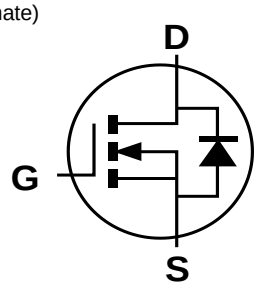
Top View



Bottom View



Pinout
Bottom View



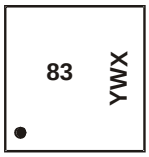
Equivalent Circuit

Ordering Information (Note 4)

Part Number	Package	Packing	
		Qty.	Carrier
DMT8030LFDF-7	U-DFN2020-6 (Type F)	3,000	Reel
DMT8030LFDF-13	U-DFN2020-6 (Type F)	10,000	Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information



83 = Product Type Marking Code
YWX = Date Code Marking
Y or Y = Year (ex: 4 = 2024)
W = Week (ex: a = week 27; z represents week 52 and 53)
X = Internal Code (ex: U = Monday)

Date Code Key

Year	2019	-	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033
Code	9	-	4	5	6	7	8	9	0	1	2	3

Week	1-26	27-52	53
Code	A-Z	a-z	z

Internal Code	Sun	Mon	Tue	Wed	Thu	Fri	Sat
Code	T	U	V	W	X	Y	Z

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Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Drain-Source Voltage		V_{DSS}	80	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current, V_{GS} = 10V (Note 5)	T_A = +25°C	I_D	7.5	A
	T_A = +70°C		6.1	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)		I_{DM}	40	A
Maximum Body Diode Continuous Current		I_S	7.5	A
Pulsed Body Diode Current (10µs Pulse, T_C = +25°C, Package Limited)		I_{SM}	40	A
Avalanche Current, L = 0.3mH		I_{AS}	12.5	A
Avalanche Energy, L = 0.3mH		E_{AS}	23.4	mJ

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 6)	T_A = +25°C	P_D	1.2	W
	T_A = +70°C		0.7	
Thermal Resistance, Junction to Ambient (Note 6)		$R_{\theta JA}$	103	°C/W
Total Power Dissipation (Note 5)	T_A = +25°C	P_D	2.2	W
	T_A = +70°C		1.4	
Thermal Resistance, Junction to Ambient (Note 5)		$R_{\theta JA}$	58	°C/W
Thermal Resistance, Junction to Case (Note 5)		$R_{\theta JC}$	6.7	
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	80	—	—	V	V_{GS} = 0V, I_D = 1mA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	µA	V_{DS} = 64V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(TH)}$	1.2	—	2.5	V	V_{DS} = V_{GS}, I_D = 250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	23.8	25	mΩ	V_{GS} = 10V, I_D = 5A
		—	33.6	38		V_{GS} = 4.5V, I_D = 4A
Diode Forward Voltage	V_{SD}	—	0.7	1.2	V	V_{GS} = 0V, I_S = 10A
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	641	—	pF	V_{DS} = 25V, V_{GS} = 0V f = 1.0MHz
Output Capacitance	C_{oss}	—	272	—		
Reverse Transfer Capacitance	C_{rss}	—	32	—		
Gate Resistance	R_g	—	1.4	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1.0MHz
Total Gate Charge (V_{GS} = 4.5V)	Q_g	—	5.4	—	nC	V_{DS} = 40V, I_D = 7.5A
Total Gate Charge (V_{GS} = 10V)	Q_g	—	10.4	—		
Gate-Source Charge	Q_{gs}	—	1.8	—		
Gate-Drain Charge	Q_{gd}	—	2.4	—		
Turn-On Delay Time	$t_{D(ON)}$	—	11.3	—	ns	V_{DD} = 40V V_{GS} = 4.5V, R_g = 2.7Ω I_D = 10A
Turn-On Rise Time	t_R	—	14.3	—		
Turn-Off Delay Time	$t_{D(OFF)}$	—	10.8	—		
Turn-Off Fall Time	t_F	—	8.3	—		
Body Diode Reverse-Recovery Time	t_{RR}	—	25.5	—	ns	I_F = 7.5A, di/dt = 100A/µs
Body Diode Reverse-Recovery Charge	Q_{RR}	—	20.6	—	nC	I_F = 7.5A, di/dt = 100A/µs

Notes:
5. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.

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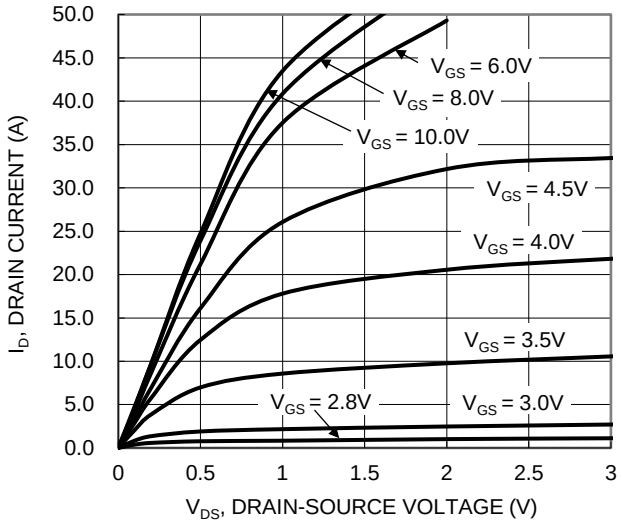


Figure 1. Typical Output Characteristic

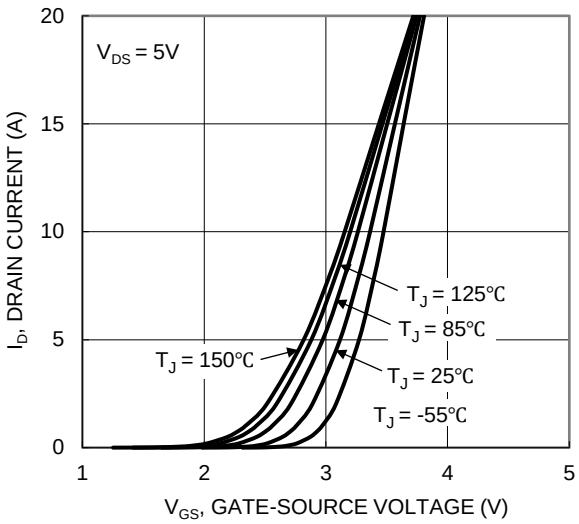


Figure 2. Typical Transfer Characteristic

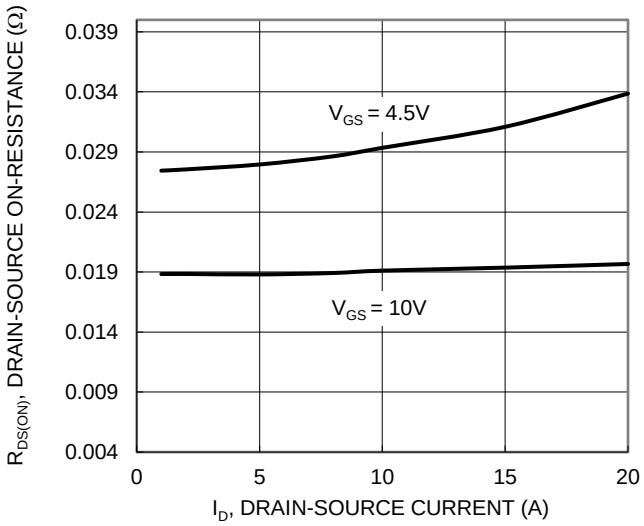


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

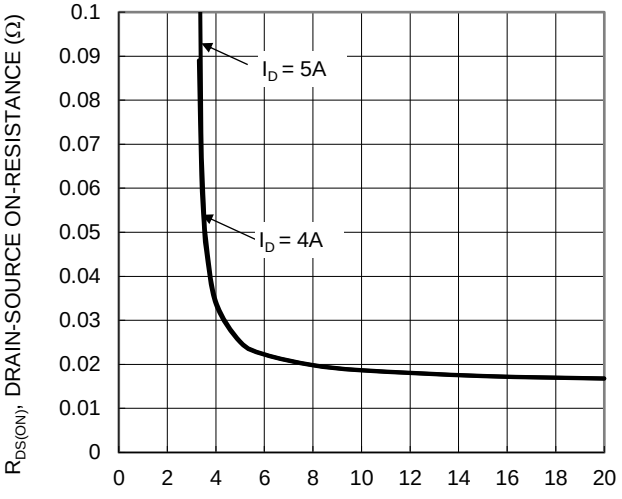


Figure 4. Typical Transfer Characteristic

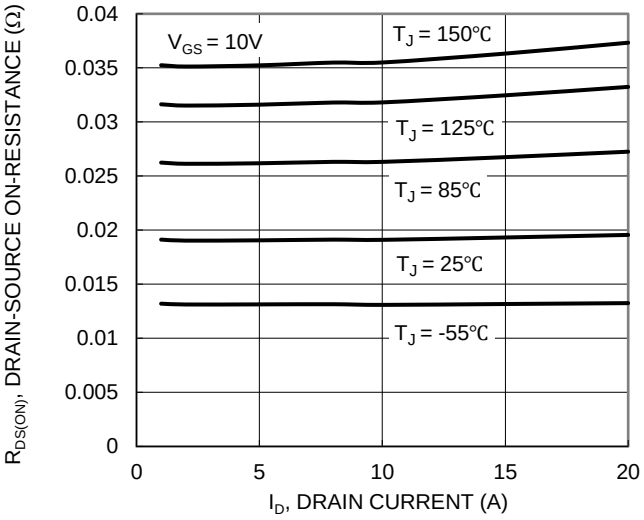


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

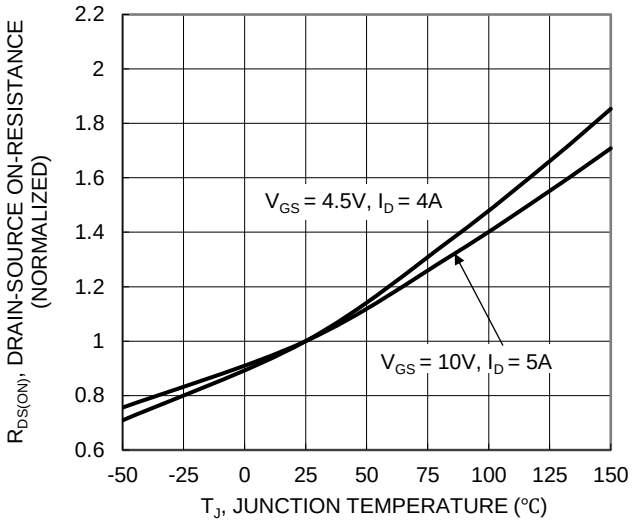


Figure 6. On-Resistance Variation with Junction Temperature

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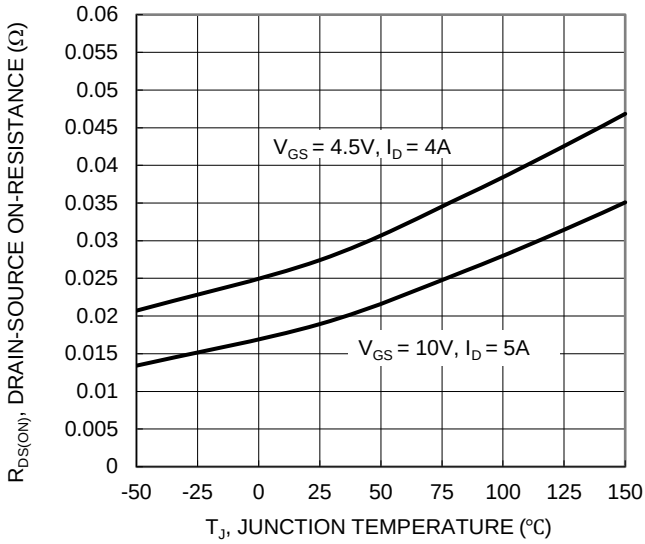


Figure 7. On-Resistance Variation with Junction Temperature

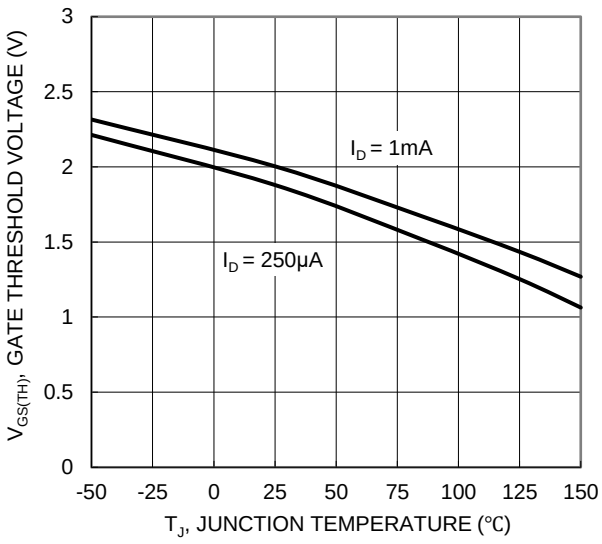


Figure 8. Gate Threshold Variation vs. Junction Temperature

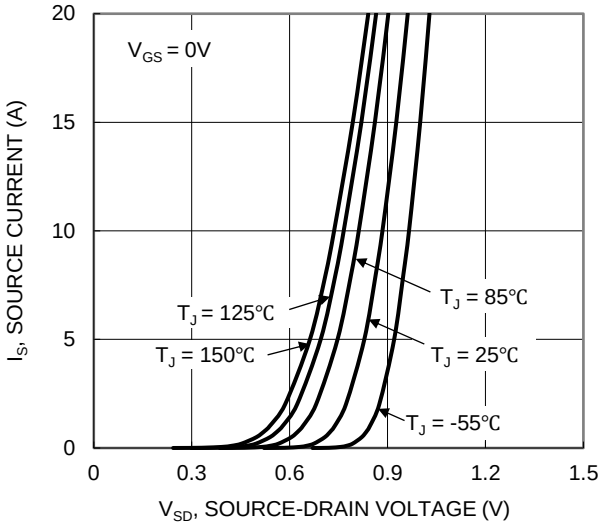


Figure 9. Diode Forward Voltage vs. Current

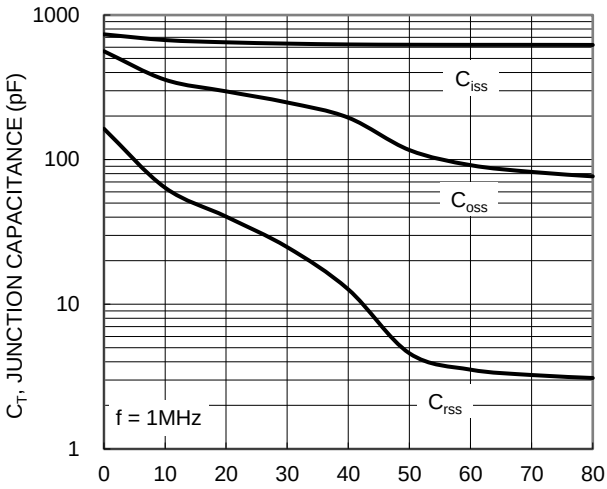


Figure 10. Typical Junction Capacitance

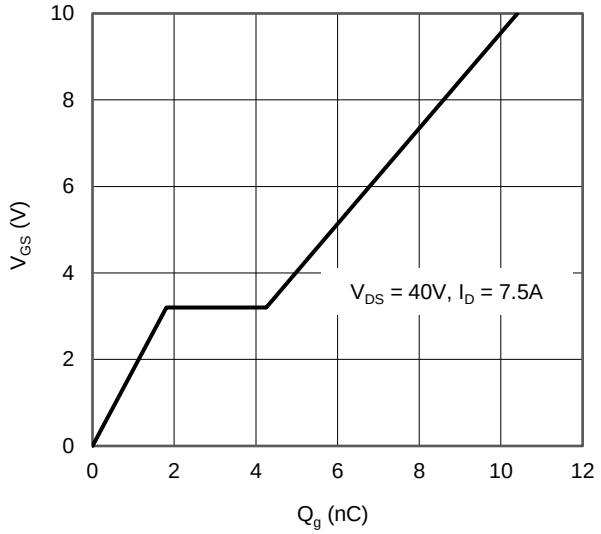


Figure 11. Gate Charge

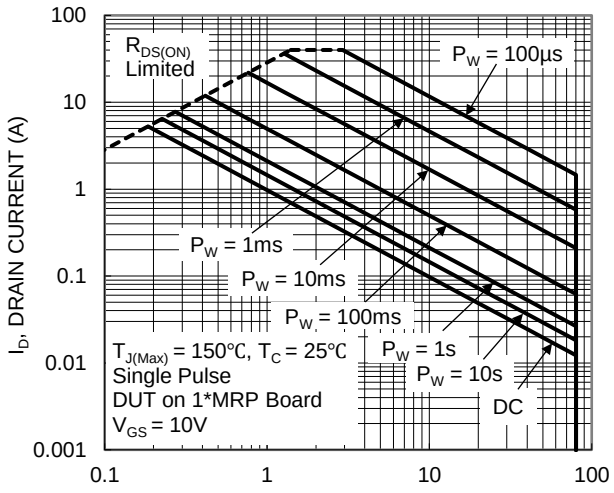


Figure 12. SOA, Safe Operation Area

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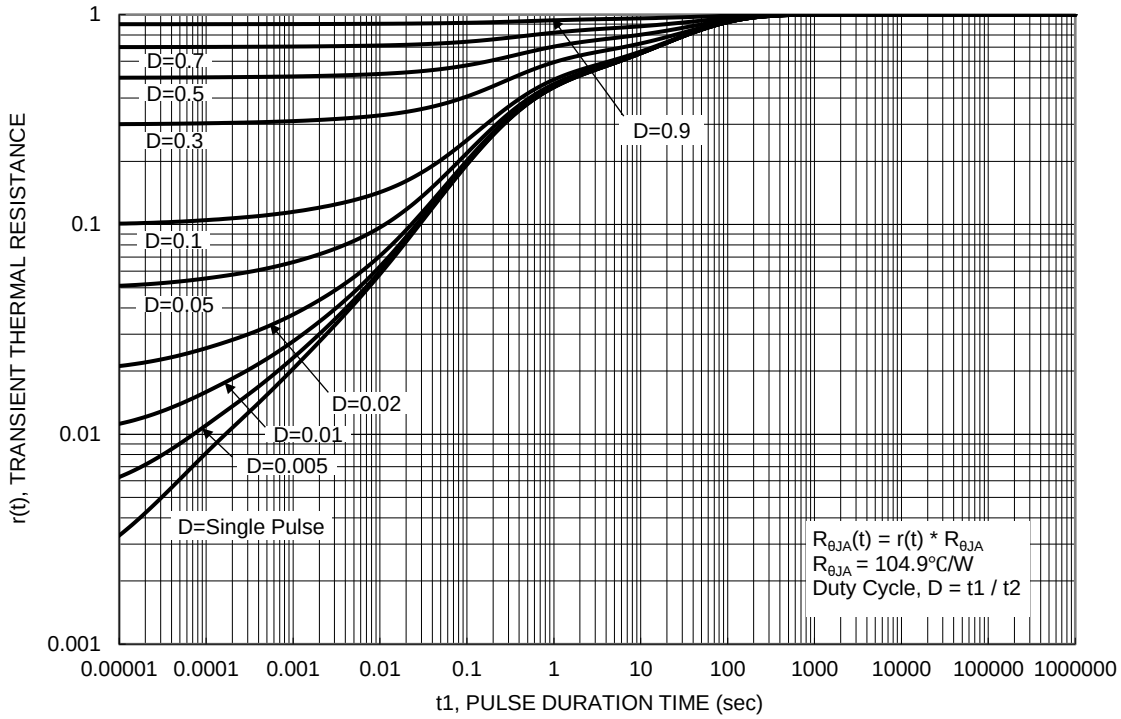


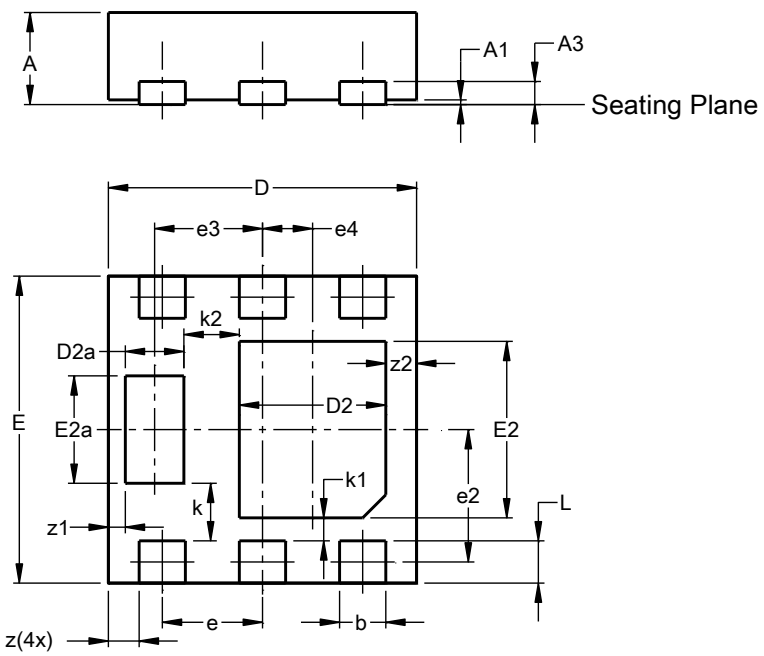
Figure 13. Transient Thermal Resistance

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Package Outline Dimension

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-DFN2020-6 (Type F)

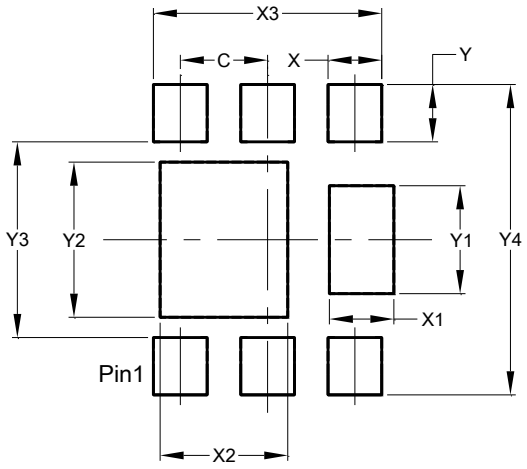


U-DFN2020-6 (Type F)			
Dim	**Min**	**Max**	**Typ**
A	0.57	0.63	0.60
A1	0.00	0.05	0.03
A3	-	-	0.15
b	0.25	0.35	0.30
D	1.95	2.05	2.00
D2	0.85	1.05	0.95
D2a	0.33	0.43	0.38
E	1.95	2.05	2.00
E2	1.05	1.25	1.15
E2a	0.65	0.75	0.70
e	0.65 BSC		
e2	0.863 BSC		
e3	0.70 BSC		
e4	0.325 BSC		
k	0.37 BSC		
k1	0.15 BSC		
k2	0.36 BSC		
L	0.225	0.325	0.275
z	0.20 BSC		
z1	0.110 BSC		
z2	0.20 BSC		
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-DFN2020-6 (Type F)



Dimensions	Value (in mm)
C	0.650
X	0.400
X1	0.480
X2	0.950
X3	1.700
Y	0.425
Y1	0.800
Y2	1.150
Y3	1.450
Y4	2.300

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