100V 175°C N-CHANNEL ENHANCEMENT MODE MOSFET
PowerDI®5060-8

Product Summary

BV_{DSS}	$R_{DS(ON)}$ Max	I_D T_C = +25°C
100V	14.5mΩ @ V_{GS} = 10V	56A
	19.5mΩ @ V_{GS} = 6V	49A

Description and Applications

This new generation N-Channel enhancement mode MOSFET is designed to minimize $R_{DS(ON)}$ yet maintain superior switching performance. This device is ideal for use in:

- Motor control
- DC-DC converters
- Power management

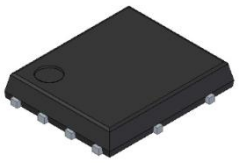
Features

- Rated to +175°C — Ideal for High Ambient Temperature Environments
- 100% Unclamped Inductive Switching (UIS) Test in Production — Ensures More Reliable and Robust End Application
- Thermally Efficient Package — Cooler Running Applications
- Low $R_{DS(ON)}$ — Minimizes On-State Losses
- Low Input Capacitance
- Fast Switching Speed
- **Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **This part is qualified to JEDEC standards (as references in AEC-Q) for High Reliability. https://www.diodes.com/quality/product-definitions/**
- **An automotive-compliant part is available under a separate datasheet (DMTH10H015SPSQ)**

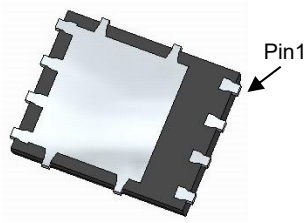
Mechanical Data

- Package: PowerDI5060-8
- Package Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See Diagram
- Terminals: Finish – Matte Tin Annealed over Copper Lead-Frame. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.097 grams (Approximate)

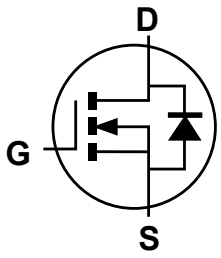
PowerDI5060-8



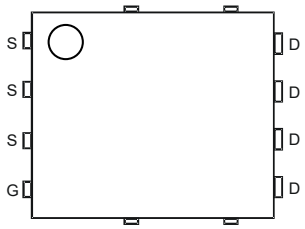
Top View



Bottom View



Internal Schematic



Top View
Pin Configuration

Ordering Information (Note 4)

Orderable Part Number	Package	Packing	
		Qty.	Carrier
DMTH10H015SPS-13	PowerDI5060-8	2,500	Tape & Reel

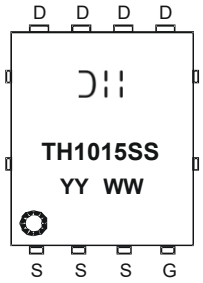
Notes:
1. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

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Marking Information

PowerDI5060-8



= Manufacturer's Marking
TH1015SS = Product Type Marking Code
YYWW = Date Code Marking
YY = Last Two Digits of Year (ex: 26 = 2026)
WW = Week Code (01 to 53)

Maximum Ratings (@ T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	100	V
Gate-Source Voltage			V_{GSS}	±20	V
Continuous Drain Current (Note 5) V_{GS} = 10V	Steady State	T_C = 25°C T_C = 100°C	I_D	56 39	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)			I_{DM}	120	A
Maximum Continuous Body Diode Forward Current (Note 5)			I_S	56	A
Avalanche Current (Note 7), L = 3mH			I_{AS}	7.5	A
Avalanche Energy (Note 7), L = 3mH			E_{AS}	85	mJ
Avalanche Current, L = 0.1mH			I_{AS}	15.8	A
Avalanche Energy, L = 0.1mH			E_{AS}	12.5	mJ

Thermal Characteristics

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 6)	T_A = 25°C	P_D	2.7	W
Thermal Resistance, Junction to Ambient (Note 6)		$R_{\theta JA}$	55	°C/W
Total Power Dissipation (Note 5)	T_C = 25°C	P_D	94	W
Thermal Resistance, Junction to Case (Note 5)		$R_{\theta JC}$	1.6	°C/W
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to 175	°C

Notes: 5. Thermal resistance from junction to soldering point (on the exposed drain pad).
6. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate.
7. Guaranteed by design. Not subject to product testing.

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Electrical Characteristics (@ T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV_{DSS}	100	—	—	V	V_{GS} = 0V, I_D = 1mA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	μA	V_{DS} = 80V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	$V_{GS(TH)}$	2	—	4	V	V_{DS} = V_{GS}, I_D = 250μA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	11.3	14.5	mΩ	V_{GS} = 10V, I_D = 20A
		—	14.7	19.5		V_{GS} = 6V, I_D = 20A
Diode Forward Voltage	V_{SD}	—	0.9	1.3	V	V_{GS} = 0V, I_S = 20A
DYNAMIC CHARACTERISTICS (Note 7)						
Input Capacitance	C_{iss}	—	2343	—	pF	V_{DS} = 50V, V_{GS} = 0V f = 1MHz
Output Capacitance	C_{oss}	—	487	—		
Reverse Transfer Capacitance	C_{rss}	—	26	—		
Gate Resistance	R_g	—	0.69	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge	Q_g	—	30.1	—	nC	V_{DD} = 50V, I_D = 10A, V_{GS} = 10V
Gate-Source Charge	Q_{gs}	—	7.5	—		
Gate-Drain Charge	Q_{gd}	—	6.5	—		
Turn-On Delay Time	$t_{D(ON)}$	—	9.8	—	ns	V_{DD} = 50V, V_{GS} = 10V, I_D = 10A, R_G = 6Ω
Turn-On Rise Time	t_R	—	7.8	—		
Turn-Off Delay Time	$t_{D(OFF)}$	—	22.5	—		
Turn-Off Fall Time	t_F	—	9.6	—		
Reverse-Recovery Time	t_{RR}	—	43.1	—	ns	I_F = 10A, di/dt = 100A/μs
Reverse-Recovery Charge	Q_{RR}	—	65.1	—	nC	

Notes: 7. Guaranteed by design. Not subject to product testing.
8. Short duration pulse test used to minimize self-heating effect.

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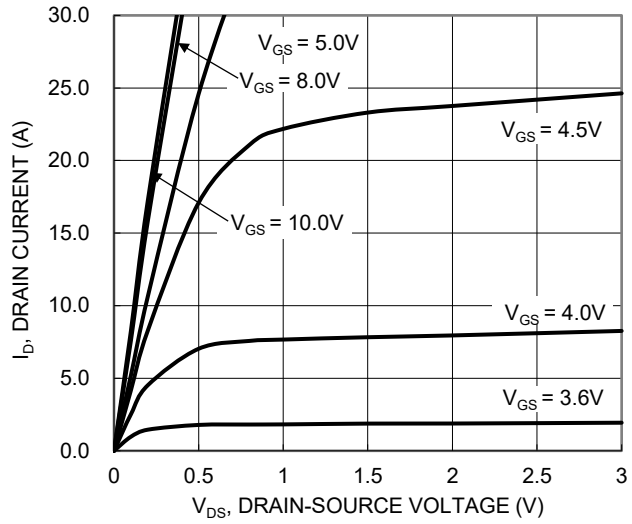


Figure 1. Typical Output Characteristic

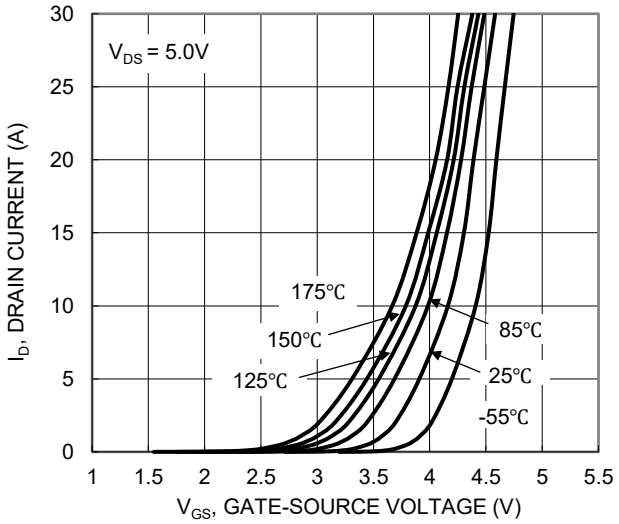


Figure 2. Typical Transfer Characteristic

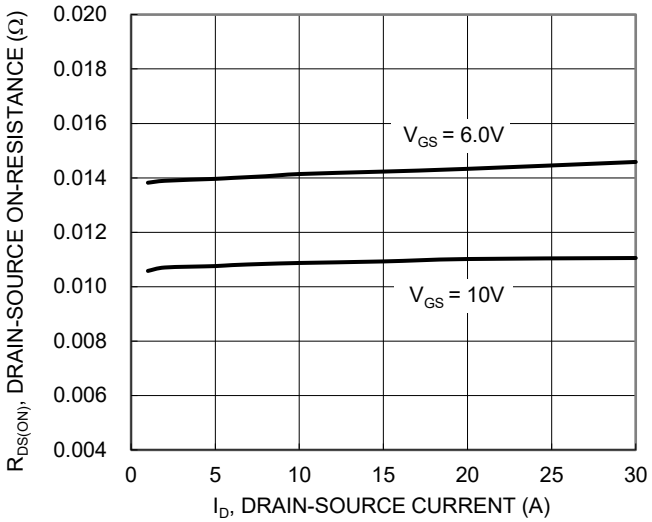


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

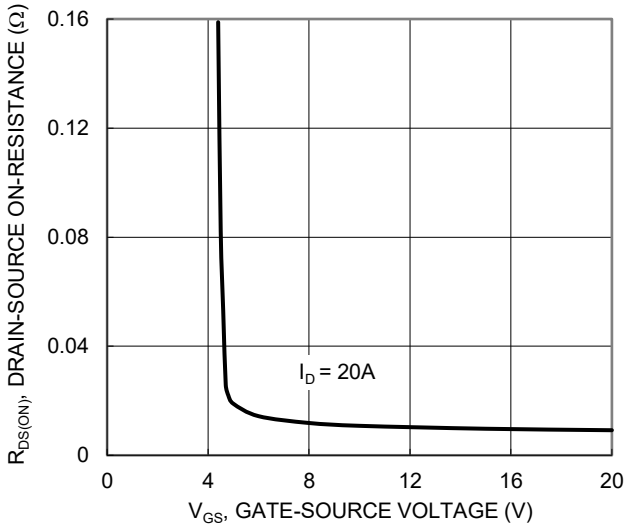


Figure 4. Typical Transfer Characteristic

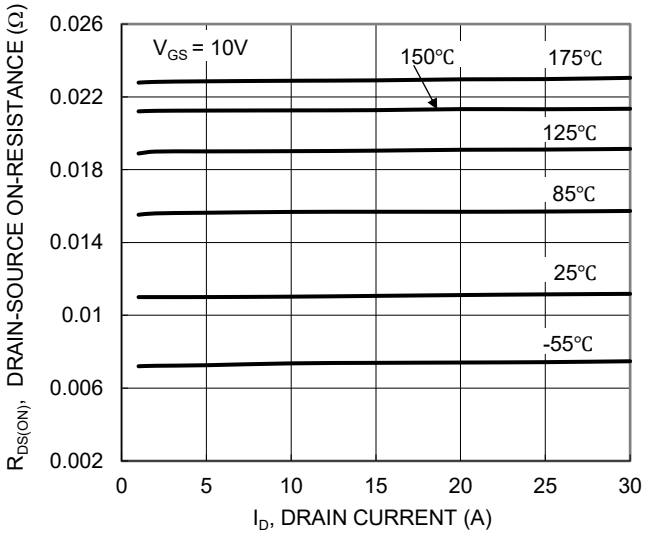


Figure 5. Typical On-Resistance vs. Drain Current and Temperature

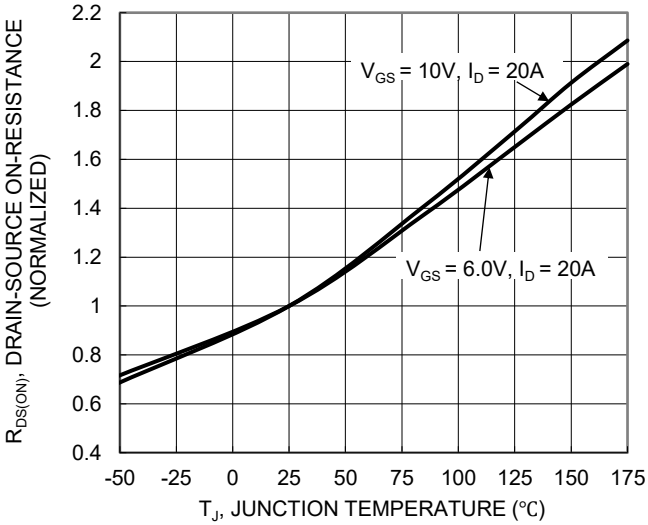


Figure 6. On-Resistance Variation with Temperature

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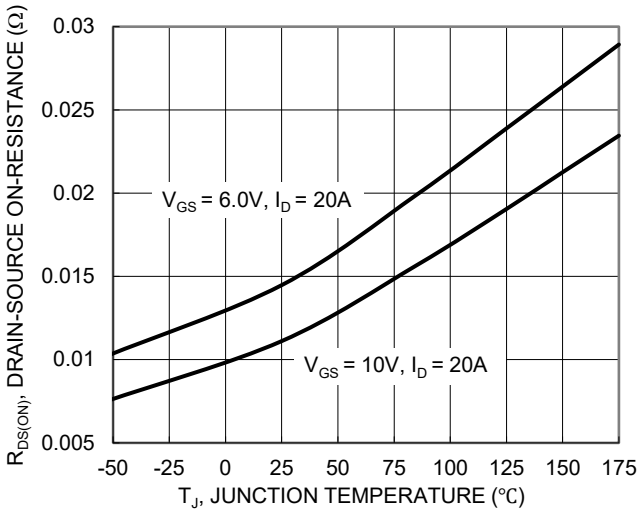


Figure 7. On-Resistance Variation with Temperature

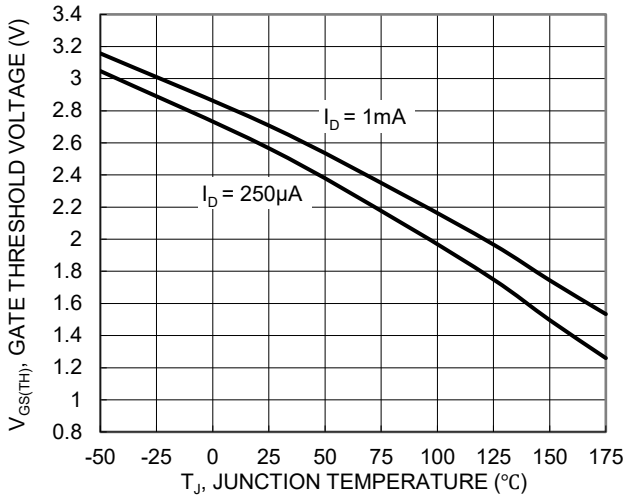


Figure 8. Gate Threshold Variation vs. Junction Temperature

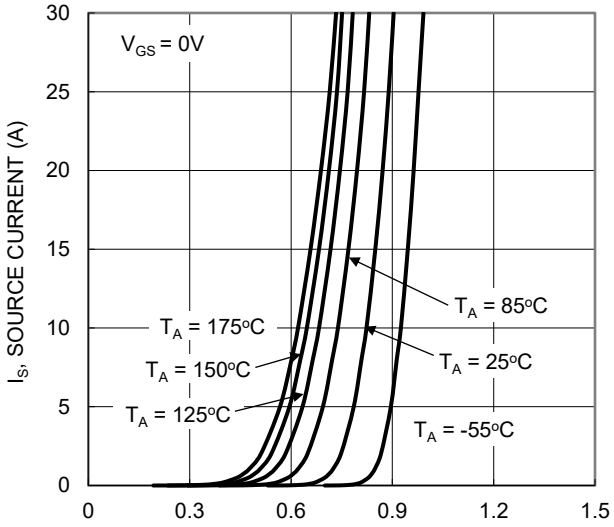


Figure 9. Diode Forward Voltage vs. Current

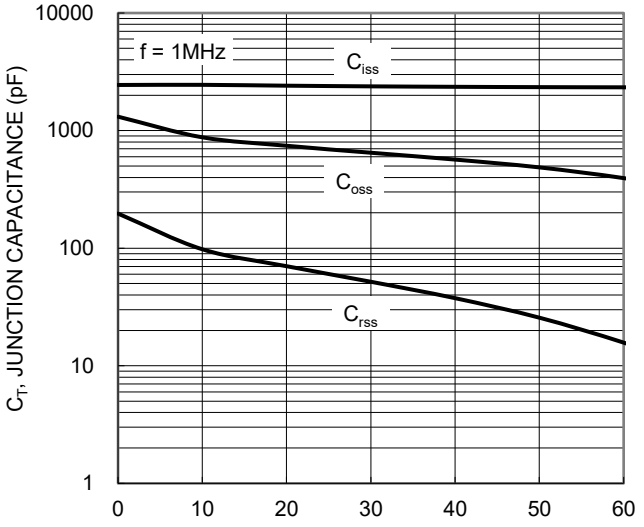


Figure 10. Typical Junction Capacitance

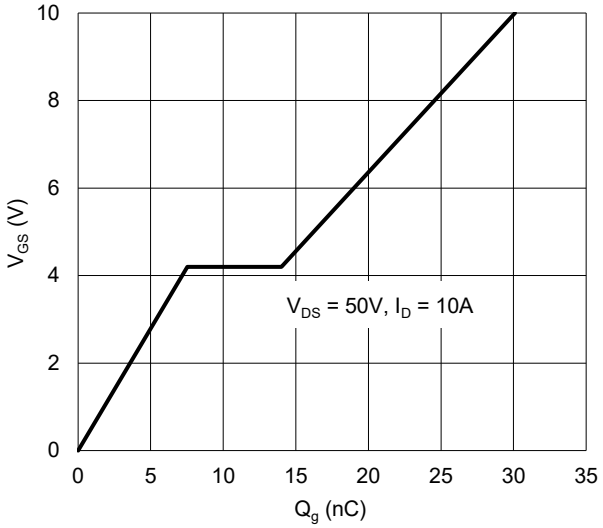


Figure 11. Gate Charge

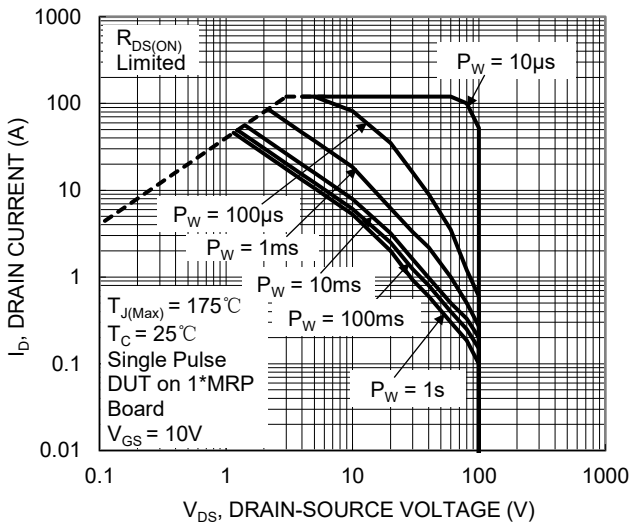


Figure 12. SOA, Safe Operation Area

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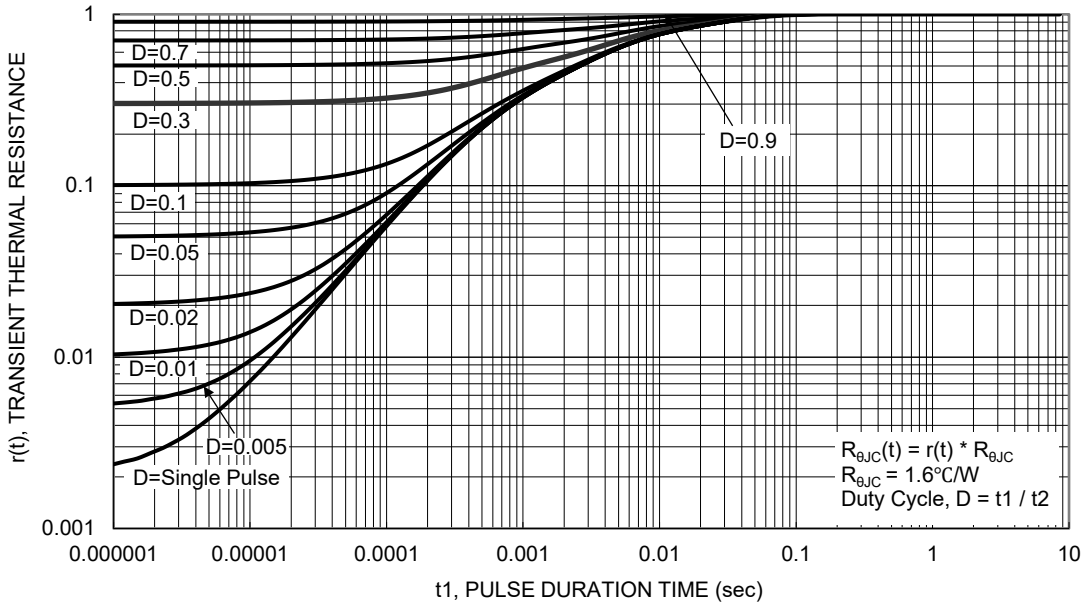


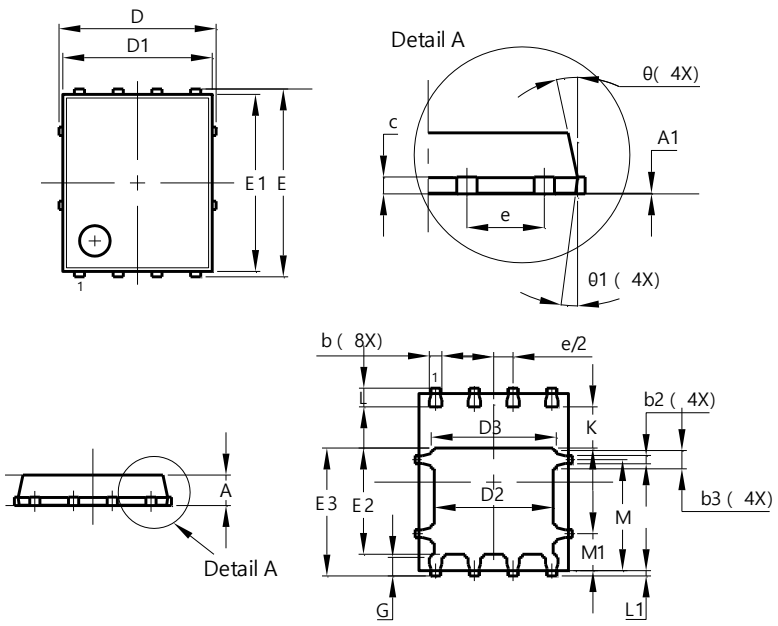
Figure 13. Transient Thermal Resistance

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Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

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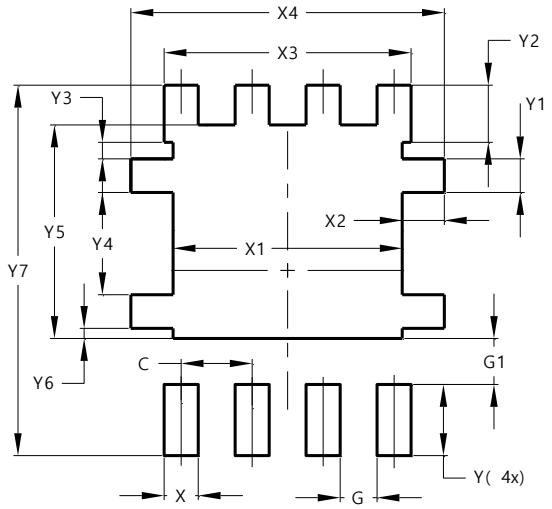


PowerDI5060-8			
Dim	**Min**	**Max**	**Typ**
A	0.90	1.10	1.00
A1	0.00	0.05	–
b	0.33	0.51	0.41
b2	0.200	0.350	0.273
b3	0.40	0.80	0.60
c	0.230	0.330	0.277
D	5.15 BSC		
D1	4.70	5.10	4.90
D2	3.70	4.10	3.90
D3	3.90	4.30	4.10
E	6.15 BSC		
E1	5.60	6.00	5.80
E2	3.28	3.68	3.48
E3	3.99	4.39	4.19
e	1.27 BSC		
G	0.51	0.71	0.61
K	0.51	–	–
L	0.51	0.71	0.61
L1	0.100	0.200	0.175
M	3.235	4.035	3.635
M1	1.00	1.40	1.21
Θ	10°	12°	11°
Θ1	6°	8°	7°
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI5060-8



Dimensions	Value (in mm)
C	1.270
G	0.660
G1	0.820
X	0.610
X1	4.100
X2	0.755
X3	4.420
X4	5.610
Y	1.270
Y1	0.600
Y2	1.020
Y3	0.295
Y4	1.825
Y5	3.810
Y6	0.180
Y7	6.610

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