100V +175°C N-CHANNEL ENHANCEMENT MODE MOSFET
PowerDI5060-8

Product Summary

BV_{DSS}	$R_{DS(ON)}$	I_D T_C = +25°C
100V	32mΩ @ V_{GS} = 10V	33A
	50mΩ @ V_{GS} = 4.5V	26A

Features

- 100% Unclamped Inductive Switching (UIS) Test in Production — Ensures More Reliable and Robust End Application
- High Conversion Efficiency
- Low Input Capacitance
- Fast Switching Speed
- Wettable Flank for Improved Optical Inspection
- **Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

Description and Applications

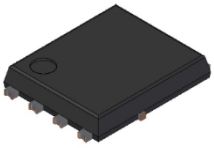
This MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$) yet maintain superior switching performance, making it ideal for high efficiency power management applications.

- Synchronous rectifiers
- Backlighting
- Power management functions
- DC-DC converters

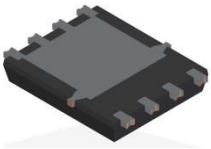
Mechanical Data

- Package: PowerDI®5060-8
- Package Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Finish — Matte Tin Annealed over Copper Leadframe; Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.097 grams (Approximate)

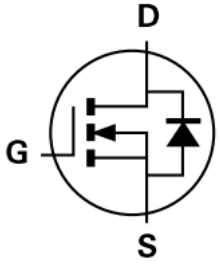
PowerDI5060-8 (SWP) (Type UX)



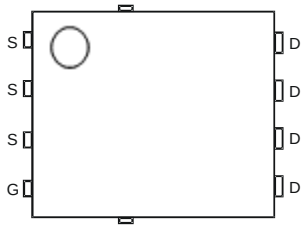
Top View



Bottom View



Internal Schematic



Top View
Pin Configuration

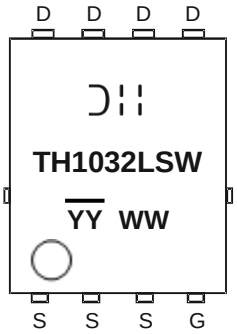
Ordering Information (Note 4)

Part Number	Package	Packing	
		Qty.	Carrier
DMTH10H032LPSW-13	PowerDI5060-8 (SWP) (Type UX)	2,500	Tape & Reel

Notes:
1. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

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Marking Information



= Manufacturer's Marking
TH1032LSW = Product Type Marking Code
YYWW = Date Code Marking
YY = Last Two Digits of Year (ex: 22 = 2022)
WW = Week Code (01 to 53)

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Drain-Source Voltage		V_{DSS}	100	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current, V_{GS} = 10V (Note 5)	T_C = +25°C T_C = +100°C	I_D	33 23	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)		I_{DM}	132	A
Maximum Continuous Body Diode Forward Current (Note 5)		I_S	33	A
Pulsed Body Diode Forward Current (10µs Pulse, Duty Cycle = 1%)		I_{SM}	132	A
Avalanche Current, L = 0.3mH (Note 6)		I_{AS}	13	A
Avalanche Energy, L = 0.3mH (Note 6)		E_{AS}	25.3	mJ

Thermal Characteristics

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 7)	T_A = +25°C	P_D	3.4	W
Thermal Resistance, Junction to Ambient (Note 7)		$R_{\theta JA}$	44	°C/W
Total Power Dissipation (Note 5)	T_C = +25°C	P_D	68	W
Thermal Resistance, Junction to Case (Note 5)		$R_{\theta JC}$	2.2	°C/W
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +175	°C

Notes: 5. Thermal resistance from junction to soldering point (on the exposed drain pad).
6. I_{AS} and E_{AS} ratings are based on low frequency and duty cycles to keep T_J = +25°C.
7. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate.

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Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV_{DSS}	100	—	—	V	V_{GS} = 0V, I_D = 1mA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	μA	V_{DS} = 80V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	$V_{GS(TH)}$	1.3	—	2.5	V	V_{DS} = V_{GS}, I_D = 250μA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	22	32	mΩ	V_{GS} = 10V, I_D = 5A
		—	32	50		V_{GS} = 4.5V, I_D = 4.5A
Diode Forward Voltage	V_{SD}	—	0.8	1	V	V_{GS} = 0V, I_S = 5A
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C_{iss}	—	683	—	pF	V_{DS} = 50V, V_{GS} = 0V f = 1MHz
Output Capacitance	C_{oss}	—	165	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	6.9	—	pF	
Gate Resistance	R_g	—	1.2	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge (V_{GS} = 4.5V)	Q_g	—	6.3	—	nC	V_{DS} = 50V, I_D = 6A
Total Gate Charge (V_{GS} = 10V)	Q_g	—	11.9	—	nC	
Gate-Source Charge	Q_{gs}	—	2.0	—	nC	
Gate-Drain Charge	Q_{gd}	—	3.1	—	nC	
Turn-On Delay Time	$t_{D(ON)}$	—	4.1	—	ns	V_{DS} = 50V, R_L = 5.85Ω V_{GS} = 10V, R_g = 3Ω
Turn-On Rise Time	t_R	—	4.5	—	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	12.5	—	ns	
Turn-Off Fall Time	t_F	—	9.3	—	ns	
Reverse Recovery Time	t_{RR}	—	31.5	—	ns	I_F = 6A, dI/dt = 500A/μs
Reverse Recovery Charge	Q_{RR}	—	94.6	—	nC	

Notes: 8. Short duration pulse test used to minimize self-heating effect.
9. Guaranteed by design. Not subject to product testing.

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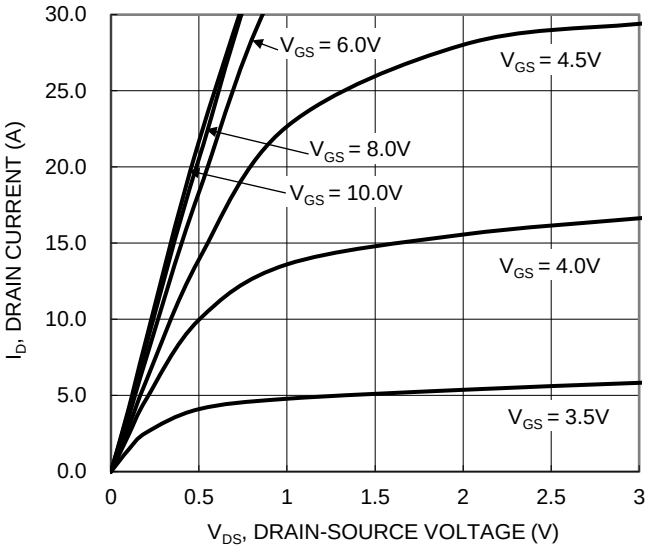


Figure 1. Typical Output Characteristic

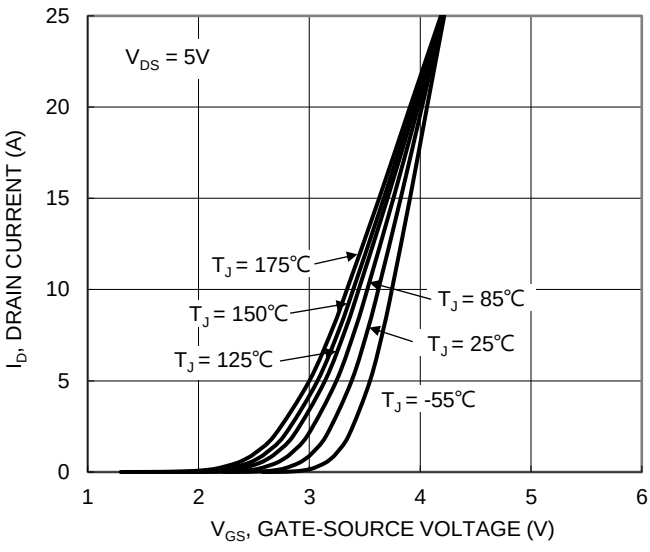


Figure 2. Typical Transfer Characteristic

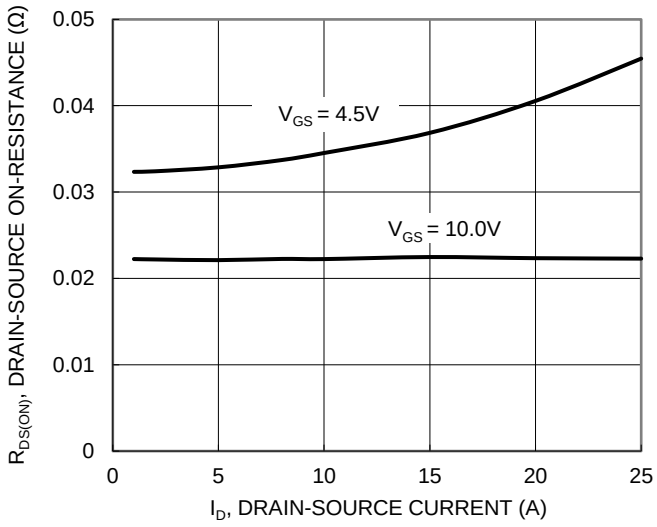


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

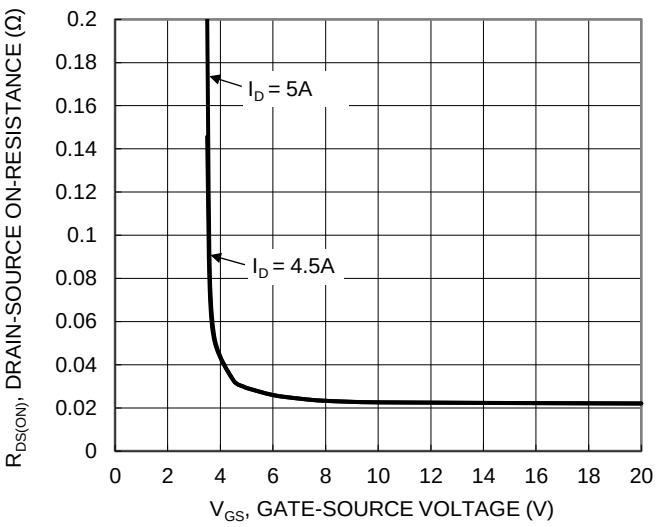


Figure 4. Typical Transfer Characteristic

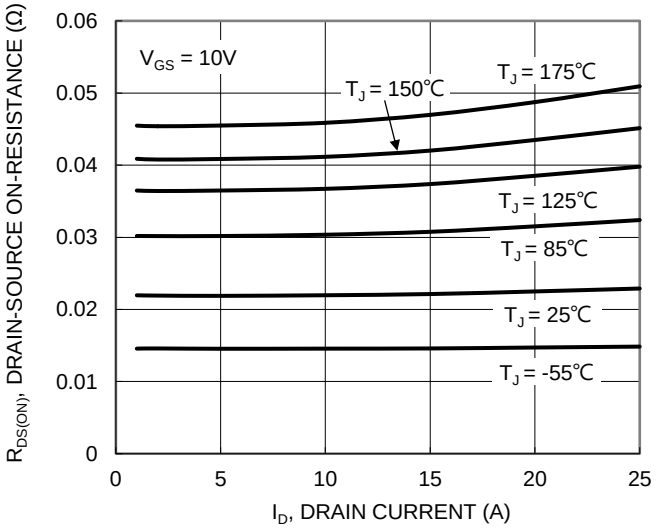


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

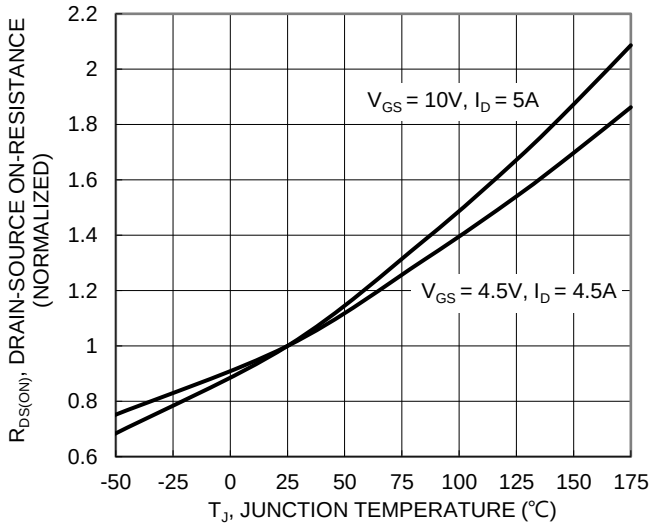


Figure 6. On-Resistance Variation with Junction Temperature

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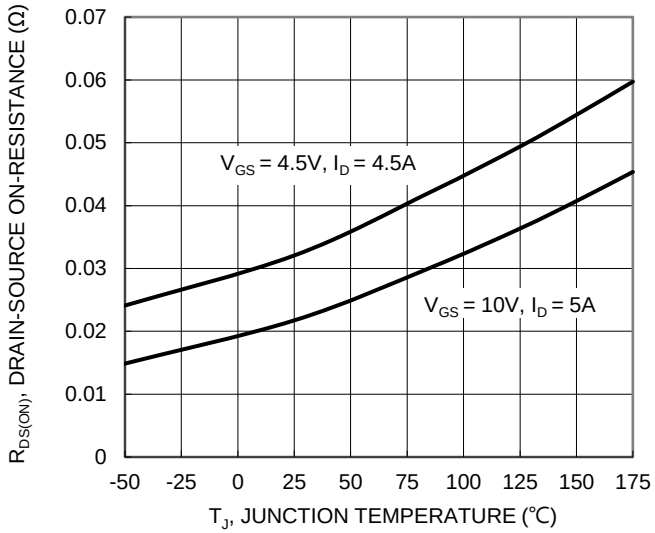


Figure 7. On-Resistance Variation with Junction Temperature

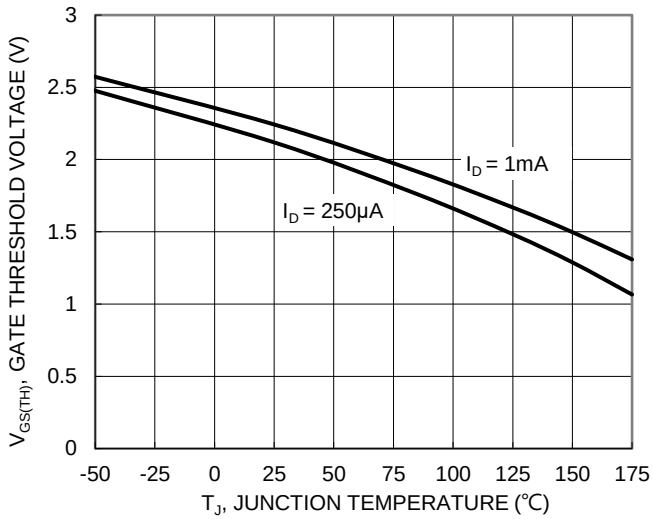


Figure 8. Gate Threshold Variation vs. Junction Temperature

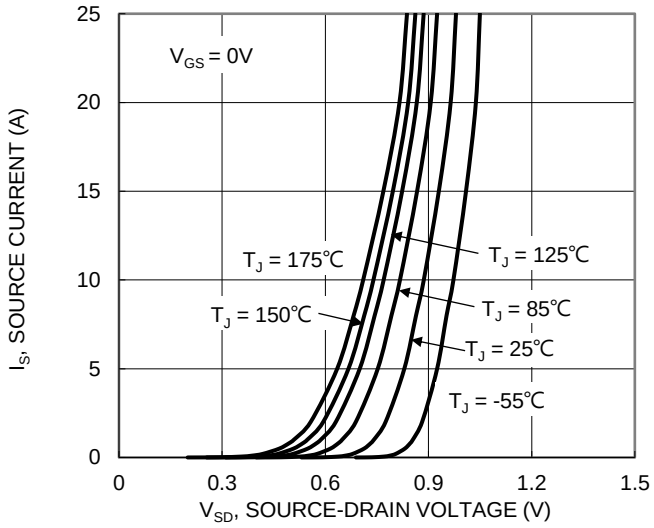


Figure 9. Diode Forward Voltage vs. Current

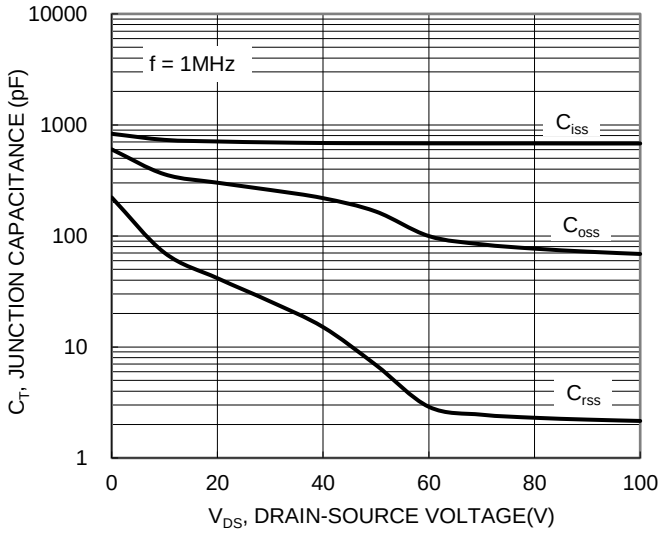


Figure 10. Typical Junction Capacitance

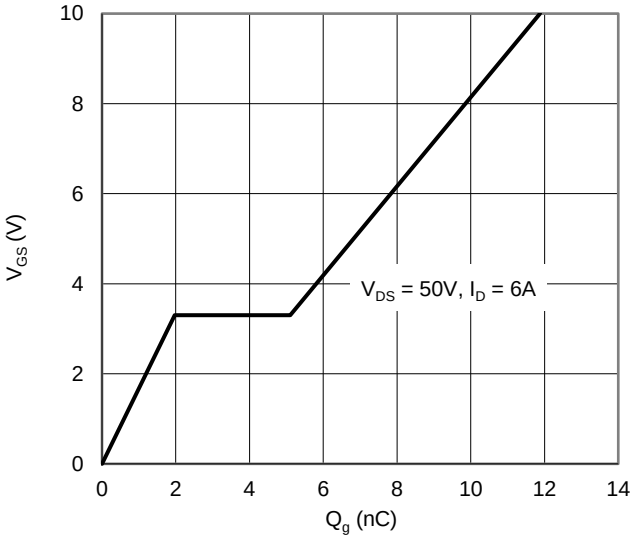


Figure 11. Gate Charge

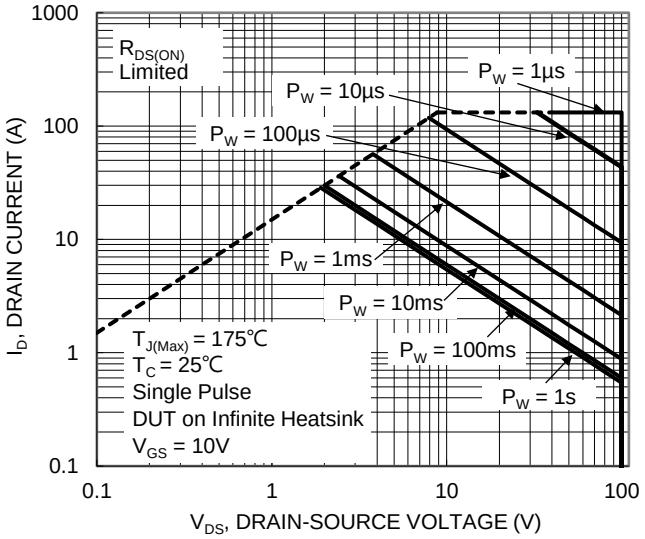


Figure 12. SOA, Safe Operation Area

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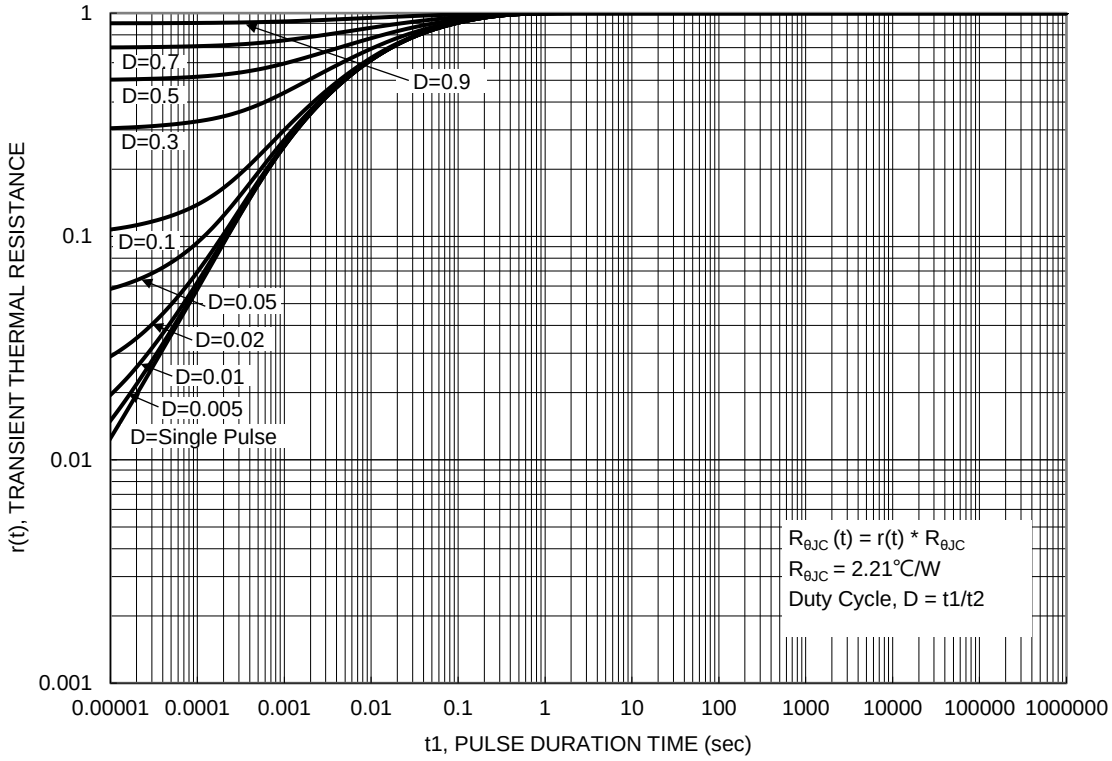


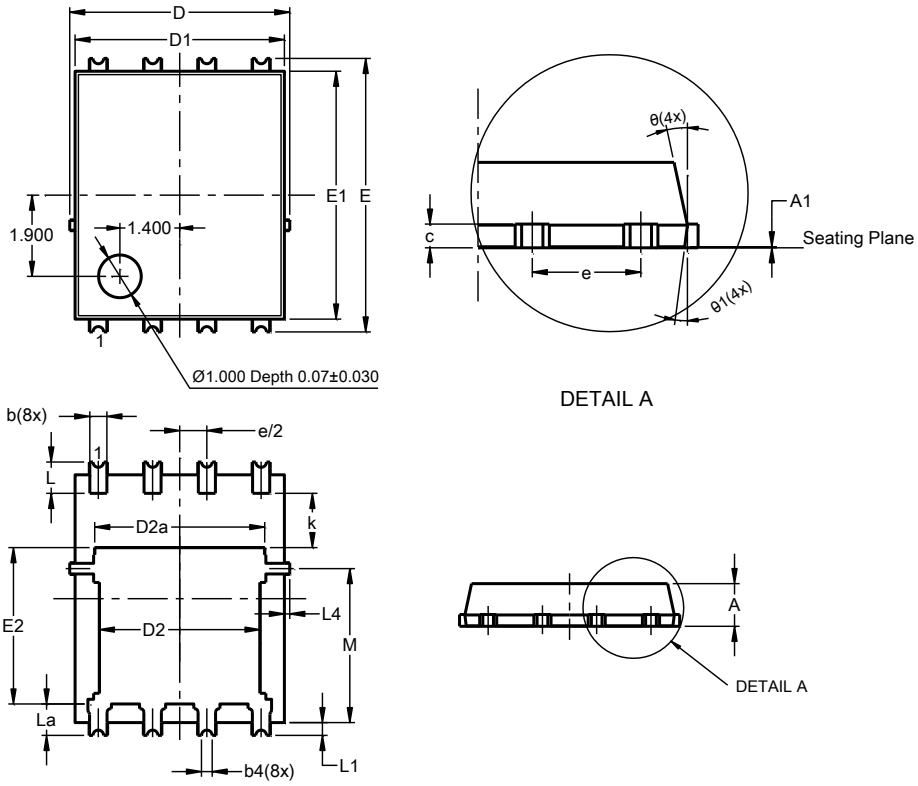
Figure 13. Transient Thermal Resistance

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Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI5060-8 (SWP) (Type UX)

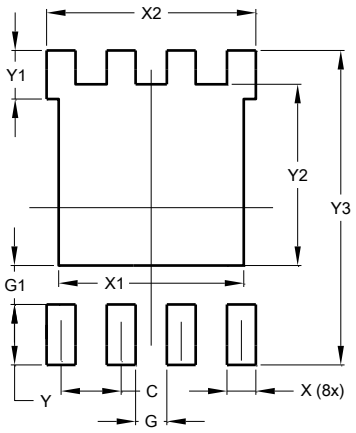


PowerDI5060-8 (SWP) (Type UX)			
Dim	**Min**	**Max**	**Typ**
A	0.90	1.10	1.00
A1	0	0.05	--
b	0.30	0.50	0.41
b2	0.20	0.35	0.25
b4	0.25REF		
c	0.230	0.330	0.277
D	5.15 BSC		
D1	4.70	5.10	4.90
D2	3.56	3.96	3.76
D2a	3.78	4.18	3.98
E	6.40 BSC		
E1	5.60	6.00	5.80
E2	3.46	3.86	3.66
E2a	4.195	4.595	4.395
e	1.27BSC		
k	1.05	--	--
L	0.635	0.835	0.735
La	0.635	0.835	0.735
L1	0.200	0.400	0.300
L1a	0.050REF		
L4	0.025	0.225	0.125
M	3.205	4.005	3.605
θ	10°	12°	11°
θ1	6°	8°	7°
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI5060-8 (SWP) (Type UX)



Dimensions	Value (in mm)
C	1.270
G	0.660
G1	0.820
X	0.610
X1	4.100
X2	4.420
Y	1.270
Y1	1.020
Y2	3.810
Y3	6.610

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