General Description

The DS1340 is a real-time clock (RTC)/calendar that is pin compatible and functionally equivalent to the ST M41T00, including the software clock calibration. The device additionally provides trickle-charge capability on the V_{BACKUP} pin, a lower timekeeping voltage, and an oscillator STOP flag. Block access of the register map is identical to the ST device. Two additional registers, which are accessed individually, are required for the trickle charger and flag. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. A built-in power-sense circuit detects power failures and automatically switches to the backup supply. Reads and writes are inhibited while the clock continues to run. The device is programmed serially through an I²C bidirectional bus.

Applications

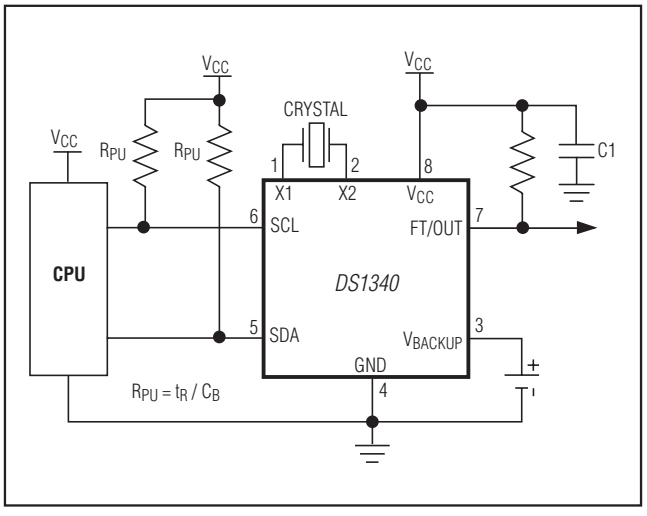
Portable Instruments

Point-of-Sale Equipment

Medical Equipment

Telecommunications

Typical Operating Circuit



Pin Configurations appear at end of data sheet.

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Benefits and Features

- Enhanced Second Source for the ST M41T00
- Completely Manages All Timekeeping Functions
  - RTC Counts Seconds, Minutes, Hours, Day, Date, Month, and Year
  - Software Clock Calibration
  - Oscillator Stop Flag
- Low-Power Operation Extends Battery Backup Run Time
  - Low Timekeeping Voltage Down to 1.3V
  - Automatic Power-Fail Detect and Switch Circuitry
  - Trickle-Charge Capability
- Three Operating Voltage Ranges (1.8V, 3V, and 3.3V) Supports Systems Using Legacy and Modern Power Buses
- Surface-Mount Package with an Integrated Crystal (DS1340C) Saves Additional Space and Simplifies Design
- Simple Serial Port Interfaces with Most Microcontrollers
  - Fast (400kHz) I²C Interface
- 8-Pin µSOP or SO Package Minimizes Required Space
- Underwriters Laboratories (UL®) Recognized

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK†
DS1340Z-18+	-40°C to +85°C	8 SO (0.150in)	D1340-18
DS1340Z-3+	-40°C to +85°C	8 SO (0.150in)	DS1340-3
DS1340Z-33+	-40°C to +85°C	8 SO (0.150in)	D134033
DS1340U-18+	-40°C to +85°C	8 µSOP	1340 -18
DS1340U-3+	-40°C to +85°C	8 µSOP	1340 -3
DS1340U-33+	-40°C to +85°C	8 µSOP	1340 -33
DS1340C-18#	-40°C to +85°C	16 SO	DS1340C-18
DS1340C-3#	-40°C to +85°C	16 SO	DS1340C-3
DS1340C-33#	-40°C to +85°C	16 SO	DS1340C-33

+Denotes a lead(Pb)-free/RoHS-compliant package.

#Denotes a RoHS-compliant device that may include lead(Pb) that is exempt under RoHS requirements. The lead finish is JESD97 category e3, and is compatible with both lead-based and lead-free soldering processes.

†A "+" anywhere on the top mark denotes a lead(Pb)-free device. A "#" denotes a RoHS-compliant device.

maxim integrated™

Absolute Maximum Ratings

Voltage Range on V_{CC} or V_{BACKUP} Pins
Relative to Ground.....-0.3V to +6.0V
Voltage Range on SDA, SCL, and FT/OUT
Relative to Ground.....-0.3V to (V_{CC} + 0.3V)

Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-55°C to +125°C
Lead Temperature (soldering, 10s) .....+260°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions

(V_{CC} = $V_{CC\ MIN}$ to $V_{CC\ MAX}$, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage (Note 2)	V_{CC}	DS1340-18	1.71	1.8	5.5	V
		DS1340-3	2.7	3.0	5.5	
		DS1340-33	2.97	3.3	5.5	
Input Logic 1 (SDA, SCL)	V_{IH}	(Note 2)	0.7 x V_{CC}		V_{CC} + 0.3	V
Input Logic 0 (SDA, SCL)	V_{IL}	(Note 2)	-0.3		+0.3 x V_{CC}	V
Supply Voltage, Pullup (FT/OUT, SDA, SCL), V_{CC} = 0V	V_{PU}	(Note 2)			5.5	V
Backup Supply Voltage (Note 2)	V_{BACKUP}	DS1340-18	1.3		3.7	V
		DS1340-3	1.3		3.7	
		DS1340-33	1.3		5.5	
Trickle-Charge Current-Limiting Resistors	R1	(Notes 3, 4)		250		Ω
	R2	(Note 5)		2000		
	R3	(Note 6)		4000		
Power-Fail Voltage (Note 2)	V_{PF}	DS1340-18	1.51	1.6	1.71	V
		DS1340-3	2.45	2.6	2.7	
		DS1340-33	2.70	2.88	2.97	
Input Leakage (SCL, CLK)	I_{LI}		-1		+1	µA
I/O Leakage (SDA, FT/OUT)	I_{LO}		-1		+1	µA
SDA Logic 0 Output	I_{OLSDA}	V_{CC} > 2V; V_{OL} = 0.4V			3.0	mA
		1.7V < V_{CC} < 2V; V_{OL} = 0.2 x V_{CC}			3.0	
FT/OUT Logic 0 Output	I_{OLSQW}	V_{CC} > 2V; V_{OL} = 0.4V			3.0	mA
		1.7V < V_{CC} < 2V; V_{OL} = 0.2 x V_{CC}			3.0	
		1.3V < V_{CC} < 1.7V; V_{OL} = 0.2x V_{CC}			250	µA
Active Supply Current (Note 7)	I_{CCA}	DS1340-18; V_{CC} = 1.89V		72	150	µA
		DS1340-3; V_{CC} = 3.3V		108	200	
		DS1340-33; V_{CC} = 5.5V		192	300	
Standby Current (Note 8)	I_{CCS}	DS1340-18; V_{CC} = 1.89V		60	100	µA
		DS1340-3; V_{CC} = 3.3V		81	125	
		DS1340-33; V_{CC} = 5.5V		100	150	
V_{BACKUP} Leakage Current	$I_{BACKUPLKG}$	V_{BACKUP} = 3.7V			100	nA

DC Electrical Characteristics

(V_{CC} = 0V, V_{BACKUP} = 3.7V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{BACKUP} Current	$I_{BACKUP1}$	OSC ON, FT = 0 (Note 9)		800	1150	nA
	$I_{BACKUP2}$	OSC ON, FT = 1 (Note 9)		850	1250	
	$I_{BACKUP3}$	OSC ON, FT = 0, V_{BACKUP} = 3.0V, T_A = +25°C (Notes 9, 10)		800	1000	
V_{BACKUP} Data-Retention Current	$I_{BACKUPDR}$	OSC OFF		25.0	100	nA

AC Electrical Characteristics

(V_{CC} = $V_{CC\ MIN}$ to $V_{CC\ MAX}$, T_A = -40°C to +85°C, unless otherwise noted.) (Notes 1,14, Figure 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	Standard mode	0		100	kHz
		Fast mode	100		400	
Bus Free Time Between STOP and START Conditions	t_{BUF}	Standard mode	4.7			µs
		Fast mode	1.3			
Hold Time (Repeated) START Condition (Note 11)	$t_{HD:STA}$	Standard mode	4.0			µs
		Fast mode	0.6			
Low Period of SCL Clock	t_{LOW}	Standard mode	4.7			µs
		Fast mode	1.3			
High Period of SCL Clock	t_{HIGH}	Standard mode	4.0			µs
		Fast mode	0.6			
Data Hold Time (Notes 12, 13)	$t_{HD:DAT}$	Standard mode	0		0.9	µs
		Fast mode	0		0.9	
Data Setup Time (Note 14)	$t_{SU:DAT}$	Standard mode	250			ns
		Fast mode	100			
START Setup Time	$t_{SU:STA}$	Standard mode	4.7			µs
		Fast mode	0.6			
Rise Time of SDA and SCL Signals (Note 15)	t_R	Standard mode	$20 + 0.1C_B$		1000	ns
		Fast mode	$20 + 0.1C_B$		300	
Fall Time of SDA and SCL Signals (Note 15)	t_F	Standard mode	$20 + 0.1C_B$		300	ns
		Fast mode	$20 + 0.1C_B$		300	
Setup Time for STOP Condition	$t_{SU:STO}$	Standard mode	4.7			µs
		Fast mode	0.6			
Capacitive Load for Each Bus Line	C_B	(Note 15)			400	pF
I/O Capacitance (SCL, SDA)	$C_{I/O}$			10		pF
Pulse Width of Spikes that Must be Suppressed by the Input Filter	t_{SP}	Fast mode		30		ns
Oscillator Stop Flag (OSF) Delay	t_{OSF}	(Note 16)		100		ms

Power-Up/Power-Down Characteristics

(T_A = -40°C to +85°C) (Figure 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Recovery at Power-Up	t_{REC}	(Note 17)			2	ms
V_{CC} Fall Time; $V_{PF(MAX)}$ to $V_{PF(MIN)}$	t_{VCCF}		300			µs
V_{CC} Rise Time; $V_{PF(MIN)}$ to $V_{PF(MAX)}$	t_{VCCR}		0			µs

WARNING: Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery-backup mode.

Note 1: Limits at -40°C are guaranteed by design and not production tested.
Note 2: All voltages are referenced to ground.
Note 3: Measured at V_{CC} = typ, V_{BACKUP} = 0V, register 08h = A5h.
Note 4: The use of the 250Ω trickle-charge resistor is not allowed at V_{CC} > 3.63V and should not be enabled.
Note 5: Measured at V_{CC} = typ, V_{BACKUP} = 0V, register 08h = A6h.
Note 6: Measured at V_{CC} = typ, V_{BACKUP} = 0V, register 08h = A7h.
Note 7: I_{CCA}—SCL clocking at max frequency = 400kHz.
Note 8: Specified with I²C bus inactive.
Note 9: Measured with a 32.768kHz crystal attached to the X1 and X2 pins.
Note 10: Limits at +25°C are guaranteed by design and not production tested.
Note 11: After this period, the first clock pulse is generated.
Note 12: A device must internally provide a hold time of at least 300ns for the SDA signal (referred to as the $V_{IH(MIN)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.
Note 13: The maximum $t_{HD:DAT}$ only has to be met if the device does not stretch the low period (t_{LOW}) of the SCL signal.
Note 14: A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT}$ ≥ to 250ns must be met. This is automatically the case if the device does not stretch the low period of the SCL signal. If such a device does stretch the low period of the SCL signal, it must output the next data bit to the SDA line $t_{R\ MAX}$ + $t_{SU:DAT}$ = 1000 + 250 = 1250ns before the SCL line is released.
Note 15: C_B—total capacitance of one bus line in pF.
Note 16: The parameter t_{OSF} is the period of time the oscillator must be stopped for the OSF flag to be set over the 0V ≤ V_{CC} ≤ V_{CCMAX} and 1.3V ≤ V_{BAT} ≤3.7V range.
Note 17: This delay applies only if the oscillator is enabled and running. If the oscillator is disabled or stopped, no power-up delay occurs.

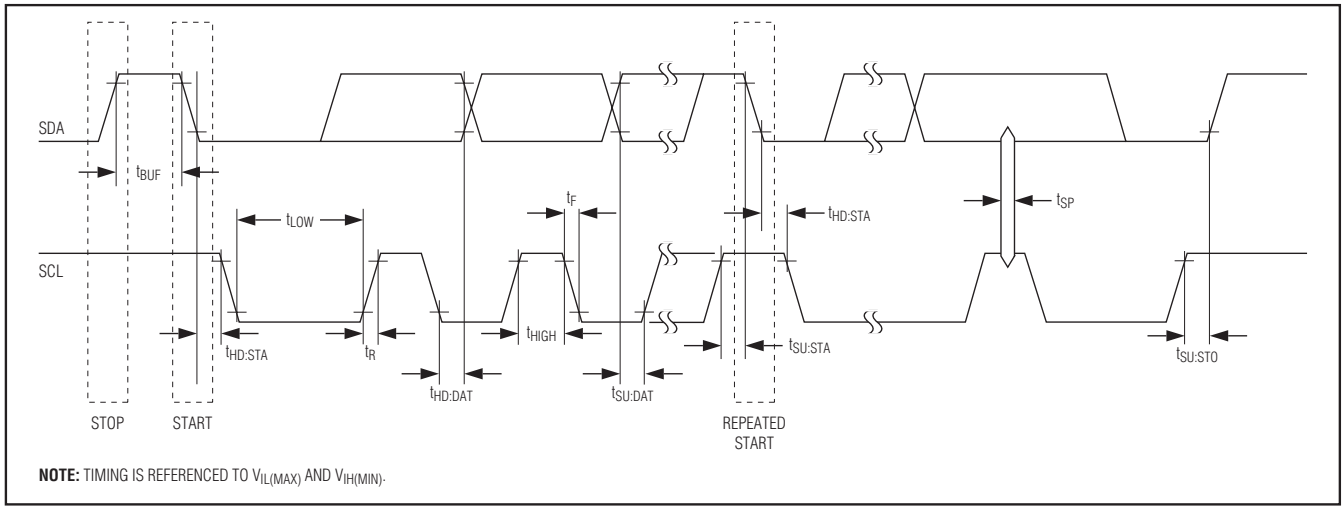


Figure 1. Data Transfer on I²C Serial Bus

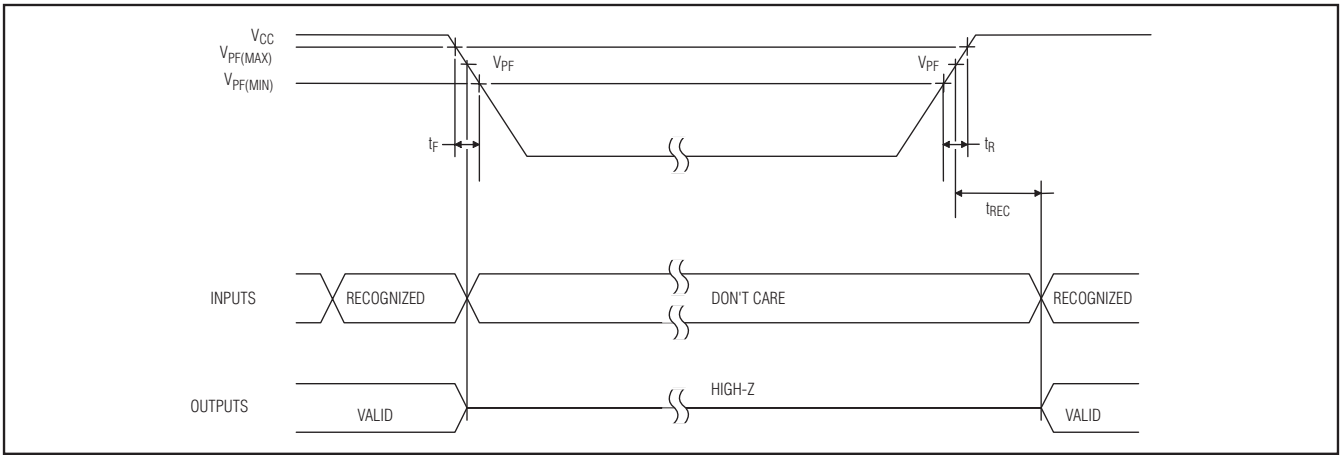
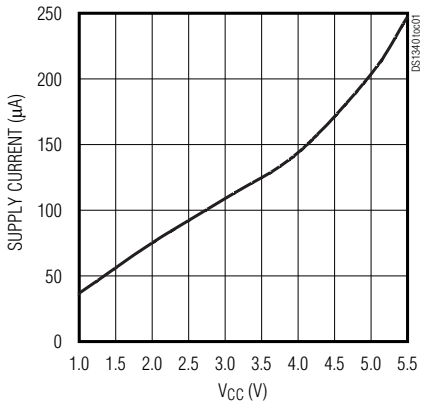


Figure 2. Power-Up/Power-Down Timing

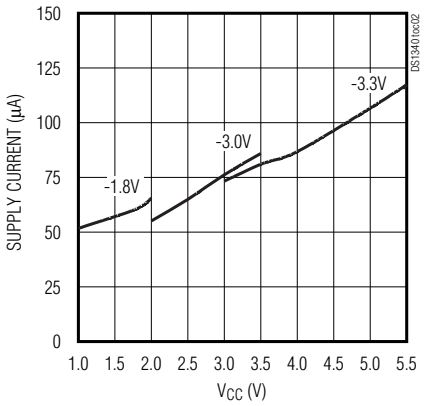
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

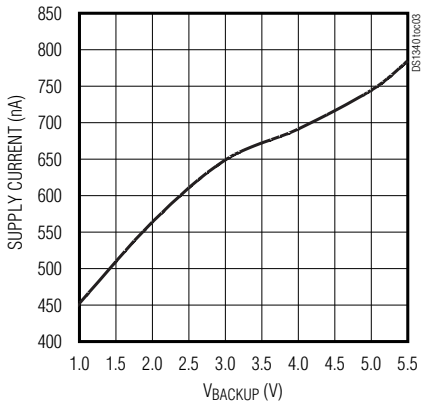
I_{CCSA} vs. V_{CC} FT = 0



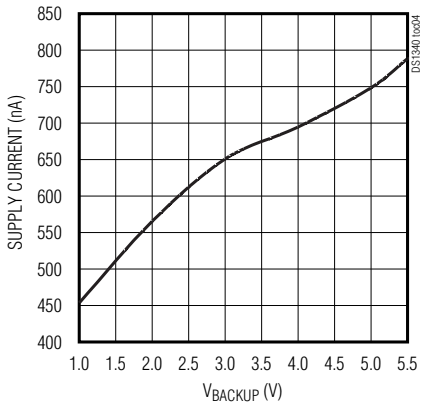
I_{CCS} vs. V_{CC} FT = 0



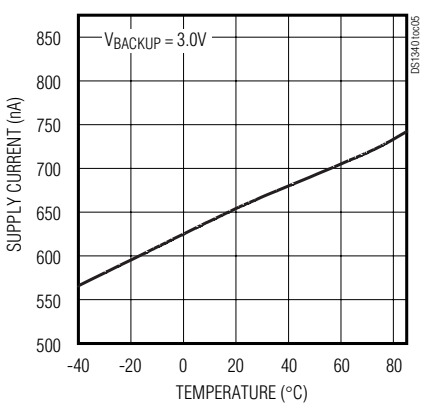
$I_{BACKUP1}$ (FT = 0) vs. V_{BACKUP}



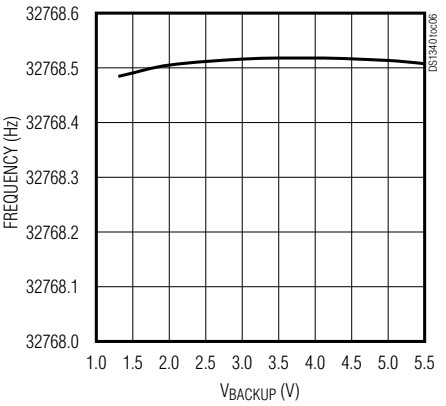
$I_{BACKUP2}$ (FT = 1) vs. V_{BACKUP}



$I_{BACKUP3}$ vs. TEMPERATURE



OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE (FT x 64)



Pin Description

PIN		NAME	FUNCTION
8	16		
1	—	X1	Connections for a Standard 32.768kHz Quartz Crystal. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (C_L) of 12.5pF. X1 is the input to the oscillator and can optionally be connected to an external 32.768kHz oscillator. The output of the internal oscillator, X2, is left unconnected if an external oscillator is connected to X1.
2	—	X2	
3	14	V_{BACKUP}	Connection for a Secondary Power Supply. For the 1.8V and 3V devices, V_{BACKUP} must be held between 1.3V and 3.7V for proper operation. Diodes placed in series between the supply and the input pin may result in improper operation. V_{BACKUP} can be as high as 5.5V on the 3.3V device. This pin can be connected to a primary cell such as a lithium coin cell. Additionally, this pin can be connected to a rechargeable cell or a super cap when used with the trickle-charge feature. UL recognized to ensure against reverse charging when used with a lithium battery (**www.maximintegrated.com/qa/info/ul**).
4	15	GND	Ground
5	16	SDA	Serial Data Input/Output. SDA is the data input/output for the I2C serial interface. The SDA pin is open drain and requires an external pullup resistor.
6	1	SCL	Serial Clock Input. SCL is the clock input for the I2C interface and is used to synchronize data movement on the serial interface.
7	2	FT/OUT	Frequency Test/Output. This pin is used to output either a 512Hz signal or the value of the OUT bit. When the FT bit is logic 1, the FT/OUT pin toggles at a 512Hz rate. When the FT bit is logic 0, the FT/OUT pin reflects the value of the OUT bit. This open-drain pin requires an external pullup resistor, and operates with either V_{CC} or V_{BACKUP} applied. The pullup voltage can be up to 5.5V, regardless of the voltage on V_{CC}. If not used, this pin can be left unconnected.
8	3	V_{CC}	Primary Power Supply. When voltage is applied within normal limits, the device is fully accessible and data can be written and read. When a backup supply is connected to the device and V_{CC} is below V_{PF}, reads and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage.
—	4–13	N.C.	No Connection. Must be connected to ground.

Detailed Description

The DS1340 is a low-power clock/calendar with a trickle charger. Address and data are transferred serially through a I2C bidirectional bus. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The DS1340 has a built-in power-sense circuit that detects power failures and automatically switches to the backup supply.

Power Control

The power-control function is provided by a precise, temperature-compensated voltage reference and a comparator circuit that monitors the V_{CC} level. The device is fully accessible and data can be written and read when V_{CC} is greater than V_{PF}. However, when V_{CC} falls below V_{PF}, the internal clock registers are blocked from any access. If V_{PF} is less than V_{BACKUP}, the device power is switched from V_{CC} to V_{BACKUP} when V_{CC} drops below V_{PF}. If V_{PF} is greater than V_{BACKUP}, the device power is switched from V_{CC} to V_{BACKUP}

Table 1. Power Control

SUPPLY CONDITION	READ/WRITE ACCESS	POWERED BY
$V_{CC} < V_{PF}$, $V_{CC} < V_{BACKUP}$	No	V_{BAT}
$V_{CC} < V_{PF}$, $V_{CC} > V_{BACKUP}$	No	V_{CC}
$V_{CC} > V_{PF}$, $V_{CC} < V_{BACKUP}$	Yes	V_{CC}
$V_{CC} > V_{PF}$, $V_{CC} > V_{BACKUP}$	Yes	V_{CC}

when V_{CC} drops below V_{BACKUP}. The registers are maintained from the V_{BACKUP} source until V_{CC} is returned to nominal levels (Table 1). After V_{CC} returns above V_{PF}, read and write access is allowed t_{REC}.

Oscillator Circuit

The DS1340 uses an external 32.768kHz crystal. The oscillator circuit does not require any external resistors or capacitors to operate. Table 2 specifies several crystal parameters for the external crystal. Figure 3 shows a functional schematic of the oscillator circuit. If using a crystal with the specified characteristics, the startup time is usually less than one second.

Clock Accuracy

The initial clock accuracy depends on the accuracy of the crystal and the accuracy of the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Additional error is added by crystal frequency drift caused by temperature shifts. External circuit noise coupled into the oscillator circuit can result in the clock running fast. Figure 4 shows a typical PC board layout for isolating the crystal and oscillator from noise. Refer to *Application Note 58: Crystal Considerations with Dallas Real-Time Clocks* (**www.maximintegrated.com/RTCapps**) for detailed information.

Table 2. Crystal Specifications*

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Nominal Frequency	f_O		32.768		kHz
Series Resistance	ESR			80	kΩ
Load Capacitance	C_L		12.5		pF

**The crystal, traces, and crystal input pins should be isolated from RF generating signals. Refer to* Application Note 58: Crystal Considerations for Dallas Real-Time Clocks *for additional specifications.*

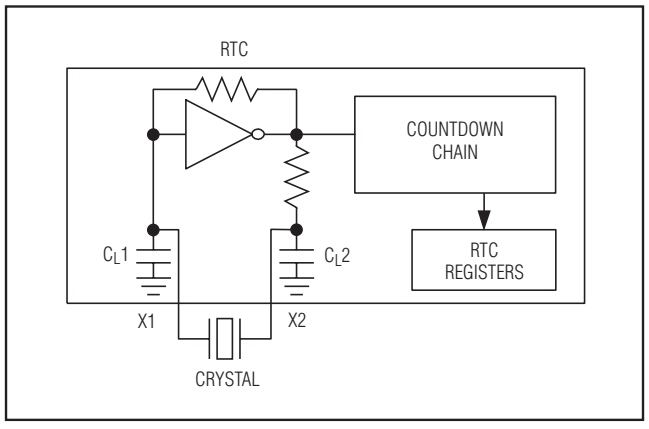


Figure 3. Oscillator Circuit Showing Internal Bias Network

DS1340C Only

The DS1340C integrates a standard 32,768Hz crystal into the package. Typical accuracy with nominal V_{CC} and +25°C is approximately +15ppm. Refer to Application Note 58 for information about crystal accuracy vs. temperature.

Operation

The DS1340 operates as a slave device on the serial bus. Access is obtained by implementing a START condition and providing a device identification code followed by data. Subsequent registers can be accessed sequentially until a STOP condition is executed. The device is fully accessible and data can be written and read when V_{CC} is greater than V_{PF}. However, when V_{CC} falls below V_{PF}, the internal clock registers are blocked from any access. If V_{PF} is less than V_{BACKUP}, the device power is switched from V_{CC} to V_{BACKUP} when V_{CC} drops below V_{PF}. If V_{PF} is greater than V_{BACKUP}, the device power is switched from V_{CC} to V_{BACKUP} when V_{CC} drops below V_{BACKUP}. The registers are maintained from the V_{BACKUP} source until V_{CC} is returned to nominal levels. The functional diagram (Figure 5) shows the main elements of the serial RTC.

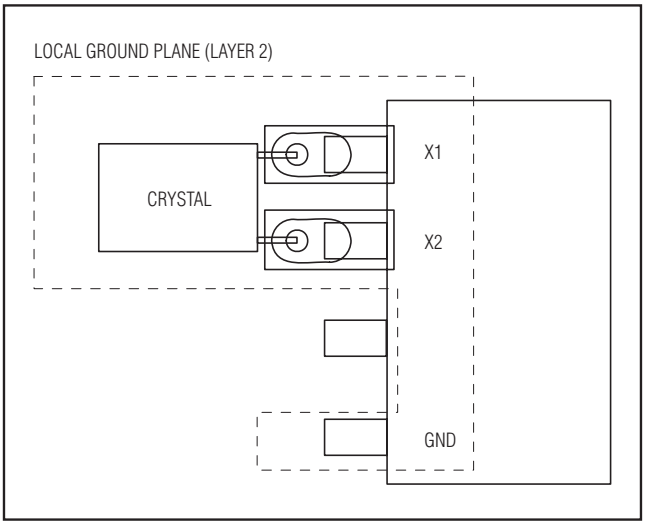


Figure 4. Layout Example

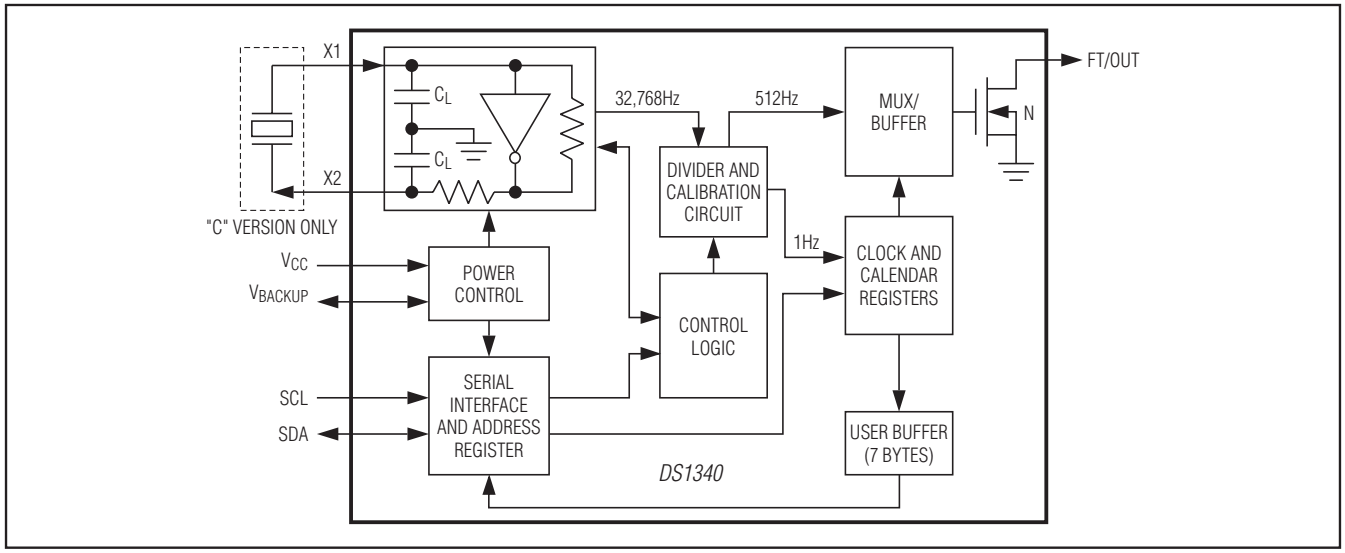


Figure 5. Functional Diagram

Address Map

Table 3 shows the DS1340 address map. The RTC registers are located in address locations 00h to 06h, and the control register is located at 07h. The trickle-charge and flag registers are located in address locations 08h to 09h. During a multibyte access of the timekeeping registers, when the address pointer reaches 07h—the end of the clock and control register space—it wraps around to location 00h. Writing the address pointer to the corresponding location accesses address locations 08h and 09h. After accessing location 09h, the address pointer wraps around to location 00h. On a I²C START, STOP, or address pointer incrementing to location 00h, the current time is transferred to a second set of registers. The time information is read from these secondary registers, while the clock may continue to run. This eliminates the need to reread the registers in case the main registers update during a read.

Clock and Calendar

The time and calendar information is obtained by reading the appropriate register bytes. Table 3 shows the RTC registers. The time and calendar data are set or initialized by writing the appropriate register bytes. The contents of the time and calendar registers are in the binary-coded decimal (BCD) format. The day-of-week

Table 3. Address Map

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FUNCTION	RANGE
00H	$\overline{EOSC}$	10 Seconds			Seconds				Seconds	00–59
01H	X	10 Minutes			Minutes				Minutes	00–59
02H	CEB	CB	10 Hours		Hours				Century/Hours	0–1; 00–23
03H	X	X	X	X	X	Day			Day	01–07
04H	X	X	10 Date		Date				Date	01–31
05H	X	X	X	10 Month	Month				Month	01–12
06H	10 Year				Year				Year	00–99
07H	OUT	FT	S	CAL4	CAL3	CAL2	CAL1	CAL0	Control	—
08H	TCS3	TCS2	TCS1	TCS0	DS1	DS0	ROUT1	ROUT0	Trickle Charger	—
09H	OSF	0	0	0	0	0	0	0	Flag	—

X = Read/Write bit

Note: *Unless otherwise specified, the state of the registers is not defined when power is first applied.*

register increments at midnight. Values that correspond to the day of week are user-defined but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on). Illogical time and date entries result in undefined operation. Bit 7 of register 0 is the enable oscillator ($\overline{EOSC}$) bit. When this bit is set to 1, the oscillator is disabled. When cleared to 0, the oscillator is enabled. The initial power-up value of $\overline{EOSC}$ is 0. The clock can be halted whenever the timekeeping functions are not required, minimizing V_{BAT} current ($I_{BACKUPDR}$) when V_{CC} is not applied.

Location 02h is the century/hours register. Bit 7 and bit 6 of the century/hours register are the century-enable bit (CEB) and the century bit (CB). Setting CEB to logic 1 causes the CB bit to toggle, either from a logic 0 to a logic 1, or from a logic 1 to a logic 0, when the years register rolls over from 99 to 00. If CEB is set to logic 0, CB does not toggle.

When reading or writing the time and date registers, secondary (user) buffers are used to prevent errors when the internal registers update. When reading the time and date registers, the user buffers are synchronized to the internal registers on any START or STOP and when the register pointer rolls over to zero. The time information is read from these secondary registers while the clock continues to run. This eliminates the need to reread the registers in case the internal registers update during a read.

The divider chain is reset whenever the seconds register is written. Write transfers occur on the acknowledge from the DS1340. Once the divider chain is reset, to avoid rollover issues, the remaining time and date registers must be written within one second.

On a power-on reset (POR), the time and date are set to 00:00:00 01/01/00 (hh:mm:ss DD/MM/YY) and the day register is set to 01.

Special-Purpose Registers

The DS1340 has three additional registers (control, trickle charger, and flag) that control the RTC, trickle charger, and oscillator flag output.

Control Register (07h)

Bit 7: Output Control (OUT). This bit controls the output level of the FT/OUT pin when the FT bit is set to 0. If FT = 0, the logic level on the FT/OUT pin is 1 if OUT = 1 and 0 if OUT = 0. The initial power-up OUT value is 1.

Bit 6: Frequency Test (FT). When this bit is 1, the FT/OUT pin toggles at a 512Hz rate. When FT is written to 0, the OUT bit controls the state of the FT/OUT pin. The initial power-up value of FT is 0.

Bit 5: Calibration Sign Bit (S). A logic 1 in this bit indicates positive calibration for the RTC. A 0 indicates negative calibration for the clock. See the *Clock Calibration* section for a detailed description of the bit operation. The initial power-up value of S is 0.

Bits 4 to 0: Calibration Bits (CAL4 to CAL0). These bits can be set to any value between 0 and 31 in binary form. See the *Clock Calibration* section for a detailed description of the bit operation. The initial power-up value of CAL0–CAL4 is 0.

Trickle-Charger Register (08h)

The simplified schematic in Figure 6 shows the basic components of the trickle charger. The trickle-charge select (TCS) bits (bits 4–7) control the selection of the trickle charger. To prevent accidental enabling, only a

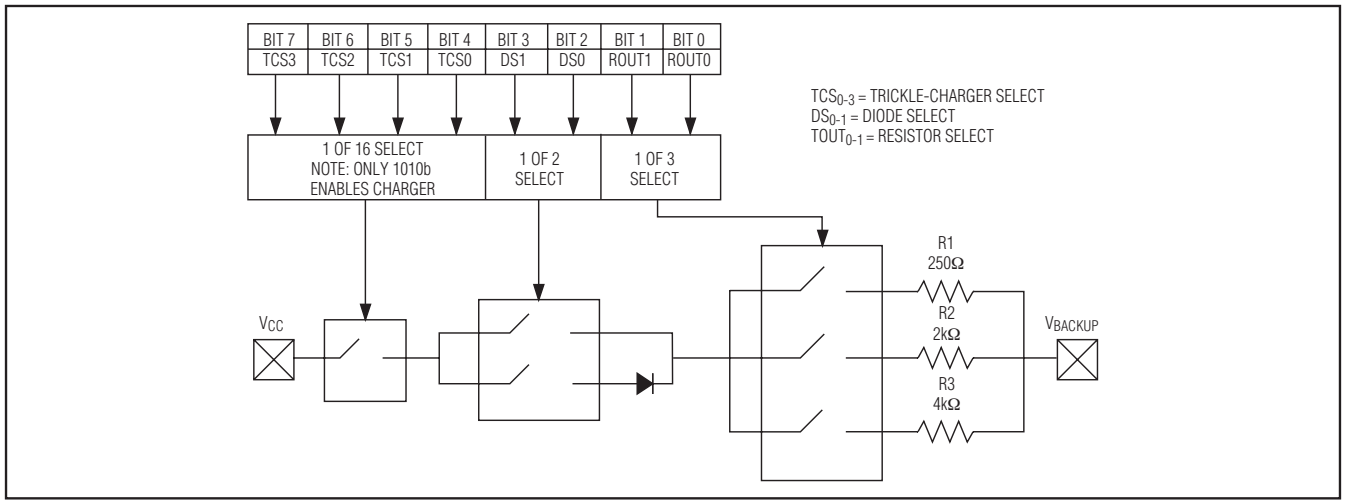


Figure 6. Trickle Charger Functional Diagram

Table 4. Trickle-Charge Register

TCS3	TCS2	TCS1	TCS0	DS1	DS0	ROUT1	ROUT0	FUNCTION
X	X	X	X	0	0	X	X	Disabled
X	X	X	X	1	1	X	X	Disabled
X	X	X	X	X	X	0	0	Disabled
1	0	1	0	0	1	0	1	No diode, 250Ω resistor
1	0	1	0	1	0	0	1	One diode, 250Ω resistor
1	0	1	0	0	1	1	0	No diode, 2kΩ resistor
1	0	1	0	1	0	1	0	One diode, 2kΩ resistor
1	0	1	0	0	1	1	1	No diode, 4kΩ resistor
1	0	1	0	1	0	1	1	One diode, 4kΩ resistor
0	0	0	0	0	0	0	0	Power-on reset value

pattern on 1010 enables the trickle charger. All other patterns disable the trickle charger. The trickle charger is disabled when power is first applied. The diode-select (DS) bits (bits 2, 3) select whether or not a diode is connected between V_{CC} and V_{BACKUP}. If DS is 01, no diode is selected; if DS is 10, a diode is selected. The ROUT bits (bits 0, 1) select the value of the resistor connected between V_{CC} and V_{BACKUP}. Table 3 shows the resistor selected by the resistor select (ROUT) bits and the diode selected by the diode select (DS) bits.

Warning: The ROUT value of 250Ω must not be selected whenever V_{CC} is greater than 3.63V.

The user determines diode and resistor selection according to the maximum current desired for battery or super cap charging (Table 4). The maximum charging current can be calculated as illustrated in the following example.

Assume that a 3.3V system power supply is applied to V_{CC} and a super cap is connected to V_{BACKUP}. Also assume that the trickle charger has been enabled with a diode and resistor R2 between V_{CC} and V_{BACKUP}. The maximum current I_{MAX} would therefore be calculated as follows:

$$I_{MAX} = (3.3V - \text{diode drop}) / R2 \approx (3.3V - 0.7V) / 2k\Omega \approx 1.3mA$$

As the super cap charges, the voltage drop between V_{CC} and V_{BACKUP} decreases and therefore the charge current decreases.

Flag Register (09h)

Bit 7: Oscillator Stop Flag (OSF). A logic 1 in this bit indicates that the oscillator has stopped or was stopped for some time period and may be used to judge the validity of the clock and calendar data. This bit is edge triggered and is set to logic 1 when the internal circuitry senses that the oscillator has transitioned from a normal run state to a STOP condition. The following are examples of conditions that can cause the OSF bit to be set:

1) The first time power is applied.
2) The voltages present on V_{CC} and V_{BACKUP} are insufficient to support oscillation.
3) The $\overline{EOSC}$ bit is set to 1, disabling the oscillator.
4) External influences on the crystal (e.g., noise, leakage).

The OSF bit remains at logic 1 until written to logic 0. It can only be written to logic 0. Attempting to write OSF to logic 1 leaves the value unchanged.

Bits 6 to 0: All other bits in the flag register read as 0 and cannot be written.

Clock Calibration

The DS1340 provides a digital clock calibration feature to allow compensation for crystal and temperature variations. The calibration circuit adds or subtracts counts from the oscillator divider chain at the divide-by-256 stage. The number of pulses blanked (subtracted for negative calibration) or inserted (added for positive calibration) depends upon the value loaded into the five calibration bits (CAL4–CAL0) located in the control register. Adding counts speeds the clock up and subtracting counts slows the clock down.

The calibration bits can be set to any value between 0 and 31 in binary form. Bit 5 of the control register, S, is the sign bit. A value of 1 for the S bit indicates positive calibration, while a value of 0 represents negative calibration. Calibration occurs within a 64-minute cycle. The first 62 minutes in the cycle can, once per minute,

have a one-second interval where the calibration is performed. Negative calibration blanks 128 cycles of the 32,768Hz oscillator, slowing the clock down. Positive calibration inserts 256 cycles of the 32,768Hz oscillator, speeding the clock up. If a binary 1 is loaded into the calibration bits, only the first two minutes in the 64-minute cycle are modified. If a binary 6 is loaded, the first 12 minutes are affected, and so on. Therefore, each calibration step either adds 512 or subtracts 256 oscillator cycles for every 125,829,120 actual 32,678Hz oscillator cycles (64 minutes). This equates to +4.068ppm or -2.034ppm of adjustment per calibration step. If the oscillator runs at exactly 32,768Hz, each of the 31 increments of the calibration bits would represent +10.7 or -5.35 seconds per month, corresponding to +5.5 or -2.75 minutes per month.

For example, if using the FT function, a reading of 512.01024Hz would indicate a +20ppm oscillator frequency error, requiring a -10(00 1010) value to be loaded in the S bit and the five calibration bits.

Note: Setting the calibration bits does not affect the frequency test output frequency. Also note that writing to the control register resets the divider chain.

I²C Serial Data Bus

The DS1340 supports a bidirectional I²C bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are slaves. A master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions must control the bus. The DS1340 operates as a slave on the I²C bus. Connections to the bus are made through the open-drain I/O lines SDA and SCL. Within the bus specifications a standard mode (100kHz max clock rate) and a fast mode (400kHz max clock rate) are defined. The DS1340 works in both modes.

The following bus protocol has been defined (Figure 7):

- Data transfer can be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain high.

START data transfer: A change in the data line's state from high to low, while the clock line is high, defines a START condition.

STOP data transfer: A change in the data line's state from low to high, while the clock line is high, defines a STOP condition.

Data valid: The data line's state represents valid data when, after a START condition, the data line is stable for the duration of the high period of the clock signal. The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between the START and STOP conditions is not limited, and is

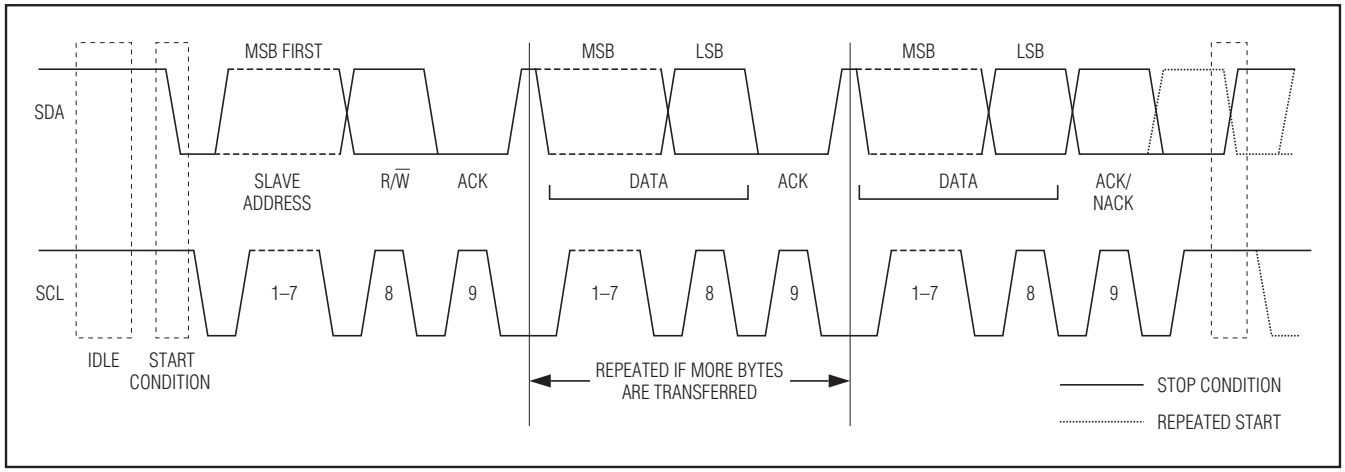


Figure 7. I²C Data Transfer Overview

determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge-related clock pulse. Setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line high to enable the master to generate the STOP condition.

Figures 8 and 9 detail how data transfer is accomplished on the I2C bus. Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible:

Data transfer from a master transmitter to a slave receiver. The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte.

Data transfer from a slave transmitter to a master receiver. The master transmits the first byte (the slave address). The slave then returns an acknowledge bit. Next follows a number of data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a not acknowledge is returned.

The master device generates all the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released.

The DS1340 can operate in the following two modes:

Slave Receiver Mode (Write Mode): Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. Start and STOP conditions are recognized as the beginning and end of a serial transfer. Hardware performs address recognition after reception of the slave address and direction bit. The slave address byte is the first byte received after the master generates the START condition. The slave address byte contains the 7-bit DS1340 address, which is 1101000, followed by the direction bit (R/$\overline{W}$), which is 0 for a write. After receiving and decoding the slave address byte, the DS1340 outputs an acknowledge on SDA. After the DS1340 acknowledges the slave address + write bit, the master transmits a word address to the DS1340. This sets the register pointer on the DS1340, with the DS1340 acknowledging the transfer. The master can then transmit zero or more bytes of data, with the DS1340 acknowledging each byte received. The register pointer increments after each data byte is transferred. The master generates a STOP condition to terminate the data write.

Slave Transmitter Mode (Read Mode): The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. The DS1340 transmits serial data on SDA while the serial clock is input on SCL. Start and STOP conditions are recognized as the beginning and end of a serial transfer. Hardware performs address recognition after reception of the slave address and direction bit. The slave address byte is the first byte received after the master generates the START condition. The slave address byte contains the 7-bit DS1340 address, which is 1101000, followed by the direction bit (R/$\overline{W}$), which is 1 for a read. After receiving and decoding the slave address byte, the DS1340 outputs an acknowledge on SDA. The DS1340 then begins to transmit data starting with the register address pointed to by the register pointer. If the register pointer is not written to before the initiation of a read mode, the first address that is read is the last one stored in the register pointer. The DS1340 must receive a not acknowledge to end a read.

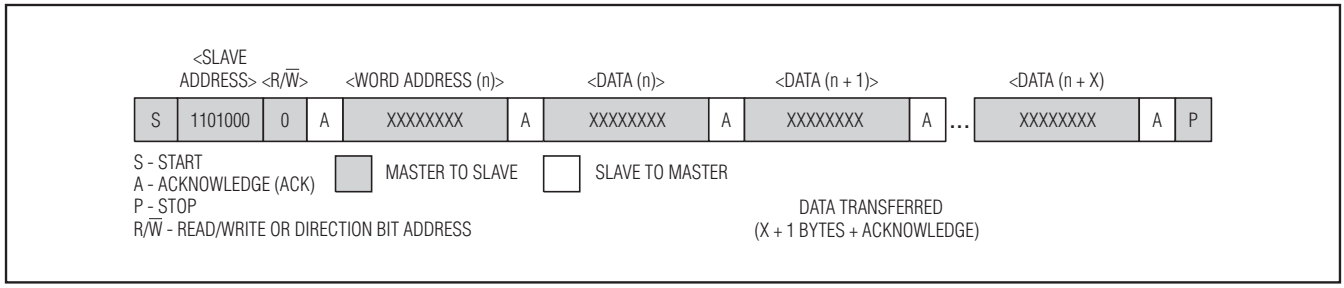


Figure 8. Data Write—Slave Receiver Mode

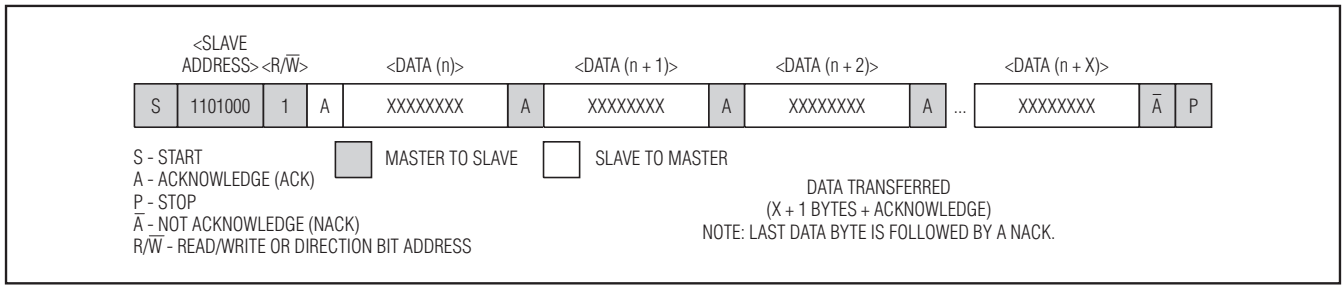


Figure 9. Data Read—Slave Transmitter Mode

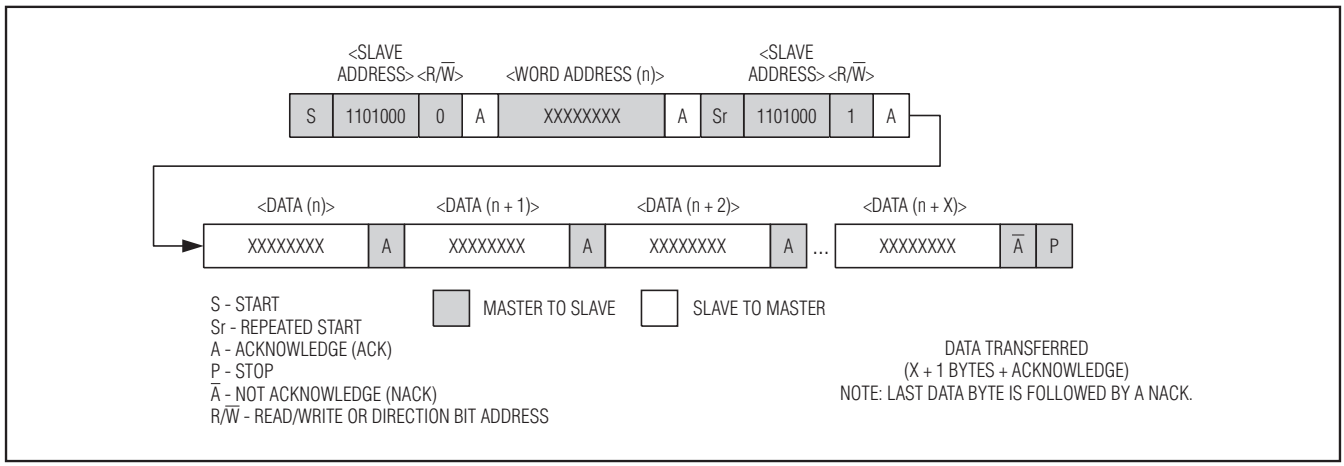


Figure 10. Data Write/Read (Write Pointer, Then Read)—Slave Receive and Transmit

Handling, PC Board Layout, and Assembly

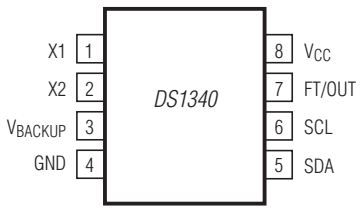
The DS1340C package contains a quartz tuning-fork crystal. Pick-and-place equipment may be used, but precautions should be taken to ensure that excessive shocks are avoided. Exposure to reflow is limited to 2 times maximum. Ultrasonic cleaning should be avoided to prevent damage to the crystal.

Avoid running signal traces under the package, unless a ground plane is placed between the package and the signal line. All N.C. (no connect) pins must be connected to ground.

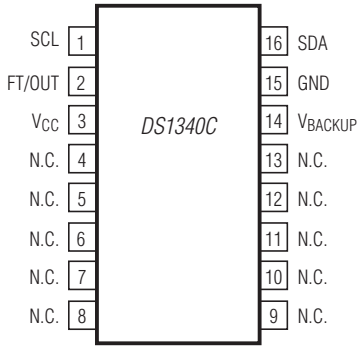
Moisture-sensitive packages are shipped from the factory dry-packed.Handling instructions listed on the package label must be followed to prevent damage during reflow. Refer to the IPC/JEDEC J-STD-020 standard for moisture-sensitive device (MSD) classifications.

Pin Configurations

TOP VIEW



SO, SOP



SO (300 mils)

Chip Information

PROCESS: CMOS

SUBSTRATE CONNECTED TO GROUND

Thermal Information

Theta-JA: 170°C/W (0.150in SO)

Theta-JC: 40°C/W (0.150in SO)

Theta-JA: 221°C/W (µSOP)

Theta-JC: 39°C/W (µSOP)

Theta-JA: 89.6°C/W (0.300in SO)

Theta-JC: 24.8°C/W (0.300in SO)

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8-pin SO (150	S8+2	21-0041	90-0096
8-pin µSOP	U8+1	21-0036	90-0092
16-pin SO (300	W16#H2	21-0042	90-0107

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/03	Initial release.	—
1	7/04	Changed “2-wire” to “I²C” throughout the data sheet.	All
		Added UL recognition info bullet to the *Features* section and to the V_{BACKUP} pin description.	1, 6
		Added the “I/O Capacitance (SCL, SDA)” parameter ($C_{I/O}$) to the *AC Electrical Characteristics* table.	2
		Added “SDA, SCL” and “V_{CC} = 0V” to the “Supply Voltage, Pullup (FT/OUT)” parameter and changed the symbol from “V_{IH}” to “V_{PU}” in the *Recommended DC Operating Conditions* table; in the *DC Electrical Characteristics* table, changed the “Oscillator Current” parameter to “V_{BACKUP} Current.”	3
2	12/04	Added the integrated-crystal and lead-free packages to the *Ordering Information* table; added the integrated-crystal packages to the *Features*, *Pin Configurations*, *Pin Description*.	1, 6
		In Table 1, added increased crystal ESR with increased supply minimum voltage requirement.	6
		Added the *DS1340C Only* section.	7
		Updated Figure 5 to also show the “C Version” crystal.	7
		Added the *Handling, PC Board Layout, and Assembly* section.	12
		Added the integrated-crystal package Theta-JA and Theta-JC information to the *Thermal Information* section.	13
3	11/05	Updated the *Ordering Information* table to correct lead-free/RoHS packages.	1
4	3/06	In the *General Description* section, indicated that the time and date function continues while powered by V_{BACKUP}.	1
		Updated the *Typical Operating Circuit* by removing pin numbers and adding a bypass capacitor.	1
		In the *Pin Description*, updated the V_{BACKUP} description to indicate that no diodes should be placed between the battery and pin and added the UL link; changed the V_{CC} description.	6
		Added the *Power Control* section and new Table 1.	6
		In the *Handling, PC Board Layout, and Assembly* section, added solder reflow information for the RoHS SO package.	13
		Added *Package Information* table.	14
5	8/08	Removed leaded part numbers from the *Ordering Information* table.	1
		Removed the t_{RPU} parameter and RST waveform from Figure 2. Replaced t_{RST} with t_{REC}.	5
		In the *Typical Operating Characteristics* section, updated/changed the “FT vs. V_{BACKUP}” graph to “OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE (FT x 64).”	5
		In the *Pin Description*, added pullup voltage information to the SDA, SCL, and FT/OUT descriptions.	6
		Updated Figure 5.	8
		In the *Clock and Calendar* section, added text explaining the use of $\overline{EOSC}$ to halt the oscillator.	9
		Replaced Figure 7 with an updated version; changed Figures 8 and 9 and added Figure 10 with more comprehensive I²C figures.	13

Revision History (continued)

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
6	10/10	Updated the top mark information in the *Ordering Information* table.	1
		Updated the soldering information in the *Absolute Maximum Ratings* section.	2
		Updated the SDA and SCL pin descriptions in the *Pin Description* table.	6
		Increased ESR from 45,60kΩ (max) to 80kΩ (max) in Table 2.	7
		Updated the *Package Information* table.	14
7	8/11	Raised $V_{CC(MAX)}$ limits for the -18 and -3 versions from 1.89V and 3.3V to 5.5V to provide wide voltage functional operation; reorganized the EC tables and notes	2, 3
8	4/13	Clarified V_{BACKUP} in *Absolute Maximum Ratings* and updated *Clock Calibration* section	2, 9
9	4/15	Revised *Benefits and Features* section	1

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