300-mA Output, High PSRR, Low-Dropout Linear Regulator

Features

- Input Voltage Range: 1.5 V to 5.5 V
- Output Voltage Range:
  - Fixed Output Voltage: 0.75 V to 3.6 V
  - Adjustable Output Voltage: 0.75 V to 5 V
- ±1% Typical Output Accuracy Under Room Temperature
- 300-mA Maximum Output Current
- Low Dropout Voltage: 250 mV Typically at 300 mA
- High PSRR:
  - 70 dB at 1 kHz
  - 54 dB at 1 MHz
- Good Transient Response
- Stable with a 4.7-μF or Larger Ceramic Output Capacitor
- Inrush Current Control During Startup
- Thermal Shutdown and Over-Current Protection
- Temperature Range: −40°C to +125°C
- Package Options:
  - SOT23-5
  - DFN1×1-4

Applications

- Portable and Battery-Powered Equipment
- Mobile Phones and Tablets
- Digital Cameras and Audio Devices Power Supply
- Video Surveillance
- Wireless and IoT Modules

Description

The TPL5031 is a series of 300-mA high PSRR, low noise, and low dropout linear regulators with high output accuracy. The TPL5031 series supports both fixed output voltage ranges from 0.75 V to 3.6 V and adjustable output voltage ranges from 0.75 V to 5 V with an external resistor divider. The TPL5031 is stable with a 4.7-μF or larger ceramic output capacitor.

The TPL5031 series has a high PSRR with 70 dB at 1 kHz. This feature makes the TPL5031 series very suitable for power-ripple-sensitive applications with high noise from the previous stage power supply, such as high-performance analog devices, or high-definition imaging equipment. The output shortage protection and thermal overload protection circuits improve reliability under heavy load conditions.

The TPL5031 series provides SOT23-5 and DFN1×1-4 packages with a guaranteed operating junction temperature range from −40°C to +125°C.

Typical Application Circuit

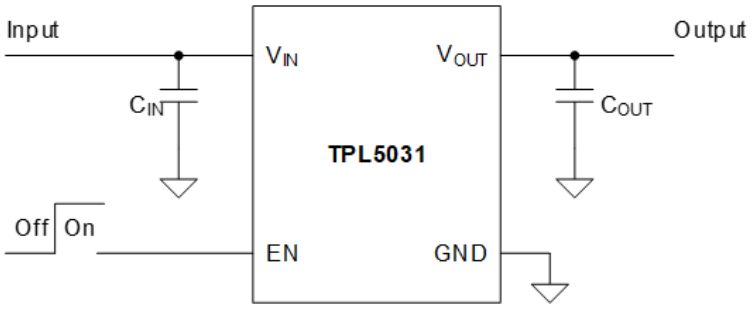


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Product Family Table

Order Number	Output Voltage (V)	Package
TPL5031075-S5TR(1)	0.75 V	SOT23-5
TPL503108-S5TR	0.8 V	SOT23-5
TPL503109-S5TR(1)	0.9 V	SOT23-5
TPL5031092-S5TR(1)	0.92 V	SOT23-5
TPL503110-S5TR(1)	1.0 V	SOT23-5
TPL503111-S5TR(1)	1.1 V	SOT23-5
TPL503112-S5TR	1.2 V	SOT23-5
TPL503115-S5TR	1.5 V	SOT23-5
TPL503118-S5TR	1.8 V	SOT23-5
TPL503121-S5TR(1)	2.1 V	SOT23-5
TPL503125-S5TR	2.5 V	SOT23-5
TPL503127-S5TR(1)	2.7 V	SOT23-5
TPL503128-S5TR	2.8 V	SOT23-5
TPL503129-S5TR(1)	2.9 V	SOT23-5
TPL503130-S5TR(1)	3.0 V	SOT23-5
TPL503133-S5TR	3.3 V	SOT23-5
TPL503136-S5TR(1)	3.6 V	SOT23-5
TPL5031075-DF1R(1)	0.75 V	DFN1×1-4
TPL503108-DF1R(1)	0.8 V	DFN1×1-4
TPL503109-DF1R(1)	0.9 V	DFN1×1-4
TPL5031092-DF1R(1)	0.92 V	DFN1×1-4
TPL503110-DF1R(1)	1.0 V	DFN1×1-4
TPL503111-DF1R(1)	1.1 V	DFN1×1-4
TPL503112-DF1R(1)	1.2 V	DFN1×1-4
TPL503115-DF1R(1)	1.5 V	DFN1×1-4
TPL503118-DF1R	1.8 V	DFN1×1-4
TPL503121-DF1R(1)	2.1 V	DFN1×1-4
TPL503125-DF1R(1)	2.5 V	DFN1×1-4
TPL503127-DF1R(1)	2.7 V	DFN1×1-4
TPL503128-DF1R(1)	2.8 V	DFN1×1-4
TPL503129-DF1R(1)	2.9 V	DFN1×1-4
TPL503130-DF1R(1)	3.0 V	DFN1×1-4
TPL503133-DF1R	3.3 V	DFN1×1-4
TPL503136-DF1R(1)	3.6 V	DFN1×1-4

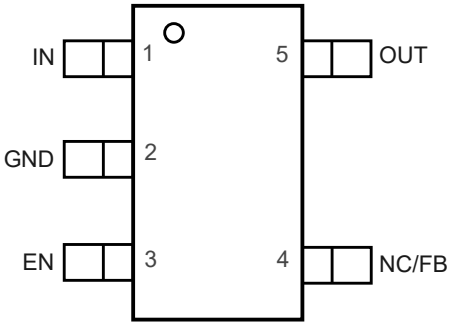
(1) For future product, contact 3PEAK factory for more information and samples.

Revision History

Date	Revision	Notes
2020-08-31	Rev.Pre.0	Preliminary version.
2021-06-23	Rev.A.0	Initial released version.
2022-02-15	Rev.A.1	1. Updated the output voltage option and output voltage accuracy. 2. Added the note of V_{DO}.
2024-11-28	Rev.A.2	Updated to a new datasheet format.
2026-07-27	Rev.A.3	1. Added the note in the Product Family Table 2. Added new part number TPL503118-DF1R and TPL503133-DF1R into Ordering Information table.

Pin Configuration and Functions

TPL5031 Series
SOT23-5
Top View



TPL5031 Series
DFN1×1-4
Top View

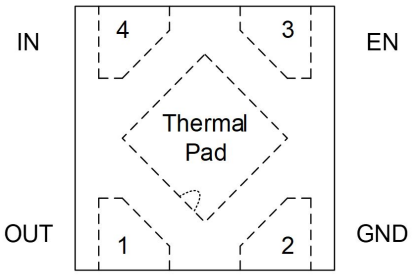


Table 1. Pin Functions: TPL5031

Pin No.		Name	I/O	Description
SOT23-5	DFN1×1-4			
3	3	EN	I	The enable pin. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. For automatic startup, connect EN to IN directly.
4	-	FB	I	The output feedback pin (adjustable version only). Connect to a resistor divider to adjust the output voltage.
2	2	GND	–	The ground reference pin. Connect the GND pin to PCB ground plane directly.
1	4	IN	I	The input voltage pin. Bypass IN to GND with a 1-μF or greater capacitor.
4	-	NC	–	Not connected.
5	1	OUT	O	The regulated output voltage pin. Bypass OUT to GND with a 4.7-μF or greater capacitor.

Specifications

Absolute Maximum Ratings

Parameter		Min	Max	Unit
IN, EN		−0.3	6	V
OUT		−0.3	6	V
FB		−0.3	6	V
T_J	Maximum Junction Temperature	−40	150	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering, 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
(2) All voltage values are with respect to GND.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±4	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Max	Unit
IN		1.5	5.5	V
EN		0	5.5	V
OUT		0	5	V
I_{OUT}		0	300	mA
C_{OUT}		4.7		μF
T_J	Operating Junction Temperature Range	−40	125	°C
P_D	Power Dissipation at Room Temperature	0	300	mW

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
SOT23-5	280	62	°C/W
DFN1×1-4	210	110	°C/W

Electrical Characteristics

All test conditions: V_{IN} = $V_{OUT\ (NOM)}$ + 0.5 V or 2.4 V, whichever is greater; C_{OUT} = 4.7 µF, I_{OUT} = 1 mA, T_A = +25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply Voltage and Current						
V_{IN}	Input Supply Voltage Range		1.5		5.5	V
I_{GND}	Ground Pin Current	I_{OUT} = 0 mA		55		µA
I_{SHDN}	Shutdown Current	V_{EN} ≤ 0.4 V		0.02		µA
Enable Input Voltage and Current						
$V_{IH(EN)}$	EN Logic-Input High Level (Enable)		1.1		V_{IN}	V
$V_{IL(EN)}$	EN Logic-Input Low Level (Disable)		0		0.4	V
I_{EN}	EN Pin Leakage Current	V_{EN} = 0 V or 5.5 V		1		µA
Regulated Output Voltage and Current						
V_{OUT}	Output Voltage Accuracy	V_{OUT} ≤ 2.0 V	−40		+40	mV
		V_{OUT} > 2.0 V	−2%		2%	
$\triangle V_{OUT}$	Line Regulation	$V_{OUT\ (NOM)}$ + 0.5 V ≤ V_{IN} ≤ 5.5V, V_{IN} ≥ 1.5 V, I_{OUT} = 1 mA		1		mV
	Load Regulation	I_{OUT} = 1 mA to 300 mA		20		mV
V_{DO} (1)	Dropout Voltage	V_{OUT} = 0.8 V, I_{OUT} = 300 mA		1200		mV
		V_{OUT} = 1.2 V, I_{OUT} = 300 mA		800		mV
		V_{OUT} = 1.8 V, I_{OUT} = 300 mA		460		mV
		V_{OUT} = 2.8 V, I_{OUT} = 300 mA		340		mV
		V_{OUT} = 3.3 V, I_{OUT} = 300 mA		250		mV
I_{OUT}	Output Current	V_{OUT} in regulation	0		300	mA
I_{CL}	Output Current Limit	V_{OUT} = 0.9 × $V_{OUT\ (NOM)}$	350	500		mA
I_{SC}	Short-Circuit Current Limit	R_{LOAD} ≤ 20 mΩ		300		mA
R_{DIS}	Active Output Discharge Resistance	V_{EN} ≤ 0.4 V		110		Ω
PSRR	Power Supply Rejection Ratio	I_{OUT} = 10 mA, f = 1 kHz		70		dB
		I_{OUT} = 10 mA, f = 1 MHz		54		dB
V_N	Output Noise Voltage	I_{OUT} = 100 mA, B_W = 100 Hz to 100 kHz		178		μV_{RMS}
t_{STR}	Start-up Time	I_{OUT} = 300 mA		170		µs
Temperature Range						
T_{SD}	Thermal Shutdown Temperature			150		ºC
	Thermal Shutdown Hysteresis			20		ºC

(1) The dropout voltage is the minimum input to output voltage differential needed to maintain the regulation at a specified output current. In the dropout mode, the output voltage is equal to V_{IN} − V_{DO}.

Typical Performance Characteristics

All test conditions: V_{IN} = $V_{OUT\ (NOM)}$ + 1 V, V_{OUT} = 3.3 V, I_{OUT} = 1 mA, C_{OUT} = 4.7 µF, unless otherwise noted.

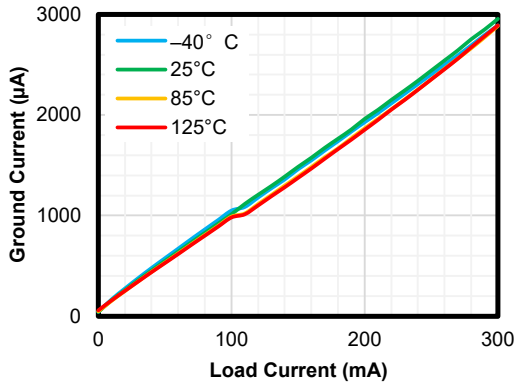


Figure 1. Quiescent Current vs. Output Current

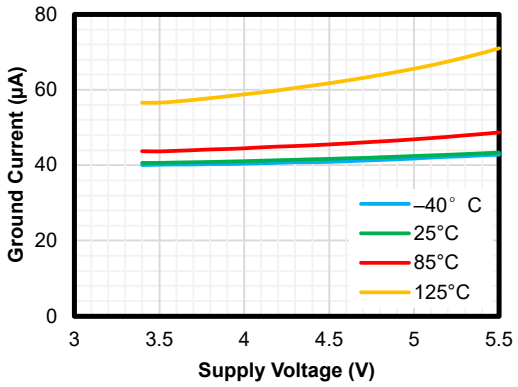


Figure 2. Quiescent Current vs. Input Voltage

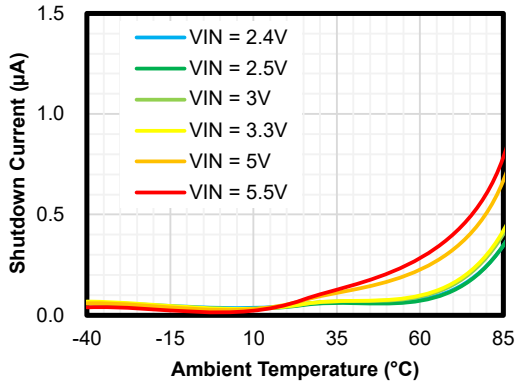


Figure 3. Shutdown Current vs. Ambient Temperature

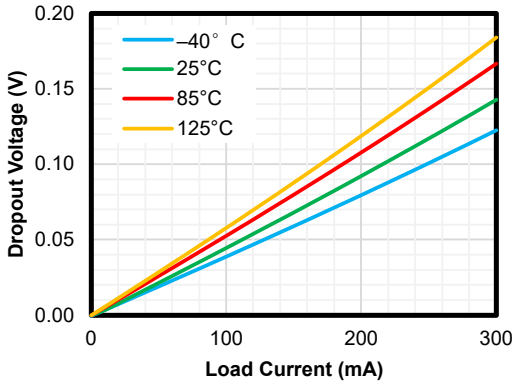


Figure 4. Dropout Voltage vs. Output Current

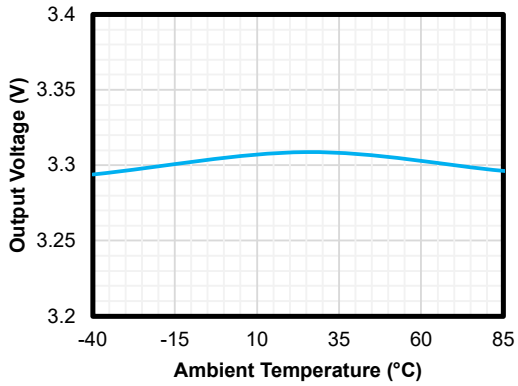


Figure 5. Output Voltage vs. Ambient Temperature

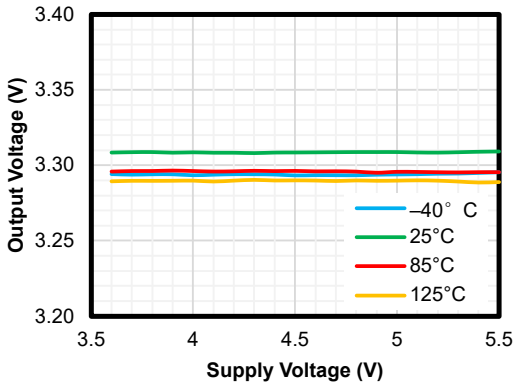


Figure 6. Output Voltage vs. Input Voltage

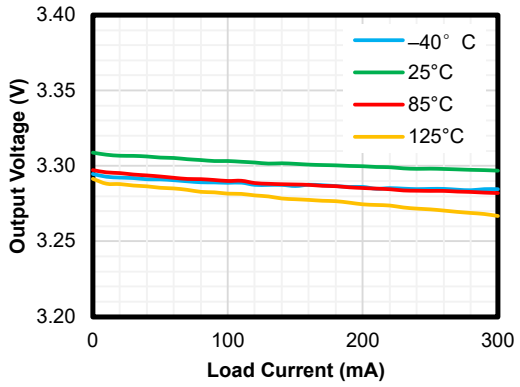
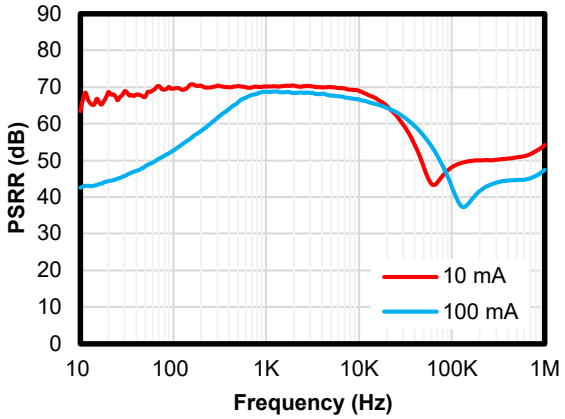
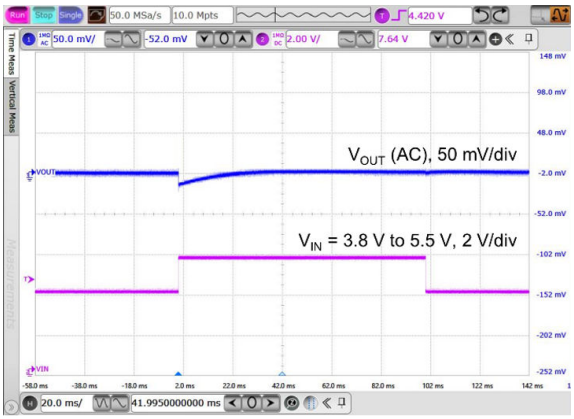


Figure 7. Output Voltage vs. Output Current



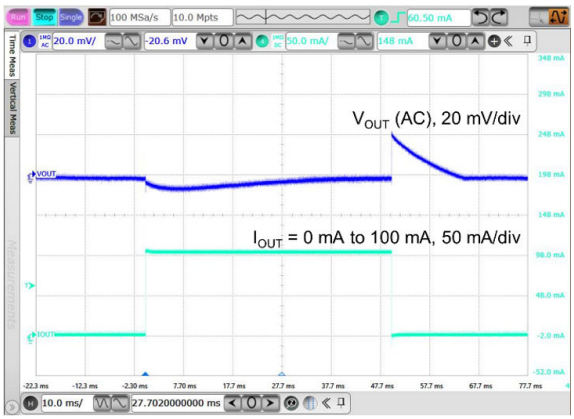
C_{OUT} = 10 µF

Figure 8. PSRR



V_{IN} = 3.8 V to 5.5 V

Figure 9. Line Transient



I_{OUT} = 0 mA to 100 mA

Figure 10. Load Transient

Detailed Description

Overview

The TPL5031 is a series of 300-mA high PSRR, low noise, and low dropout linear regulators with high output accuracy. The TPL5031 series supports both fixed output voltage ranges from 0.75 V to 3.6 V and adjustable output voltage ranges from 0.75 V to 5 V with an external resistor divider. The TPL5031 series is stable with a 4.7-µF or larger ceramic output capacitor.

The TPL5031 series has a high PSRR with 70 dB at 1 kHz. This feature makes the TPL5031 series very suitable for power-ripple-sensitive applications with high noise from the previous stage power supply, such as high-performance analog devices, or high-definition imaging equipment. The output shortage protection and thermal overload protection circuits improve reliability under heavy load conditions.

Functional Block Diagram

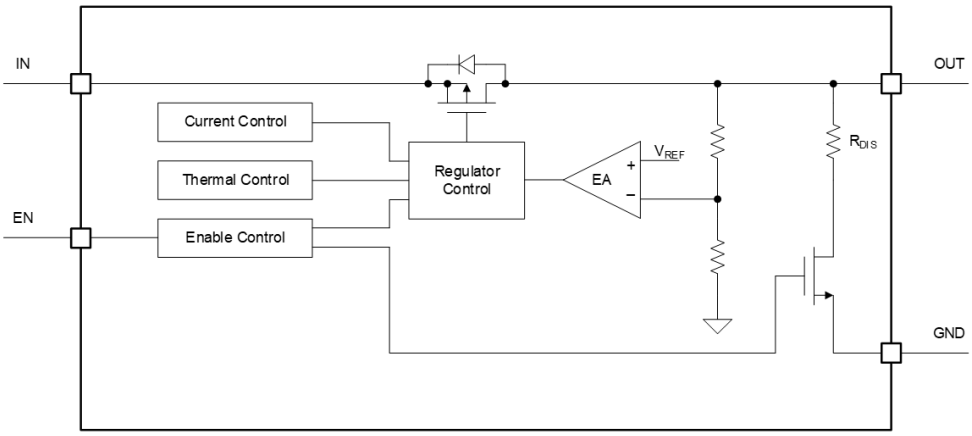


Figure 11. Functional Block Diagram

Feature Description

Enable (EN)

The enable pin (EN) is active high. Connect this pin to the GPIO of an external processor or digital logic control circuit to enable and disable the device. Or connect this pin to the IN pin for self-bias applications.

Regulated Output Voltage (OUT)

The TPL5031 series is available in fixed voltage versions of 0.75 V to 3.6 V. When the input voltage is higher than $V_{OUT\ (NOM)}$ + V_{DO} or 1.5 V, the output pin is the regulated output based on the selected voltage version. When the input voltage falls below $V_{OUT\ (NOM)}$ + V_{DO} or 1.5 V, the output pin tracks the input voltage minus the dropout voltage based on the load current.

Current Limit

The TPL5031 series integrates an internal current limit that helps to protect the regulator during over-load fault conditions. When the output is overloaded, the LDO supplies a typical current of ICL. The output voltage is not regulated in the current limit mode, and the output voltage falls to $V_{OUT} = I_{CL} \times R_{LOAD}$.

Short-Circuit Protection

The TPL5031 series integrates short-circuit protection. When the output pin is shorted to the ground, the output current of the TPL5031 series is limited to a typical value of I_{SC}.

Thermal Shutdown

During normal operation, the LDO junction temperature should not exceed 125°C. When the junction temperature exceeds the thermal shutdown threshold, the LDO shuts down the output immediately. Until the junction temperature falls below the thermal shutdown threshold minus thermal shutdown hysteresis, the output turns on again.

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPL5031 is a series of 300-mA high PSRR, ultra-low noise, and low-dropout linear regulators. The following application schematic shows a typical usage of the TPL5031 series.

Typical Application

Figure 12 shows the typical application schematic of the TPL5031 series.

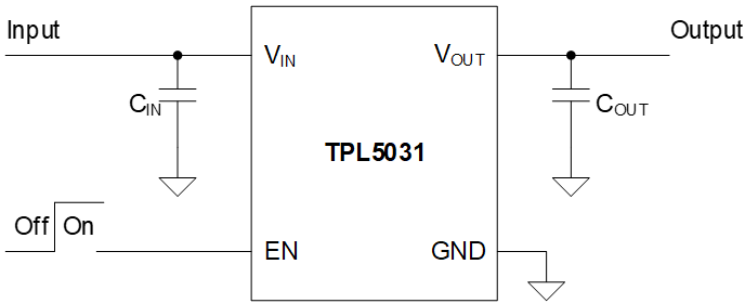


Figure 12. Typical Application Schematic

Input Capacitor and Output Capacitor

3PEAK recommends adding a 1-μF or greater capacitor with a 0.1-μF bypass capacitor in parallel at the IN pin to keep the input voltage stable. The voltage rating of the capacitors must be greater than the maximum input voltage.

To ensure loop stability, the TPL5031 series requires an output capacitor of 4.7 μF or greater. 3PEAK recommends selecting an X5R- or X7R-type ceramic capacitor with low ESR over temperature.

Both input capacitors and output capacitors must be placed as close to the device pins as possible.

Power Dissipation

During normal operation, the LDO junction temperature should not exceed 125°C. Use the below equations to calculate the power dissipation and estimate the junction temperature.

The power dissipation can be calculated using Equation 1.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad (1)$$

The junction temperature can be estimated using Equation 2. θ_{JA} is the junction-to-ambient thermal resistance.

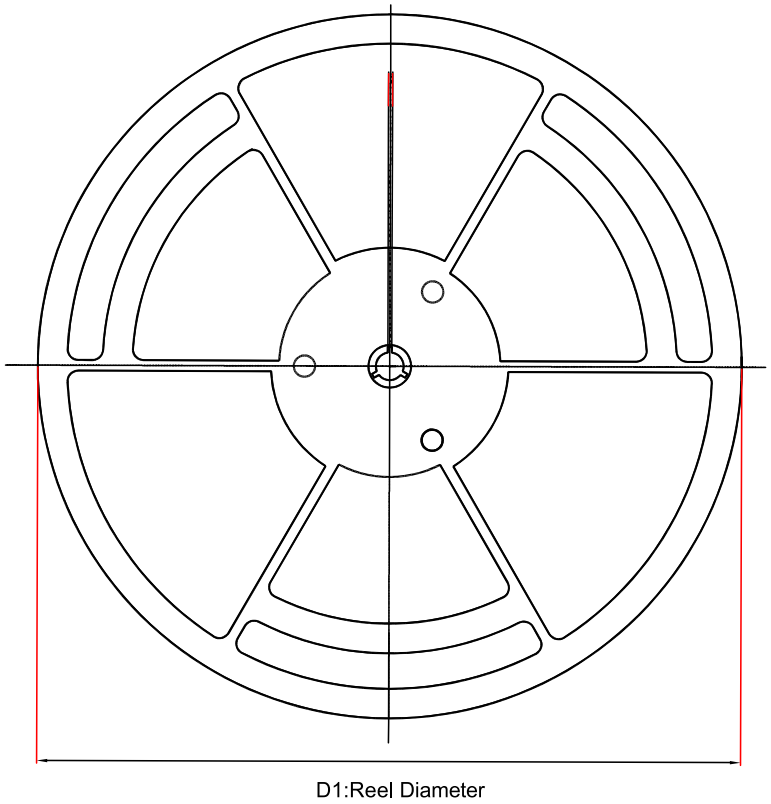
$$T_J = T_A + P_D \times \theta_{JA} \quad (2)$$

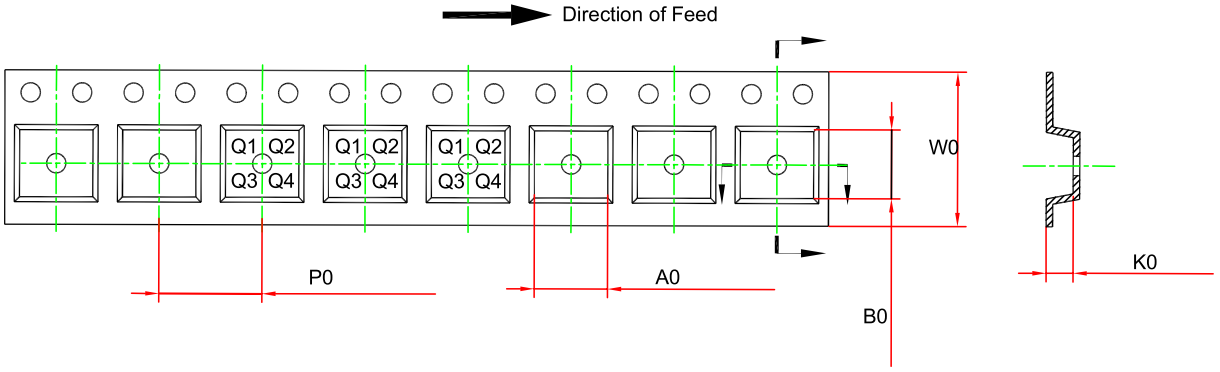
Layout

Layout Guideline

- Both input capacitors and output capacitors must be placed as close to the device pins as possible.
- It is recommended to bypass the input pin to the ground with a 0.1-μF bypass capacitor. The loop area formed by the bypass capacitor connection, the IN pin, and the GND pin of the system must be as small as possible.
- It is recommended to use wide and thick copper to minimize the I×R drop and heat dissipation.

Tape and Reel Information





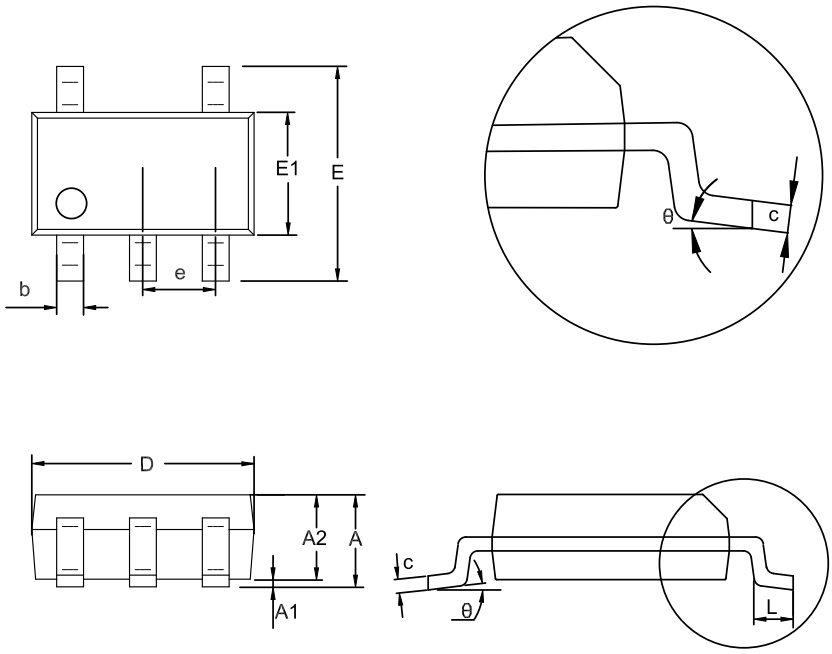
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPL5031xx-S5TR (1)	SOT23-5	180.0	13.1	3.2	3.2	1.4	4.0	8.0	Q3
TPL5031xx-DF1R	DFN1×1-4	180.0	10.0	1.16	1.16	0.5	2.0	8.0	Q1

(1) The output voltage value, xx = 075 and 08 to 50. e.g., 33 means 3.3-V output voltage.

Package Outline Dimensions

SOT23-5

Package Outline Dimensions S5T(SOT23-5-A)



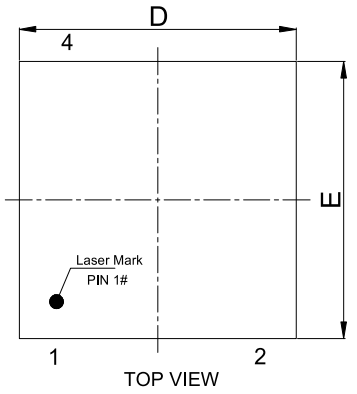
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.150	0.000	0.006
A2	1.000	1.200	0.039	0.047
b	0.280	0.500	0.011	0.020
c	0.100	0.230	0.004	0.009
D	2.820	3.020	0.111	0.119
E	2.600	3.000	0.102	0.118
E1	1.500	1.720	0.059	0.068
e	0.950 BSC		0.037 BSC	
L	0.300	0.600	0.012	0.024
θ	0	8°	0	8°

NOTES

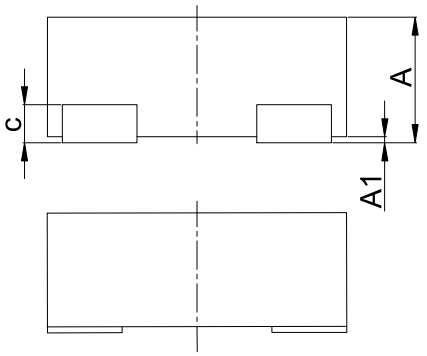
1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

DFN1×1

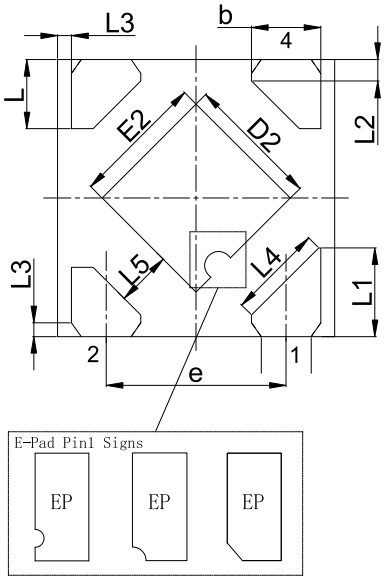
Package Outline Dimensions DF1(DFN1X1-4-A)



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.350	0.400	0.014	0.016
A1	0.000	0.050	0.000	0.002
b	0.200	0.300	0.008	0.012
c	0.070	0.170	0.003	0.007
D	0.950	1.050	0.037	0.041
D2	0.430	0.530	0.017	0.021
E	0.950	1.050	0.037	0.041
E2	0.430	0.530	0.017	0.021
e	0.650 BSC		0.026 BSC	
L	0.200	0.300	0.008	0.012
L1	0.270	0.370	0.011	0.015
L2	0.077 BSC		0.003 BSC	
L3	0.050 BSC		0.002 BSC	
L4	0.340 BSC		0.013 BSC	
L5	0.200 BSC		0.008 BSC	

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPL5031075-S5TR (1)	−40 to 125°C	SOT23-5	L9B	3	Tape and Reel, 3,000	Green
TPL503108-S5TR	−40 to 125°C	SOT23-5	L9C	3	Tape and Reel, 3,000	Green
TPL503109-S5TR (1)	−40 to 125°C	SOT23-5	L9D	3	Tape and Reel, 3,000	Green
TPL5031092-S5TR (1)	−40 to 125°C	SOT23-5	L9T	3	Tape and Reel, 3,000	Green
TPL503110-S5TR (1)	−40 to 125°C	SOT23-5	L9E	3	Tape and Reel, 3,000	Green
TPL503111-S5TR (1)	−40 to 125°C	SOT23-5	L9F	3	Tape and Reel, 3,000	Green
TPL503112-S5TR	−40 to 125°C	SOT23-5	L9G	3	Tape and Reel, 3,000	Green
TPL503115-S5TR	−40 to 125°C	SOT23-5	L9H	3	Tape and Reel, 3,000	Green
TPL503118-S5TR	−40 to 125°C	SOT23-5	L9I	3	Tape and Reel, 3,000	Green
TPL503121-S5TR (1)	−40 to 125°C	SOT23-5	L9J	3	Tape and Reel, 3,000	Green
TPL503125-S5TR	−40 to 125°C	SOT23-5	L9K	3	Tape and Reel, 3,000	Green
TPL503127-S5TR (1)	−40 to 125°C	SOT23-5	L9L	3	Tape and Reel, 3,000	Green
TPL503128-S5TR	−40 to 125°C	SOT23-5	L9M	3	Tape and Reel, 3,000	Green
TPL503129-S5TR (1)	−40 to 125°C	SOT23-5	L9N	3	Tape and Reel, 3,000	Green
TPL503130-S5TR (1)	−40 to 125°C	SOT23-5	L9P	3	Tape and Reel, 3,000	Green
TPL503133-S5TR	−40 to 125°C	SOT23-5	L9Q	3	Tape and Reel, 3,000	Green
TPL503136-S5TR (1)	−40 to 125°C	SOT23-5	L9R	3	Tape and Reel, 3,000	Green
TPL503118-DF1R	−40 to 125°C	DFN1X1-4	L9I	3	Tape and Reel, 12,000	Green
TPL503133-DF1R	−40 to 125°C	DFN1X1-4	L9Q	3	Tape and Reel, 12,000	Green

(1) For future product, contact 3PEAK factory for more information and samples.

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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