200-mA Output,1-μA Ultra-Low Quiescent Current LDO

Features

- Typical 1.4-μA Ultra-low Quiescent Current
- Input Voltage Range: 2.4 V to 6 V
- Output Voltage Options:
  - Fixed: 1 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 2.8 V, 3 V, 3.3 V, 3.6 V
- ±1% Output Voltage Accuracy under Room Temperature
- Maximum Output Current: 200 mA
- Low Shutdown Current
- Low Dropout Voltage: 170 mV at 200 mA
- Current Limit and Thermal Protection
- Stable with 2.2-μF Ceramic Capacitor
- Active Output Discharge While Disable
- Soft-start Limits Input Current Surge During Enable
- Junction Temperature Range: −40°C to +125°C
- Packages: SOT23-3, SOT23-5, and DFN1x1-4

Applications

- Handheld Devices with Battery Power Supply
- Portable Devices with Battery Power Supply
- Wearable Applications, Bluetooth Headsets
- Wireless and IoT Modules
- Personal Electronics, Personal Healthcare

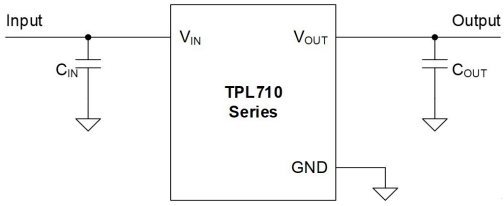
Description

The TPL710 is a series of CMOS process low Iq linear regulators with enable control function. The TPL710 series supports a maximum 200-mA output current, with typically only a 1.4-μA ultra-low quiescent current. TPL710 series is stable with low-ESR small ceramic output capacitors from 2.2 μF to 10 μF.

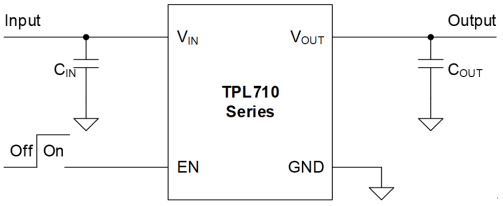
The TPL710 series has fast response performance when the load current dynamic drops or rises, especially for the load-current dynamic from some heavy load. The TPL710 series has a current limit and thermal protection, which improves the TPL710 series with high reliability.

The TPL710 series has a fixed output voltage range from 1 V to 3.6 V with ±1% output voltage accuracy, line regulation, and load regulation under room temperature. The TPL710 series is guaranteed over the junction temperature range of −40°C to +125°C. The TPL710 series is available in the SOT23-3, SOT23-5, and DFN1x1-4 packages.

Typical Application Schematic



TPL710 Series without Enable Pin



TPL710 Series with Enable Pin

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Product Family Table

Order Number	Output Voltage (V)	Package
TPL710F10-3TR	Fixed 1.0 V	SOT23-3
TPL710F12-3TR	Fixed 1.2 V	SOT23-3
TPL710F15-3TR	Fixed 1.5 V	SOT23-3
TPL710F18-3TR	Fixed 1.8 V	SOT23-3
TPL710F25-3TR	Fixed 2.5 V	SOT23-3
TPL710F28-3TR	Fixed 2.8 V	SOT23-3
TPL710F30-3TR	Fixed 3.0 V	SOT23-3
TPL710F33-3TR	Fixed 3.3 V	SOT23-3
TPL710F36-3TR	Fixed 3.6 V	SOT23-3
TPL710F10-5TR	Fixed 1.0 V	SOT23-5
TPL710F12-5TR	Fixed 1.2 V	SOT23-5
TPL710F15-5TR	Fixed 1.5 V	SOT23-5
TPL710F18-5TR	Fixed 1.8 V	SOT23-5
TPL710F25-5TR	Fixed 2.5 V	SOT23-5
TPL710F28-5TR	Fixed 2.8 V	SOT23-5
TPL710F30-5TR	Fixed 3.0 V	SOT23-5
TPL710F33-5TR	Fixed 3.3 V	SOT23-5
TPL710F36-5TR	Fixed 3.6 V	SOT23-5
TPL710F10-FR	Fixed 1.0 V	DFN1x1-4
TPL710F12-FR	Fixed 1.2 V	DFN1x1-4
TPL710F15-FR	Fixed 1.5 V	DFN1x1-4
TPL710F18-FR	Fixed 1.8 V	DFN1x1-4
TPL710F25-FR	Fixed 2.5 V	DFN1x1-4
TPL710F28-FR	Fixed 2.8 V	DFN1x1-4
TPL710F30-FR	Fixed 3.0 V	DFN1x1-4
TPL710F33-FR	Fixed 3.3 V	DFN1x1-4
TPL710F36-FR	Fixed 3.6 V	DFN1x1-4

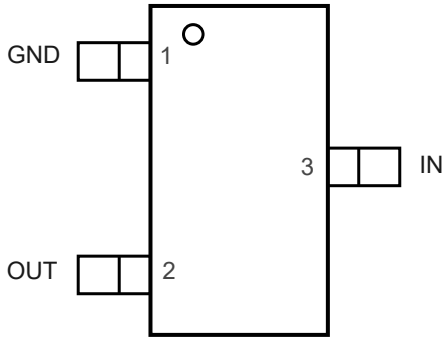
Revision History

Date	Revision	Notes
2018-09-08	Rev.Pre.0	Preliminary Version
2019-01-10	Rev.A.0	Initial Release
2019-08-30	Rev.A.1	Added 3.6 V Output Voltage Option
2020-12-31	Rev.A.2	1. Added Junction Temperature Range: −40°C to +125°C 2. Added IGND and ISHDN Data with Junction Temperature Range
2021-03-29	Rev.A.3	1. Changed the Pin 1 Orientation of the SOT23-3 package

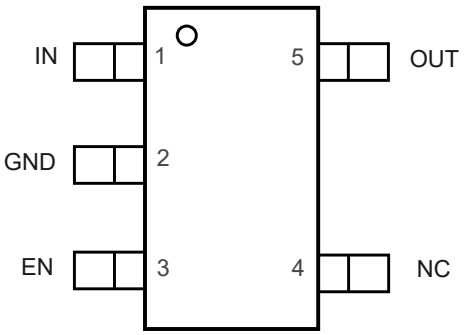
Date	Revision	Notes
		2. Added Tape and Reel Information
2021-06-15	Rev.A.4	Added 1.5 V Output Voltage Option
2022-01-05	Rev.A.5	1. Removed Part Number in SOT89-3 Package 2. Removed Operating Temperature Range
2022-05-08	Rev.A.6	Corrected Tape and Reel Information
2024-11-30	Rev.A.7	Updated to a new datasheet format

Pin Configuration and Functions

TPL710
SOT23-3 Package
Top View



TPL710
SOT23-5 Package
Top View



TPL710
DFN1X1-4 Package
Top View

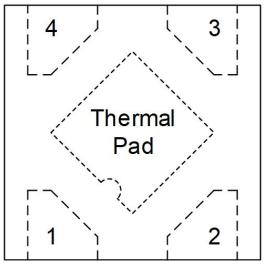


Table 1. Pin Functions: TPL710

Pin			Name	I/O	Description
SOT23-3	SOT23-5	DFN-4			
–	3	3	EN	I	Regulator enable pin. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. For automatic startup, connect EN to IN directly.
1	2	2	GND	–	Ground reference pin. Connect the GND pin to the PCB ground plane directly.
3	1	4	IN	I	Input voltage pin. Bypass IN to GND with a 1 μF or greater capacitor.
–	4	–	NC	–	No connection.
2	5	1	OUT	O	Regulated output voltage pin. Bypass OUT to GND with a 2.2 μF or greater capacitor.

(1) Thermal pad must be connected to the PCB ground plane to maximize the thermal performance.

Specifications

Absolute Maximum Ratings

Parameter		Min	Max	Unit
V_{IN}, V_{EN}	Input Voltage	−0.3	6.5	V
V_{OUT}	Output Voltage	−0.3	6.5	V
T_J	Junction Temperature Range	−40	150	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime
(2) All voltage values are with respect to GND.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±4	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Max	Unit
V_{IN}	Input Voltage	2.4	6	V
V_{EN}	Enable Voltage	0	V_{IN}	V
V_{OUT}	Output Voltage	0	5	V
I_{OUT}	Output Current	0	200	mA
T_J	Operating Junction Temperature Range	−40	125	°C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
SOT23-3	280	62	°C/W
SOT23-5	280	62	°C/W
DFN1x1-4	210	110	°C/W

Electrical Characteristics

All test conditions: V_{IN} = $V_{OUT\ (NOM)}$ + 1 V or 2.4 V, whichever is greater; C_{OUT} = 2.2 μF, T_A = +25°C, unless otherwise noted.

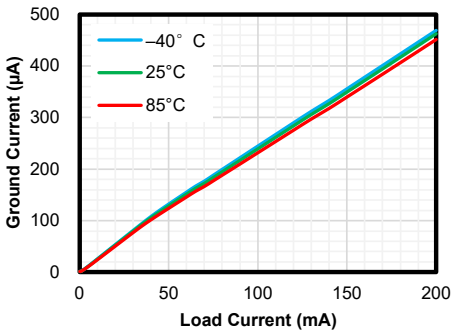
Parameter		Conditions	T_A	Typ	Max	Unit
Supply Voltage and Current						
V_{IN}	Input Voltage Range		2.4		6	V
I_{GND}	Ground Pin Current	I_{OUT} = 0 mA, –40°C ≤ T_J ≤ +105°C		1.4	8	μA
		I_{OUT} = 0 mA, –40°C ≤ T_J ≤ +125°C			30	μA
		V_{IN} = 5 V, I_{OUT} = 200 mA		500		μA
I_{SHDN}	Shutdown Current	EN = GND, –40°C ≤ T_J ≤ +105°C		0.1	3	μA
		EN = GND, –40°C ≤ T_J ≤ +125°C			5	μA
UVLO	V_{IN} Under-Voltage Lock-out	V_{IN} Rising		1.8		V
		Hysteresis		200		mV
Enable Input Voltage and Current (4-/5-Pin Package Only)						
$V_{IH\ (EN)}$	EN Logic-input High Level (Enable)		1.2		V_{IN}	V
$V_{IL\ (EN)}$	EN Logic-input Low Level (Disable)		0		0.4	V
I_{EN}	EN Pin Leakage Current	EN = V_{IN}		20		nA
Regulated Output Voltage and Current						
V_{OUT}	Output Voltage Accuracy	I_{OUT} = 30 mA, T_J = +25°C		1%		
		I_{OUT} = 30 mA, –40°C ≤ T_J ≤ +125°C	−3%		3%	
V_{REF_I}	Line Regulation	V_{IN} = $V_{OUT\ (NOM)}$ + 1 V to 6 V, or V_{IN} ≥2.4V , I_{OUT} = 1 mA		3		mV
	Load Regulation	I_{OUT} = 1 mA to 200 mA		40		mV
V_{DO}(1)	Dropout Voltage	I_{OUT}		40		mV
		V_{IN} = 0.98 × $V_{OUT\ (NOM)}$, I_{OUT} = 100 mA		80		mV

Parameter		Conditions	T_A	Typ	Max	Unit
		V_{IN} = 0.98 × $V_{OUT\ (NOM)}$, I_{OUT} = 200 mA		170		mV
I_{OUT}	Output Current	V_{OUT} in Regulation	0		200	mA
I_{CL}	Output Current limit	V_{OUT} = 0.9 × $V_{OUT\ (NOM)}$	300	560	800	mA
R_{DIS}	Output Discharge Resistance	V_{IN} = $V_{OUT\ (NOM)}$ + 1 V, EN = GND		190		Ω
PSRR	Power Supply Rejection Ratio	I_{OUT} = 10 mA, f = 100 Hz, C_{OUT} = 2.2 μF		55		dB
		I_{OUT} = 10 mA, f = 1 kHz, C_{OUT} = 2.2 μF		54		dB
		I_{OUT} = 10 mA, f = 10 kHz, C_{OUT} = 2.2 μF		50		dB
		I_{OUT} = 10 mA, f = 1 MHz, C_{OUT} = 2.2 μF		53		dB
V_N	Output Noise Voltage	I_{OUT} = 10 mA, BW = 10Hz to 100 kHz		90		μV_{RMS}
T_{STR}	Start-up Time from EN Assertion to 0.98 × $V_{OUT\ (NOM)}$	I_{OUT}= 200 mA, C_{OUT} = 2.2 μF		680		μs
Temperature Range						
T_{SD}	Thermal Shutdown Temperature			165		ºC
	Thermal Shutdown Hysteresis			15		ºC

(1) Dropout voltage is the minimum input-to-output voltage differential needed to maintain regulation at a specified output current. In dropout, the output voltage will be equal to V_{IN} – $V_{DROPOUT}$.

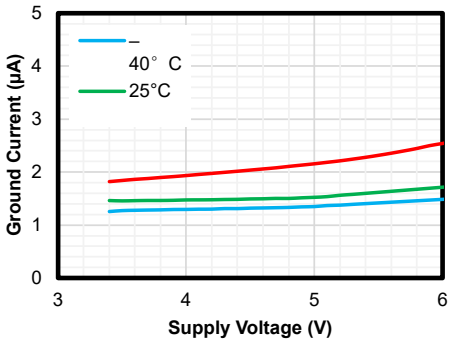
Typical Performance Characteristics

All test conditions: V_{IN} = $V_{OUT\ (NOM)}$ + 1 V or 2.4 V, whichever is greater; C_{OUT} = 2.2 μF, T_A = +25°C, unless otherwise noted.



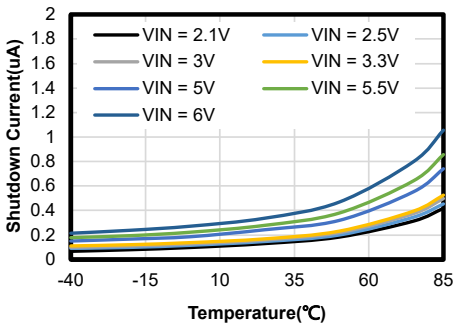
V_{OUT} = 3.3 V

Figure 1. Ground Current vs Output Current



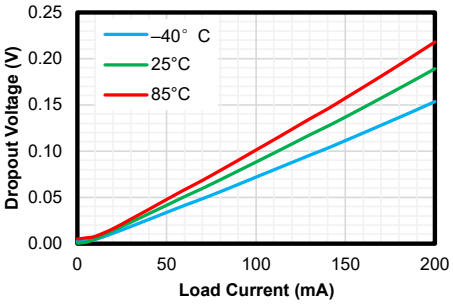
V_{OUT} = 3.3 V

Figure 2. Ground Current vs Input Voltage



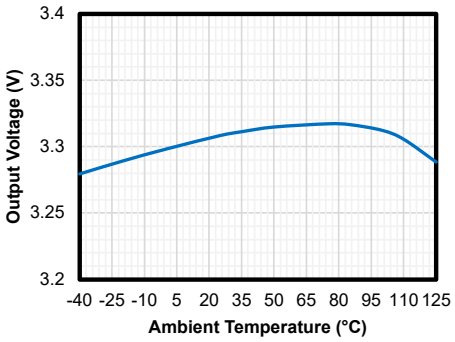
With Enable Pin

Figure 3. Shutdown Current vs Ambient Temperature



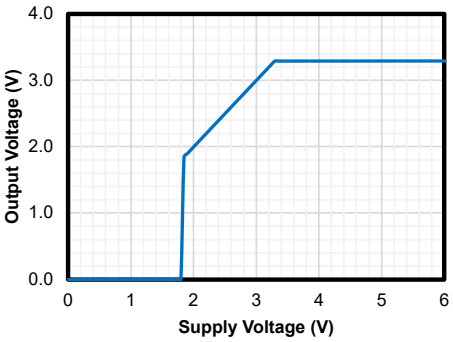
V_{OUT} = 3.3 V

Figure 4. Dropout Voltage vs Output Current



V_{OUT} = 3.3 V

Figure 5. Output Accuracy vs Ambient Temperature

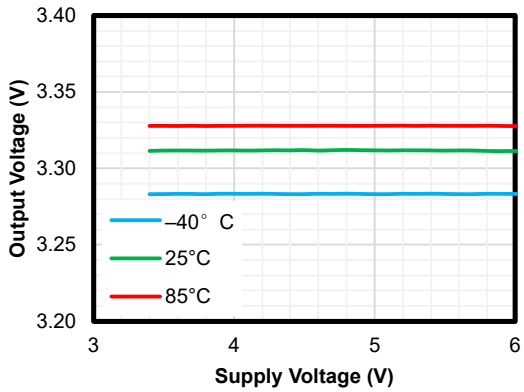


V_{OUT} = 3.3 V

Figure 6. Output Voltage vs Input Voltage

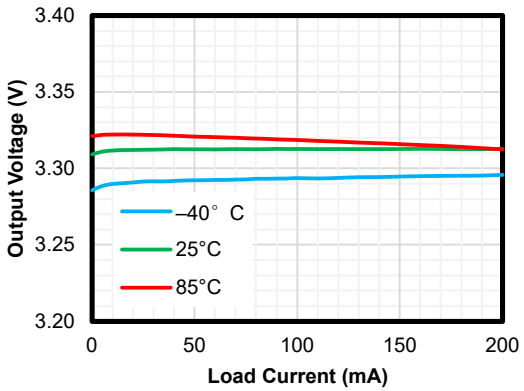
Typical Performance Characteristics (continued)

All test conditions: V_{IN} = $V_{OUT\ (NOM)}$ + 1 V or 2.4 V, whichever is greater; C_{OUT} = 2.2 μF, T_A = +25°C, unless otherwise noted.



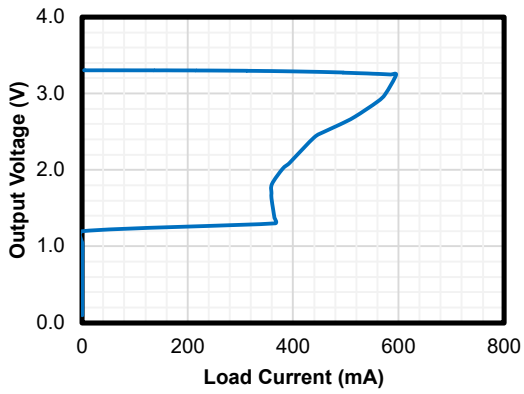
V_{OUT} = 3.3 V

Figure 7. Line Regulation



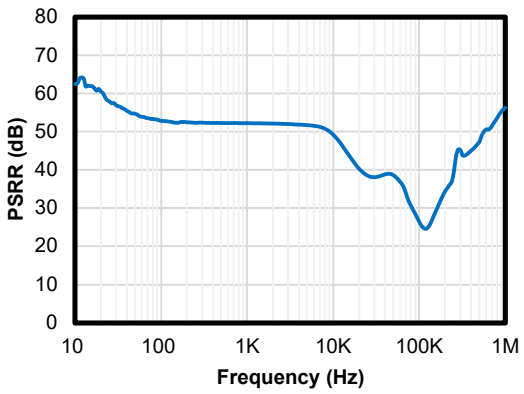
V_{OUT} = 3.3 V

Figure 8. Load Regulation



V_{OUT} = 3.3 V

Figure 9. Current Limit



V_{OUT} = 3.3 V, I_{OUT} = 10 mA, C_{OUT} = 2.2 μF

Figure 10. PSRR

Detailed Description

Overview

The TPL710 is a series of CMOS process low Iq linear regulators with ultra-low quiescent power consumption. The TPL710 series supports a maximum 200-mA output current, with typically only 1.4-μA quiescent current. TPL710 series is stable with a low-ESR small ceramic output capacitor from 2.2 μF to 10 μF. The TPL710 series is available in fixed voltage versions of 1 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 2.8 V, 3 V, 3.3 V, and 3.6 V.

Functional Block Diagram

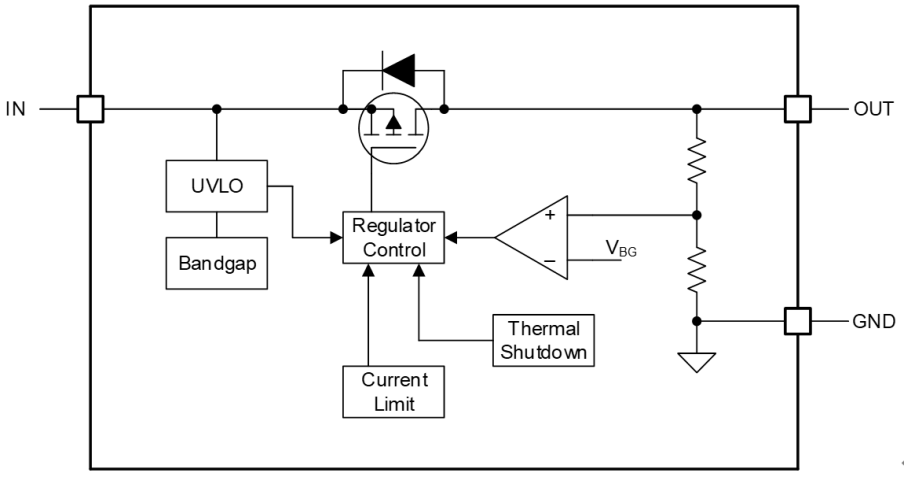


Figure 11. TPL710 Series without Enable Pin

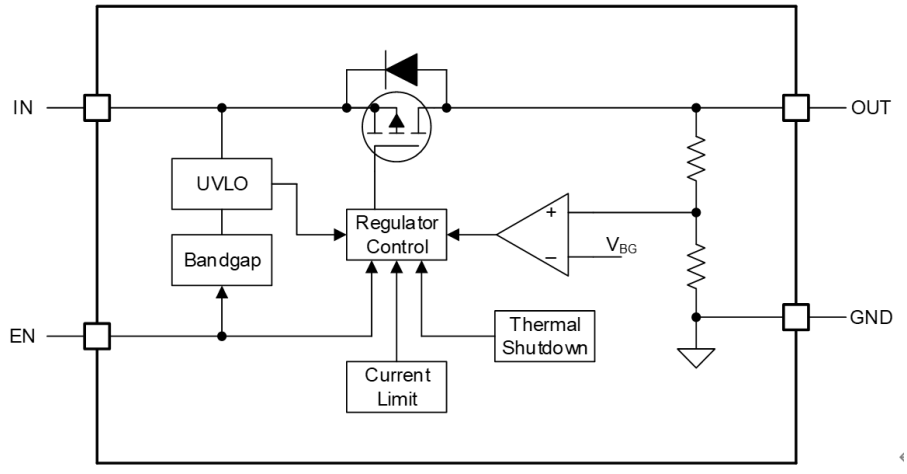


Figure 12. TPL710 Series with Enable Pin

Feature Description

Enable (4-/5-Pin Package Only)

The enable pin (EN) is active high. Connect this pin to the GPIO of an external processor or digital logic control circuit to enable and disable the device, or connect this pin to the IN pin for self-bias applications.

Under-voltage Lockout (UVLO)

Enable (4-/5-Pin Package Only) The enable pin (EN) is active high. Connect this pin to the GPIO of an external processor or digital logic control circuit to enable and disable the device. Or connect this pin to the IN pin for self-bias applications.

Regulated Output Voltage

The TPL710 series is in fixed voltage versions of 1V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 2.8 V, 3 V, 3.3 V, and 3.6 V. When the input voltage is higher than $V_{OUT\ (NOM)}$+ V_{DO}or 2.4 V, the output pin is the regulated output based on the selected voltage version. When the input voltage falls below $V_{OUT\ (NOM)}$+ V_{DO}or 2.4 V, the output pin tracks the input voltage minus the dropout voltage based on the load current. When the input voltage drops below the UVLO threshold, the output keeps shutting off.

Current Limit

The TPL710 series integrates an internal current limit that helps protect the regulator during fault conditions. When the output is overloaded or shorted to ground, the LDO supplies output current with limited value to prevent the regulator from being damaged. The output voltage is not regulated when the device is in current limit mode, and the value is $V_{OUT} = I_{CL} \times R_{LOAD}$

Thermal Shutdown

During normal operation, the LDO junction temperature should not exceed 125°C. When the junction temperature exceeds the thermal shutdown threshold, the LDO shuts down the output immediately. Until the junction temperature falls below the thermal shutdown threshold minus thermal shutdown hysteresis, the output turns on again.

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPL710 is a series of 200-mA high PSRR, low-dropout linear regulators with low quiescent current. The following application schematic shows a typical usage of the TPL710 series.

Typical Application

Figure 13 shows the typical application schematic of the TPL710 series.

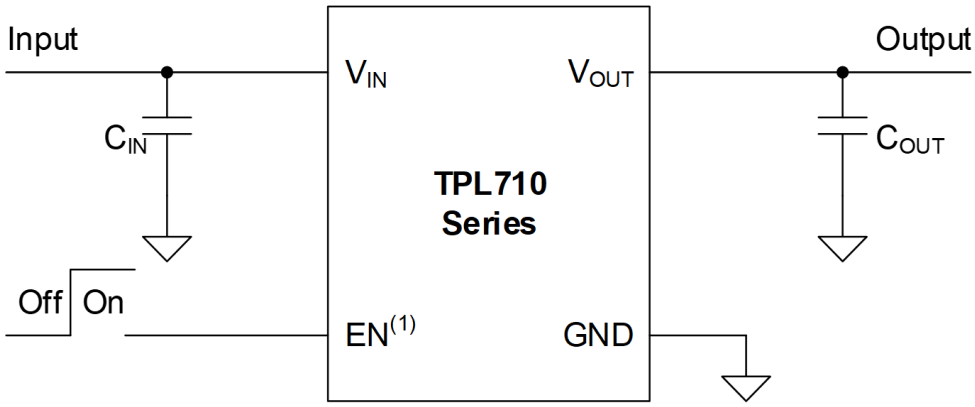


Figure 13. TPL710 Series Application Schematic

(1) EN pin is only available in the 4-/5-pin package

Input Capacitor and Output Capacitor

3PEAK recommends adding a 1 μF or greater capacitor with a 0.1-μF bypass capacitor in parallel at IN pin to keep the input voltage stable. The voltage rating of the capacitors must be greater than the maximum input voltage.

To ensure loop stability, the TPL710 series requires an output capacitor with a minimum effective capacitance value of 1 μF. 3PEAK recommends selecting an X5R- or X7R-type 2.2 μF or larger ceramic capacitor with low ESR over temperature.

Both input capacitors and output capacitors must be placed as close to the device pins as possible.

Power Dissipation

During normal operation, the LDO junction temperature should not exceed 125°C. Use the below equations to calculate the power dissipation and estimate the junction temperature.

The power dissipation can be calculated using Equation 1.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad (1)$$

The junction temperature can be estimated using Equation 2. θ_{JA} is the junction-to-ambient thermal resistance (See Section *Thermal Information*).

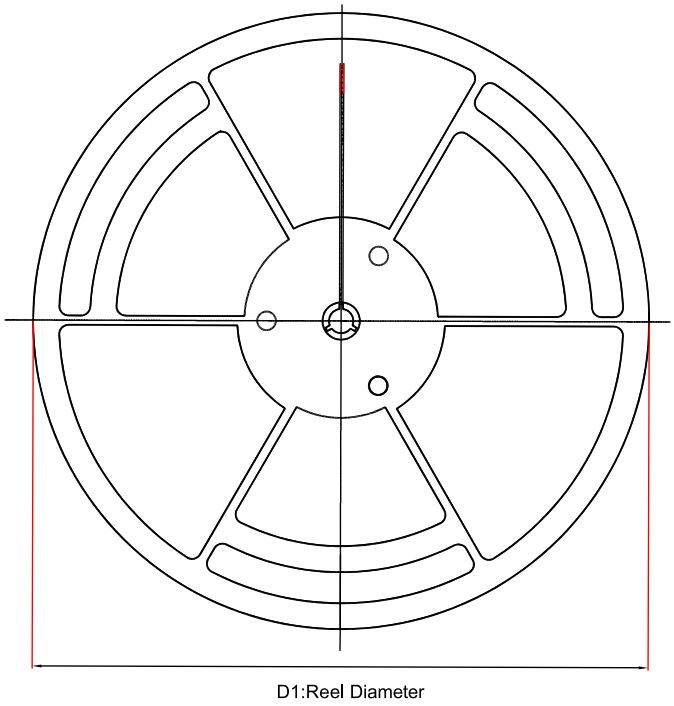
$$I_J = I_A + P_D \times \theta_{JA} \quad (2)$$

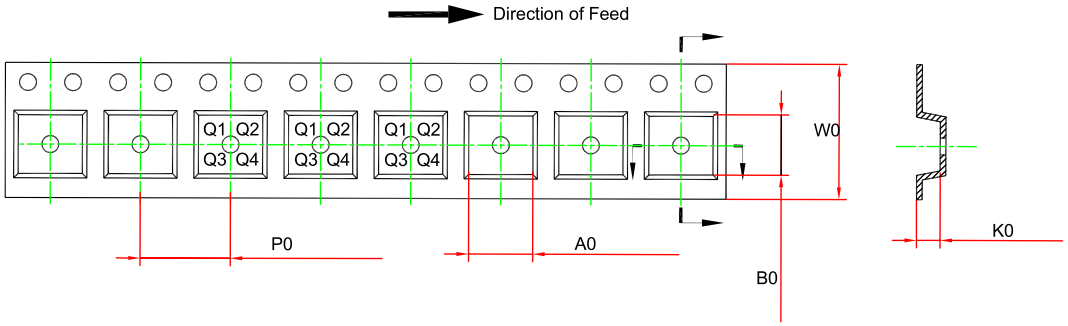
Layout

Layout Guideline

- Both input and output capacitors must be placed as close to the device pins as possible.
- It is recommended to bypass the input pin to the ground with a 0.1-μF bypass capacitor. The loop area formed by the bypass capacitor connection, the IN pin, and the GND pin of the system must be as small as possible.
- It is recommended to use wide and thick copper to minimize I×R drop and heat dissipation.

Tape and Reel Information





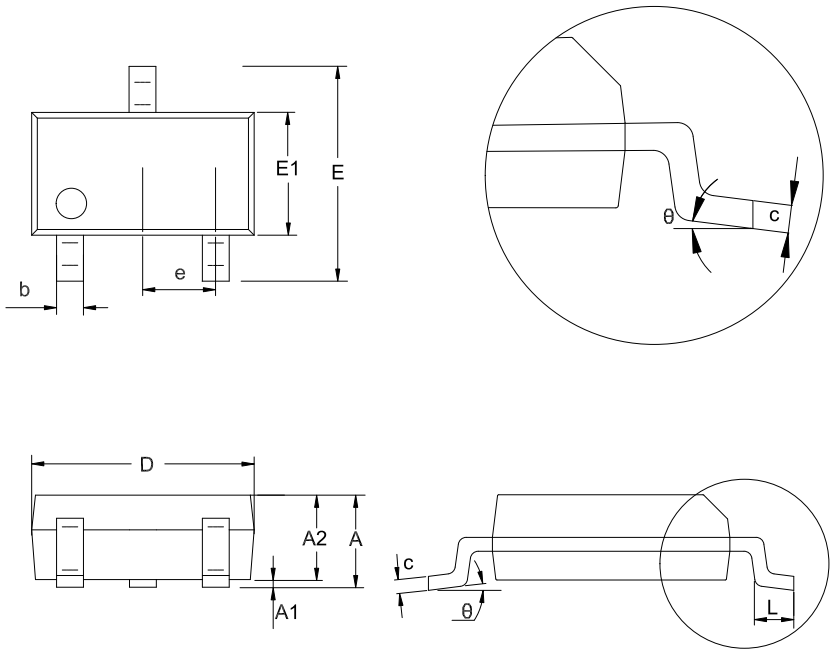
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPL710Fxx-3TR	SOT23-3	180	13.1	3.18	3.28	1.32	4	8	Q3
TPL710Fxx-5TR	SOT23-5	180	13.1	3.2	3.2	1.4	4	8	Q3
TPL710F33-FR	DFN1x1-4	180	10	1.16	1.16	0.5	2	8	Q2
TPL710Fxx-FR (1)	DFN1x1-4	180	10	1.16	1.16	0.5	2	8	Q1

(1) Output voltage value, xx = 10 to 36, e.g., 36 means 3.6 V output voltage. **NOTE: 33 IS NOT INCLUDED**

Package Outline Dimensions

SOT23-3

Package Outline Dimensions S3T(SOT23-3-A)



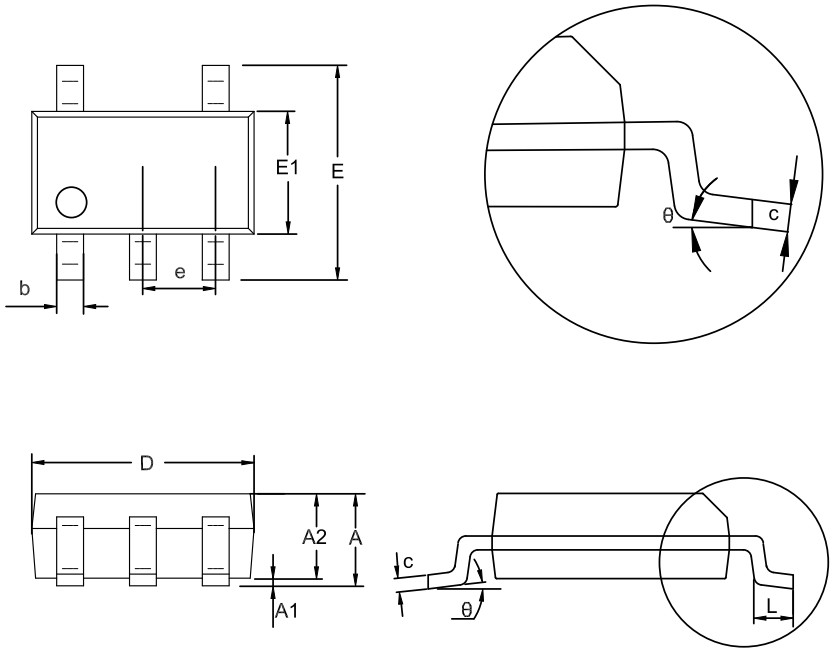
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.150	0.000	0.006
A2	1.000	1.200	0.039	0.047
b	0.280	0.500	0.011	0.020
c	0.100	0.230	0.004	0.009
D	2.820	3.020	0.111	0.119
E	2.600	3.000	0.102	0.118
E1	1.500	1.720	0.059	0.068
e	0.950 BSC		0.037 BSC	
L	0.300	0.600	0.012	0.024
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

SOT23-5

Package Outline Dimensions S5T(SOT23-5-A)



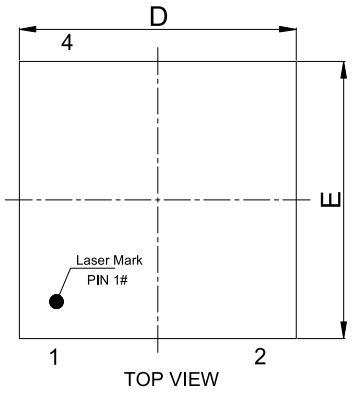
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.150	0.000	0.006
A2	1.000	1.200	0.039	0.047
b	0.280	0.500	0.011	0.020
c	0.100	0.230	0.004	0.009
D	2.820	3.020	0.111	0.119
E	2.600	3.000	0.102	0.118
E1	1.500	1.720	0.059	0.068
e	0.950 BSC		0.037 BSC	
L	0.300	0.600	0.012	0.024
θ	0	8°	0	8°

NOTES

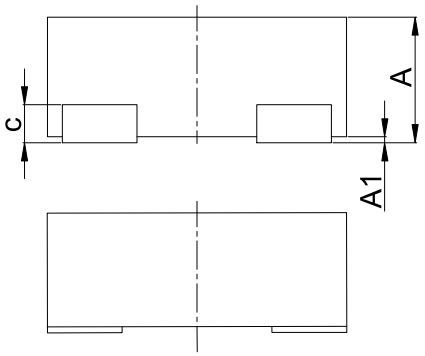
1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

DFN1X1-4

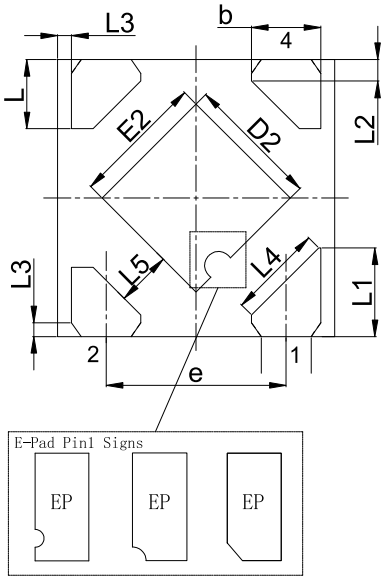
Package Outline Dimensions DF1(DFN1X1-4-A)



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.350	0.400	0.014	0.016
A1	0.000	0.050	0.000	0.002
b	0.200	0.300	0.008	0.012
c	0.070	0.170	0.003	0.007
D	0.950	1.050	0.037	0.041
D2	0.430	0.530	0.017	0.021
E	0.950	1.050	0.037	0.041
E2	0.430	0.530	0.017	0.021
e	0.650 BSC		0.026 BSC	
L	0.200	0.300	0.008	0.012
L1	0.270	0.370	0.011	0.015
L2	0.077 BSC		0.003 BSC	
L3	0.050 BSC		0.002 BSC	
L4	0.340 BSC		0.013 BSC	
L5	0.200 BSC		0.008 BSC	

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Order Information

Order Number	Junction Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPL710F10-3TR	−40 to 125°C	SOT23-3	L3C	MSL3	Tape and Reel, 3,000	Green
TPL710F12-3TR	−40 to 125°C	SOT23-3	L3D	MSL3	Tape and Reel, 3,000	Green
TPL710F15-3TR (1)	−40 to 125°C	SOT23-3	L3E	MSL3	Tape and Reel, 3,000	Green
TPL710F18-3TR	−40 to 125°C	SOT23-3	L3F	MSL3	Tape and Reel, 3,000	Green
TPL710F25-3TR	−40 to 125°C	SOT23-3	L3G	MSL3	Tape and Reel, 3,000	Green
TPL710F28-3TR	−40 to 125°C	SOT23-3	L3H	MSL3	Tape and Reel, 3,000	Green
TPL710F30-3TR	−40 to 125°C	SOT23-3	L3I	MSL3	Tape and Reel, 3,000	Green
TPL710F33-3TR	−40 to 125°C	SOT23-3	L3J	MSL3	Tape and Reel, 3,000	Green
TPL710F36-3TR (1)	−40 to 125°C	SOT23-3	L3K	MSL3	Tape and Reel, 3,000	Green
TPL710F10-5TR	−40 to 125°C	SOT23-5	L3C	MSL3	Tape and Reel, 3,000	Green
TPL710F12-5TR	−40 to 125°C	SOT23-5	L3D	MSL3	Tape and Reel, 3,000	Green
TPL710F15-5TR	−40 to 125°C	SOT23-5	L3E	MSL3	Tape and Reel, 3,000	Green
TPL710F18-5TR	−40 to 125°C	SOT23-5	L3F	MSL3	Tape and Reel, 3,000	Green
TPL710F25-5TR	−40 to 125°C	SOT23-5	L3G	MSL3	Tape and Reel, 3,000	Green
TPL710F28-5TR	−40 to 125°C	SOT23-5	L3H	MSL3	Tape and Reel, 3,000	Green
TPL710F30-5TR	−40 to 125°C	SOT23-5	L3I	MSL3	Tape and Reel, 3,000	Green
TPL710F33-5TR	−40 to 125°C	SOT23-5	L3J	MSL3	Tape and Reel, 3,000	Green
TPL710F36-5TR (1)	−40 to 125°C	SOT23-5	L3K	MSL3	Tape and Reel, 3,000	Green
TPL710F10-FR	−40 to 125°C	DFN1x1-4	L3C	MSL3	Tape and Reel, 12,000	Green
TPL710F12-FR	−40 to 125°C	DFN1x1-4	L3D	MSL3	Tape and Reel, 12,000	Green

Order Number	Junction Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPL710F15-FR (1)	−40 to 125°C	DFN1x1-4	L3E	MSL3	Tape and Reel, 12,000	Green
TPL710F18-FR	−40 to 125°C	DFN1x1-4	L3F	MSL3	Tape and Reel, 12,000	Green
TPL710F25-FR	−40 to 125°C	DFN1x1-4	L3G	MSL3	Tape and Reel, 12,000	Green
TPL710F28-FR	−40 to 125°C	DFN1x1-4	L3H	MSL3	Tape and Reel, 12,000	Green
TPL710F30-FR	−40 to 125°C	DFN1x1-4	L3I	MSL3	Tape and Reel, 12,000	Green
TPL710F33-FR	−40 to 125°C	DFN1x1-4	L3J	MSL3	Tape and Reel, 12,000	Green
TPL710F36-FR (1)	−40 to 125°C	DFN1x1-4	L3K	MSL3	Tape and Reel, 12,000	Green

(1) For future product, contact the 3PEAK factory for more information and samples.

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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