20-V/300-mA Wide-input High-PSRR Ultra-low Noise LDO Regulator

Features

- Qualified for Automotive Applications
  - AEC-Q100 Grade 1, T_A: −40°C to +125°C
- Input Voltage Range: 2.5 V to 20 V
- Output Voltage Range:
  - Adjustable Output: 1.22 V to 18 V
- ±2% Output Accuracy Over Line Regulation, Load Regulation, and Operating Temperature Range
- 300-mA Maximum Output Current
- Low Dropout Voltage: 600 mV Maximum at 300 mA
- High PSRR:
  - 96 dB at 1 kHz
  - 71 dB at 100 kHz
  - 51 dB at 1 MHz
- 5.2-μVRMS Output Voltage Noise
- Excellent Transient Response
- Stable with ≥ 2.2-μF Low ESR Ceramic Output Capacitor
- Integrated Protection:
  - Over-current Protection
  - Over-temperature Protection
- ESOP8 Package

Applications

- Automotive Surround View Camera
- High-definition Imaging System
- Infrared Image Equipment

Description

The TPL8032Q product is a 300-mA high PSRR, ultra-low noise, low dropout linear regulator with 20-V wide input voltage range. The TPL8032Q product supports adjustable output voltage ranging from 1.22 V to 18 V with an external resistor divider and is stable with a 2.2-μF or larger ceramic output capacitor.

The TPL8032Q product features high PSRR with 96 dB at 1 kHz and 5.2-μVRMS ultra-low noise. These features make the TPL8032Q product suitable for noise-sensitive applications with large ripple and noise generated from the previous stage power supply, such as high-performance analog devices or high-definition imaging equipment. The output shortage protection and thermal overload-protection circuits improve the reliability under heavy load conditions.

The TPL8032Q product provides a thermal-enhanced ESOP8 package with guaranteed operating ambient temperature ranging from −40°C to +125°C.

Typical Application Circuit

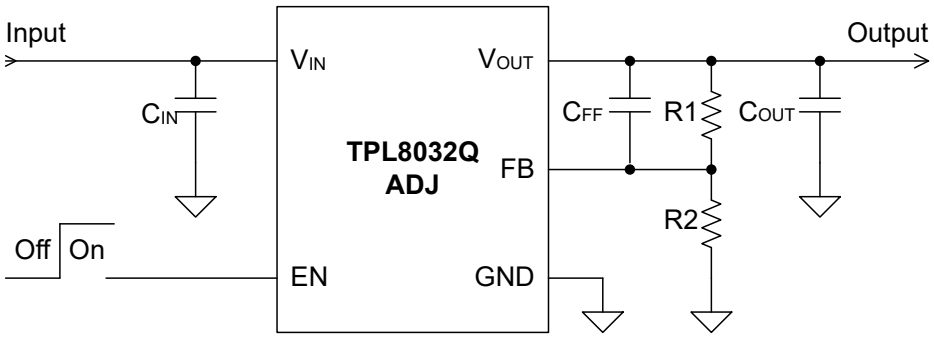


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Product Family Table

Order Number	Output Voltage (V)	Package
TPL8032ADQ-ES1R-S	Adjustable (1.22 V to 18 V)	ESOP8

Revision History

Date	Revision	Notes
2021-12-31	Rev.Pre.0	Preliminary Revision.
2022-11-30	Rev.A.0	Initial Released.
2023-05-31	Rev.A.1	Corrected X-axis Title of Figure 9, Figure 10, Figure 11 and Figure 12.
2023-10-10	Rev.A.2	Added the Tolerance of V_{FB}.
2024-02-20	Rev.A.3	Removed Output Reverse Current Protection Feature.

Pin Configuration and Functions

TPL8032Q-S
ESOP8 Package
Top View

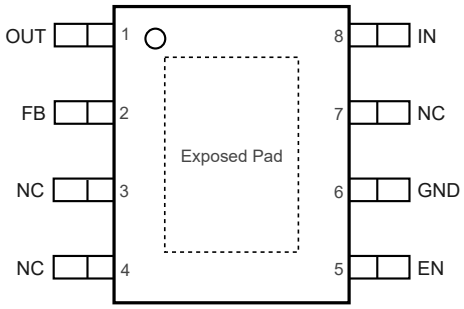


Table 1. Pin Functions: TPL8032Q-S

Pin No.	Pin Name	I/O	Description
5	EN	I	Regulator enable pin. Drive EN high to turn on the regulator; and drive EN low to turn off the regulator.
2	FB	I	Output voltage feedback pin. Connect to a resistor divider to adjust the output voltage.
6	GND	−	Ground reference pin. Connect the GND pin to PCB ground plane directly.
8	IN	I	Input voltage pin.
3, 4, 7	NC	−	No connection.
1	OUT	O	Regulated output voltage pin.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
EN, IN		−0.3	24	V
OUT		−0.3	24	V
FB		−0.3	6	V
T_J	Junction Temperature Range	−40	150	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	AEC Q100-002	±2	kV
CDM	Charged Device Model ESD	AEC Q100-011	±1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Max	Unit
IN		2.5	20	V
EN		0	V_{IN}	V
COUT		2.2		μF
ESR		1	100	mΩ
T_A	Ambient Temperature Range	−40	125	°C
T_J	Junction Temperature Range	−40	150	°C

Thermal Information

Package Type	θ_{JA}	$\theta_{JC,top}$	$\theta_{JC,bottom}$	Unit
ESOP8	39.6	83.1	14.3	°C/W

Electrical Characteristics

All test conditions: V_{IN} = $V_{IN,MIN}$ = $V_{OUT(NOM)}$ + 1 V or 2.5 V, whichever is greater, −40°C ≤ T_A ≤ +125°C; typically, V_{OUT} = 5 V, C_{IN} = 10 µF, C_{OUT} = 4.7 µF, and C_{FF} = 100 nF for adjustable output, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply Input Voltage and Current						
V_{IN}	Input Supply Voltage Range (1)		$V_{IN,MIN}$		20	V
UVLO	Input Supply Voltage Rising			2.25	2.4	V
	Hysteresis			0.2		V
I_{GND}	Ground Pin Current	I_{OUT} = 0 mA		96	160	µA
		I_{OUT} = 10 mA		450		µA
I_{SHDN}	Shutdown Current	EN = GND		2	8	µA
Enable Input Voltage and Current						
$V_{IH(EN)}$	EN Input High Level (Enable)		1.6		V_{IN}	V
$V_{IL(EN)}$	EN Input Low Level (Disable)		0		0.5	V
I_{EN}	EN Pin Leakage Current	V_{EN} = 0 V to 20 V		0.5	1	µA
Regulated Output Voltage and Current						
V_{OUT}	Output Voltage Accuracy (2)	I_{OUT} = 1 mA to 300 mA	−2%		2%	
V_{FB}	Feedback Pin Voltage		1.196	1.22	1.245	V
I_{FB}	FB Input Current	Force V_{FB} = 1.5 V	–100		100	nA
ΔV_{OUT}	Line Regulation	V_{IN} = $V_{IN,MIN}$ to 20 V, I_{OUT} = 1 mA		0.007		%/V
	Load Regulation	V_{IN} = $V_{IN,MIN}$, I_{OUT} = 1 mA to 300 mA		0.01		%/mA
V_{DO}	Dropout Voltage (3)	I_{OUT} = 100 mA		125	200	mV
		I_{OUT} = 200 mA		250	400	mV
		I_{OUT} = 300 mA		375	600	mV
I_{OUT}	Output Voltage	V_{OUT} in regulation	0		300	mA
I_{LIM}	Output Current Limit	V_{OUT} = 0.9 × $V_{OUT(NOM)}$	310	450	650	mA
I_{SC}	Short-Circuit to Ground Current Limit	V_{OUT} is forced to GND, T_J = 25°C		180		mA
PSRR	Power Supply Rejection Ratio	C_{OUT} = 2.2 µF, C_{FF} = 100 nF, I_{OUT} = 100 mA, f = 120 Hz		88		dB
		C_{OUT} = 2.2 µF, C_{FF} = 100 nF, I_{OUT} = 100 mA, f = 1 kHz		96		dB
		C_{OUT} = 2.2 µF, C_{FF} = 100 nF, I_{OUT} = 100 mA, f = 100 kHz		71		dB
		C_{OUT} = 2.2 µF, C_{FF} = 100 nF, I_{OUT} = 100 mA, f = 1 MHz		51		dB

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_N	Output Noise Voltage	C_{OUT} = 2.2 μF, C_{FF} = 100 nF, I_{OUT} = 100 mA, BW = 10 Hz to 100 kHz		5.2		μVRMS
Temperature Range						
T_{SD}	Thermal Shutdown Temperature Threshold			160		ºC
	Hysteresis			20		ºC

(1) $V_{IN,MIN}$ = $V_{OUT(NOM)}$ + 1 V or 2.5 V, whichever is greater.
(2) Tolerance of external resistor is not included.
(3) Dropout voltage is the minimum input to the output voltage differential needed to maintain regulation at a specified output current and measure for $V_{OUT(NOM)}$ ≥ 3.3 V. In the dropout mode, the output voltage will be equal to: V_{IN} − V_{DO}.

Typical Performance Characteristics

All test conditions: V_{IN} = $V_{OUT(NOM)}$ + 1 V or 2.5 V, whichever is greater, −40°C ≤ T_A ≤ +125°C; typically, V_{OUT} = 5 V, C_{IN} = 10 µF, C_{OUT} = 2.2 µF, and C_{FF} = 100 nF for adjustable output, unless otherwise noted.

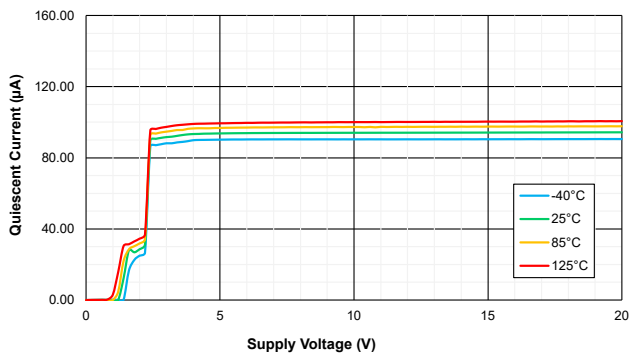


Figure 1. Quiescent Current vs Supply Voltage

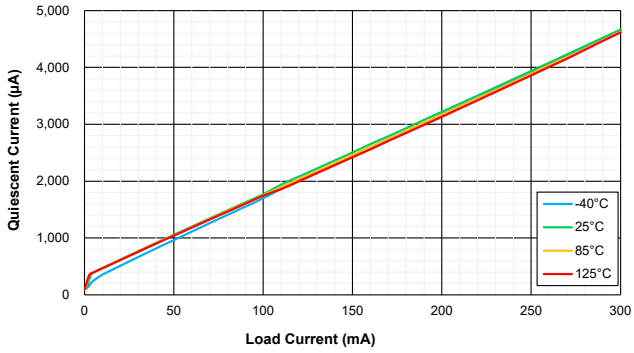


Figure 2. Quiescent Current vs Load Current

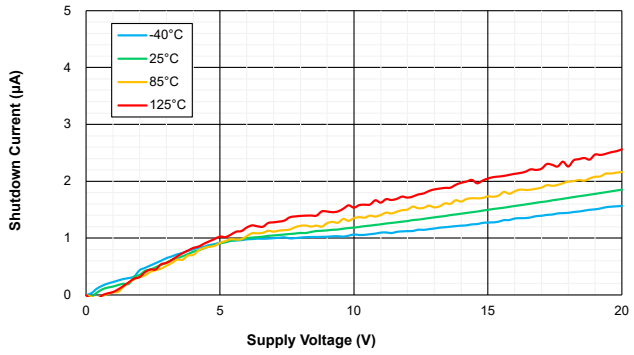
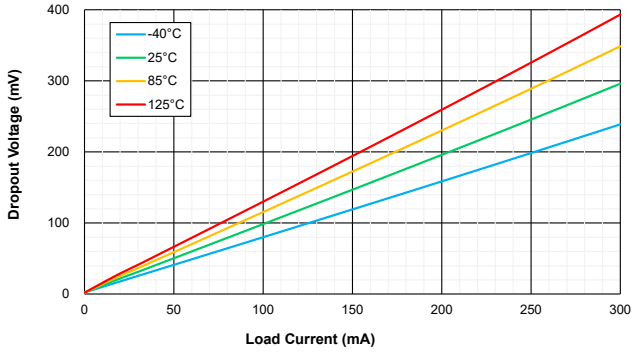
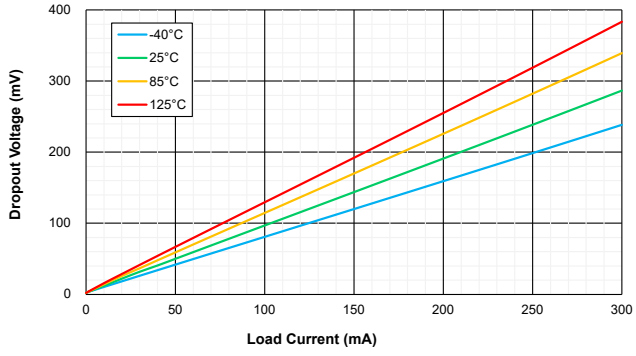


Figure 3. Shutdown Current vs Supply Voltage



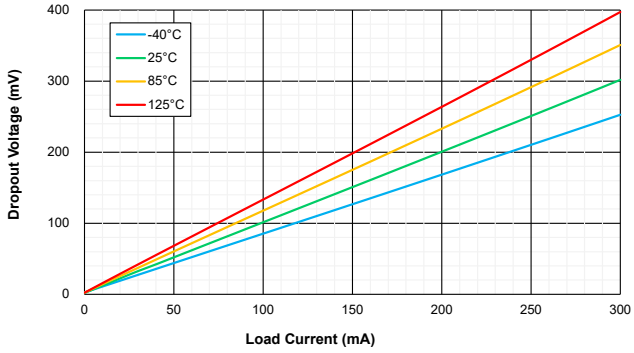
V_{OUT} = 5 V

Figure 4. Dropout Voltage vs Load Current



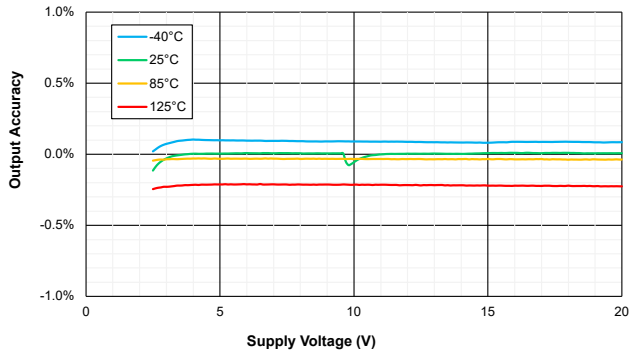
V_{OUT} = 10 V

Figure 5. Dropout Voltage vs Load Current



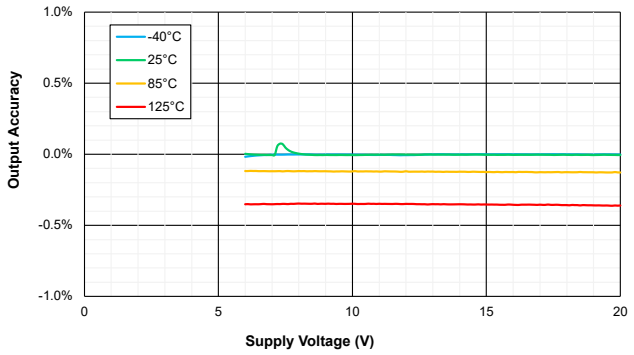
V_{OUT} = 18 V

Figure 6. Dropout Voltage vs Load Current



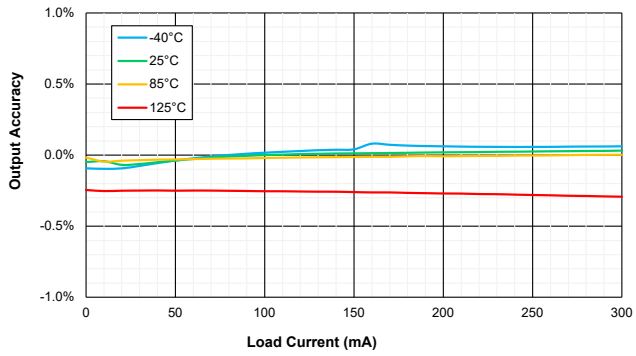
V_{OUT} = 1.22 V

Figure 7. Line Regulation



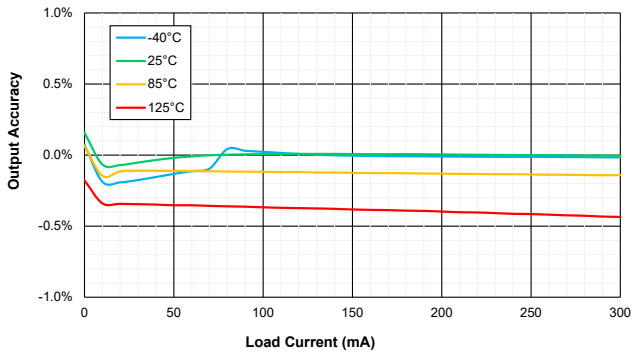
V_{OUT} = 5 V

Figure 8. Line Regulation



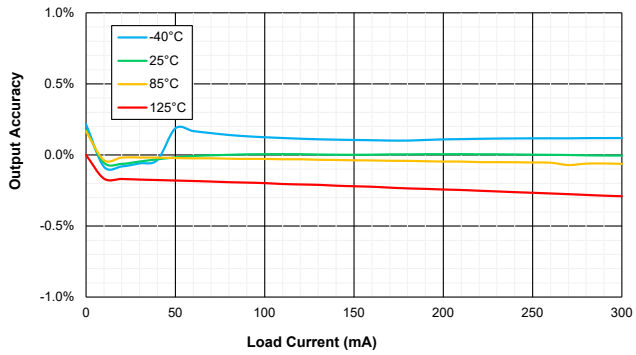
V_{OUT} = 1.22 V

Figure 9. Load Regulation



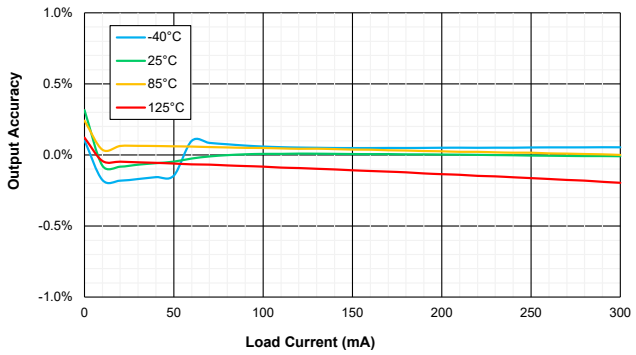
V_{OUT} = 5 V

Figure 10. Load Regulation



V_{OUT} = 10 V

Figure 11. Load Regulation



V_{OUT} = 18 V

Figure 12. Load Regulation

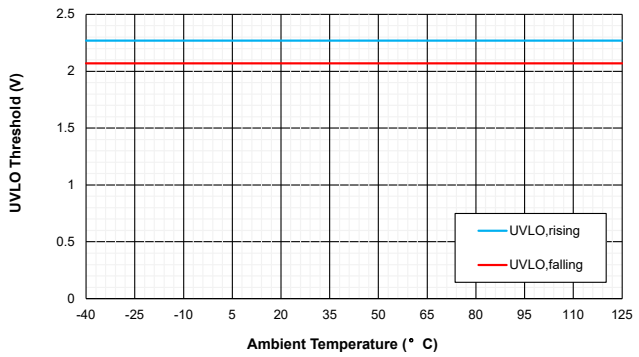


Figure 13. UVLO

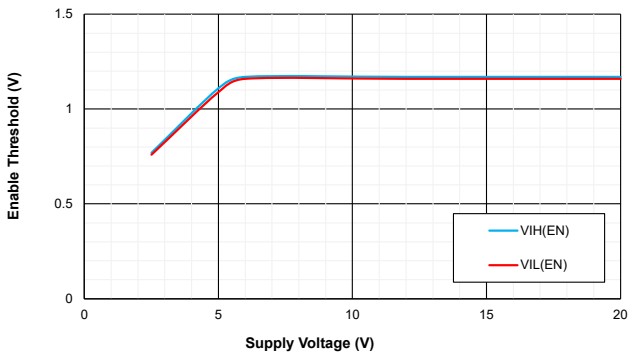


Figure 14. EN Threshold

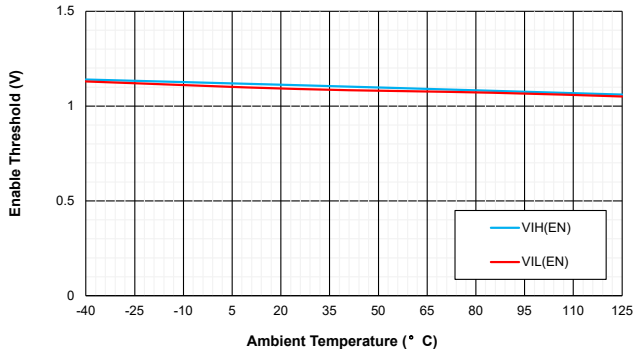
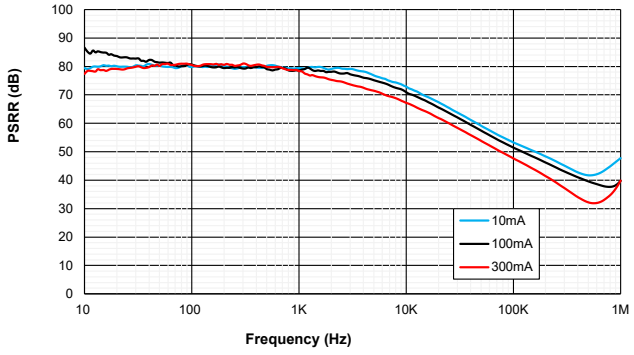
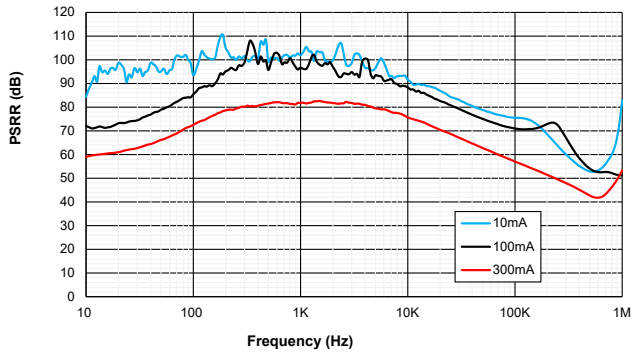


Figure 15. EN Threshold



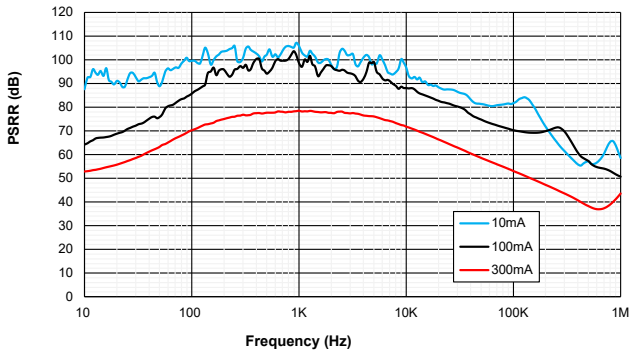
V_{OUT} = 1.22 V

Figure 16. PSRR



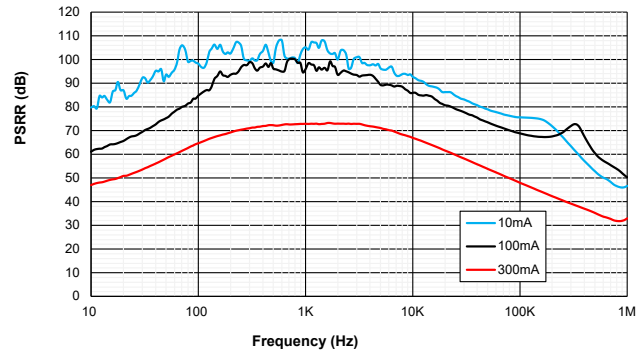
V_{OUT} = 5 V

Figure 17. PSRR



V_{OUT} = 10 V

Figure 18. PSRR



V_{OUT} = 18 V

Figure 19. PSRR

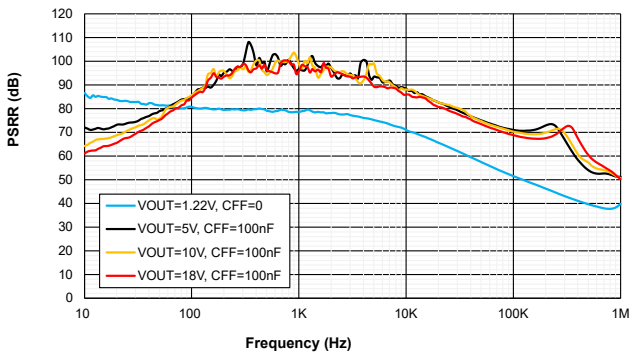
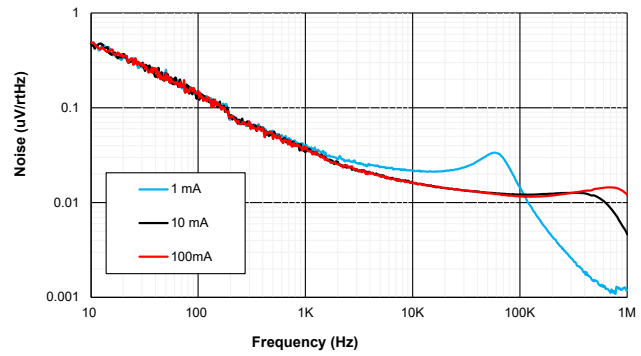
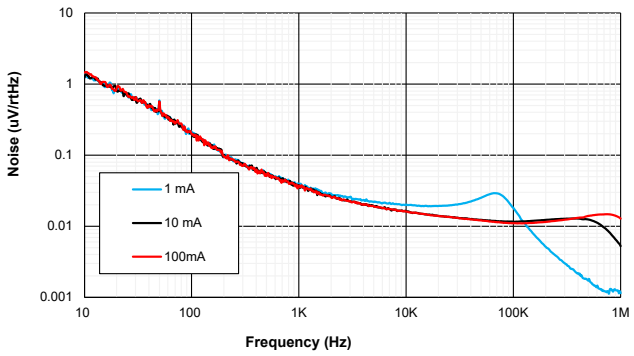


Figure 20. PSRR



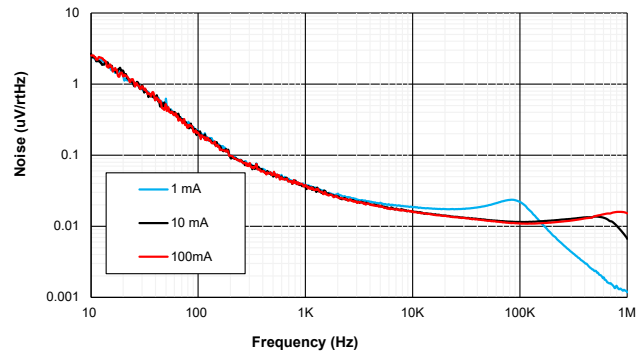
V_{OUT} = 1.22 V

Figure 21. Noise



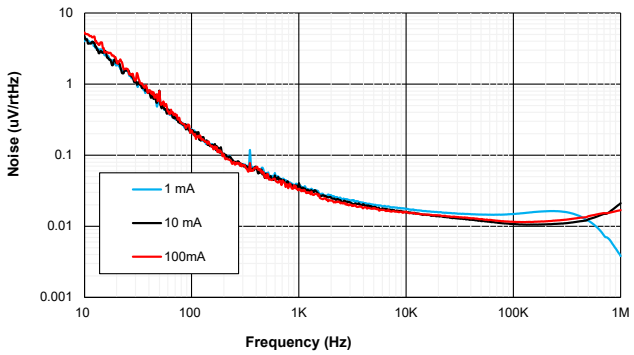
V_{OUT} = 5 V

Figure 22. Noise



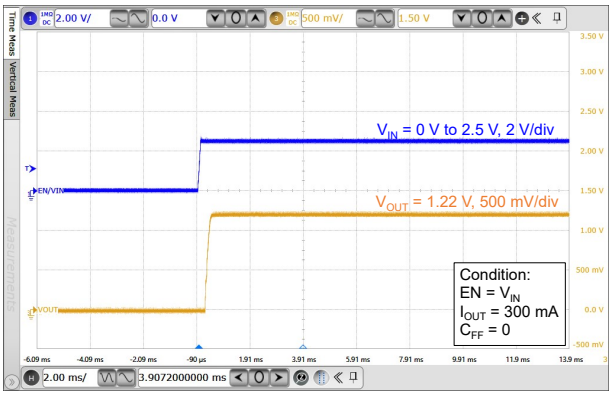
V_{OUT} = 10 V

Figure 23. Noise



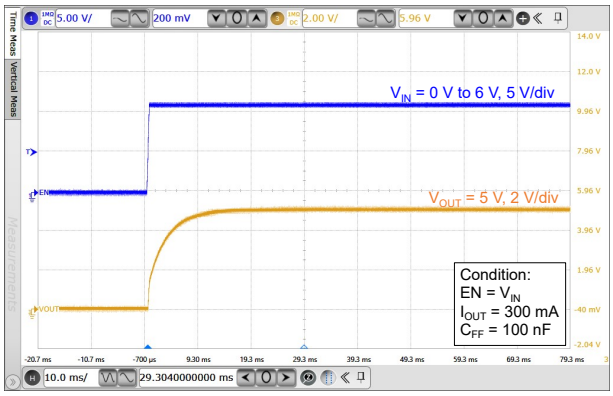
V_{OUT} = 18 V

Figure 24. Noise



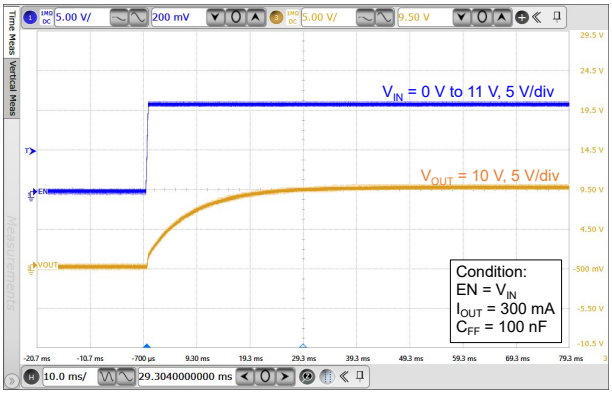
V_{OUT} = 1.22 V

Figure 25. Startup with V_{IN}



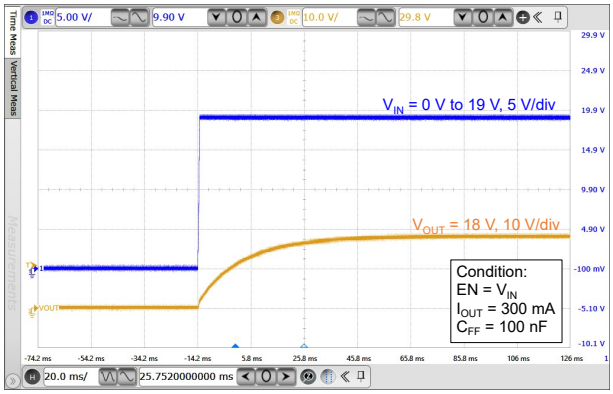
V_{OUT} = 5 V

Figure 26. Startup with V_{IN}



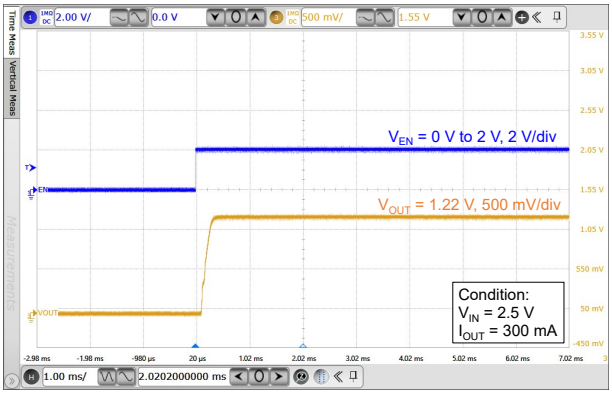
V_{OUT} = 10 V

Figure 27. Startup with V_{IN}



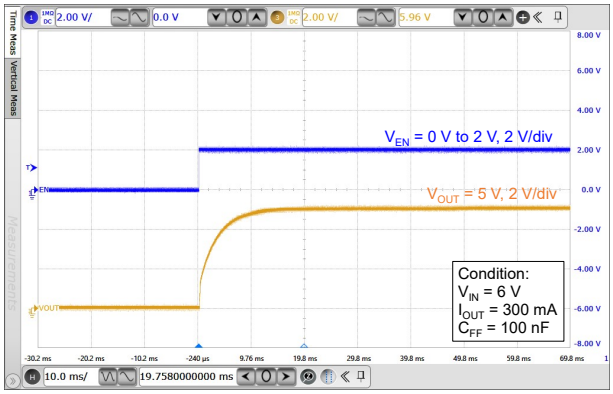
V_{OUT} = 18 V

Figure 28. Startup with V_{IN}



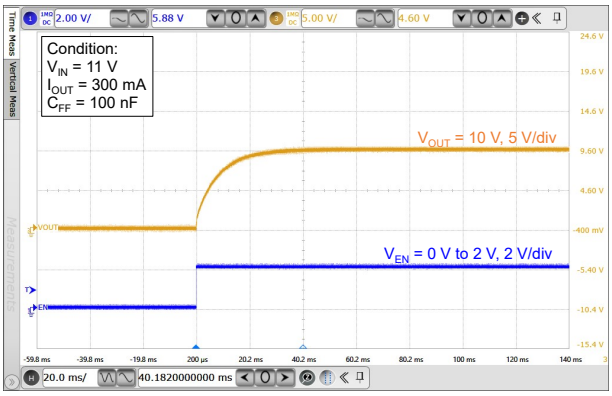
V_{OUT} = 1.22 V

Figure 29. Startup with V_{EN}



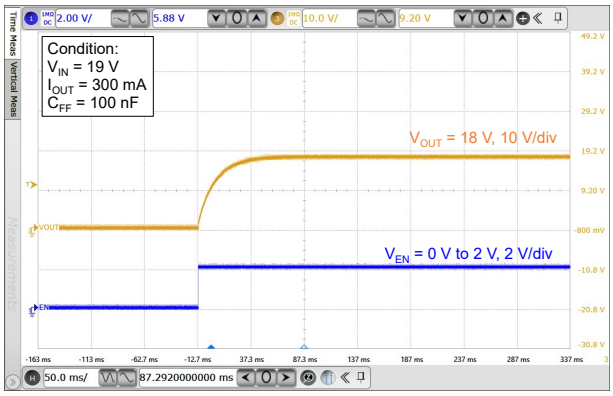
V_{OUT} = 5 V

Figure 30. Startup with V_{EN}



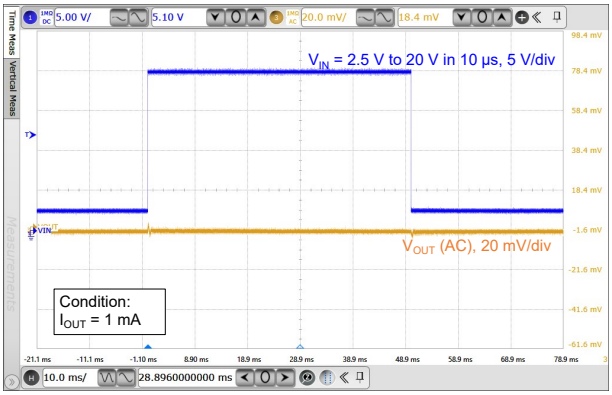
V_{OUT} = 10 V

Figure 31. Startup with V_{EN}



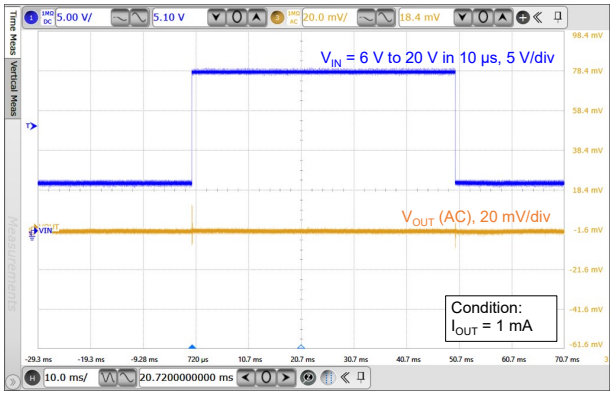
V_{OUT} = 18 V

Figure 32. Startup with V_{EN}



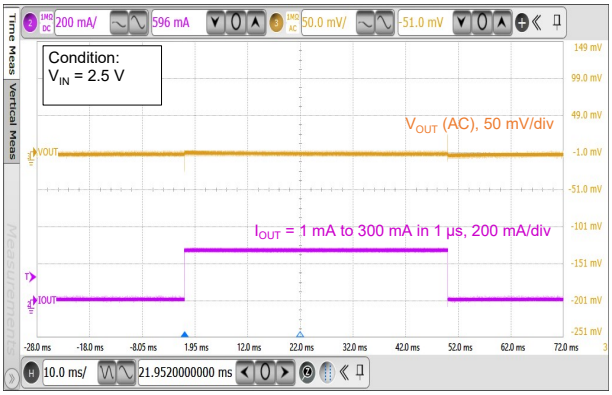
V_{OUT} = 1.22 V

Figure 33. Line Transient



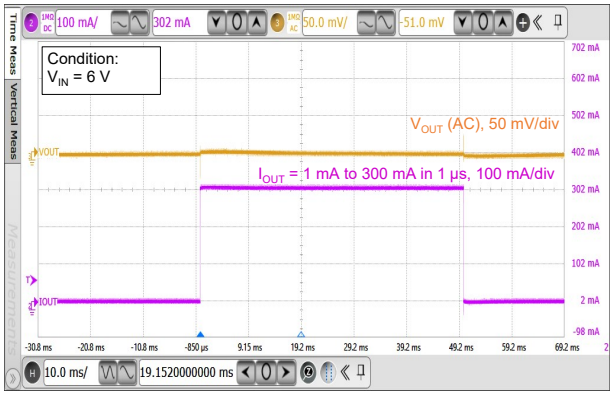
V_{OUT} = 5 V

Figure 34. Line Transient



V_{OUT} = 1.22 V

Figure 35. Load Transient



V_{OUT} = 5 V

Figure 36. Load Transient

Detailed Description

Overview

The TPL8032Q product is a 300-mA high PSRR, ultra-low noise, low dropout linear regulator with 20-V wide input voltage range. The TPL8032Q product supports adjustable output voltage ranging from 1.22 V to 18 V with an external resistor divider and is stable with a 2.2-μF or larger ceramic output capacitor.

The TPL8032Q product features high PSRR with 96 dB at 1 kHz and 5.2-μVRMS ultra-low noise. These features make the TPL8032Q product suitable for noise-sensitive applications with large ripple and noise generated from the previous stage power supply, such as high-performance analog devices or high-definition imaging equipment. Output shortage protection and thermal overload-protection circuits improve the reliability under heavy load conditions.

Functional Block Diagram

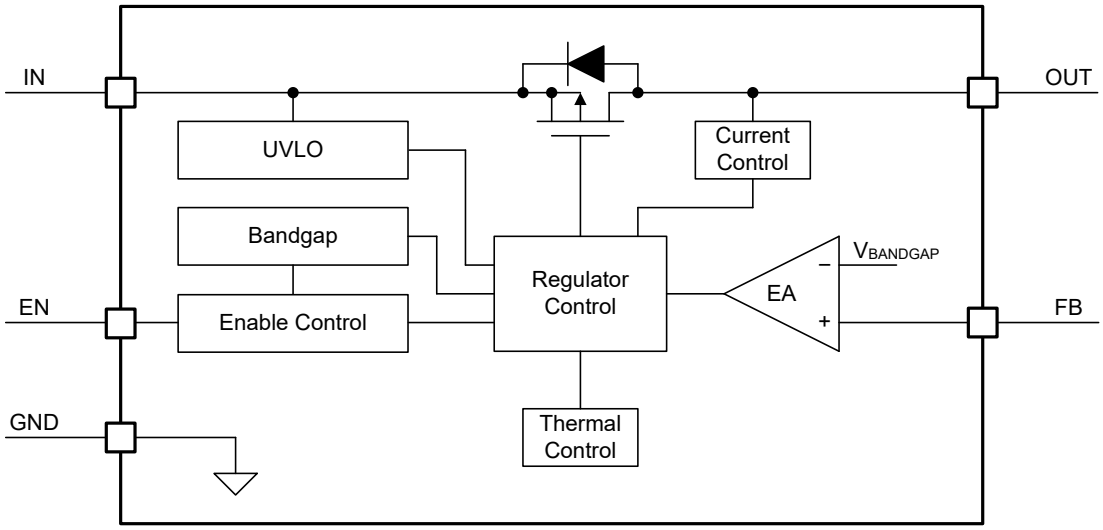


Figure 37. Functional Block Diagram

Feature Description

Enable (EN)

The enable pin (EN) is active high. Connect this pin to the GPIO of an external processor or digital logic control circuit to enable and disable the device. Or connect this pin to the IN pin for self-bias applications.

Under-Voltage Lockout (UVLO)

The TPL8032Q product uses an under-voltage lockout circuit to keep the output shut off until the internal circuitry operates properly. Refer to the Electrical Characteristics table for UVLO threshold and hysteresis.

Adjustable Output Voltage (FB and OUT)

The output voltage range of the TPL8032Q product can be set from 1.22 V to 18 V by selecting different external resistors. Use the Equation 1 to calculate the output voltage.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right) \quad (1)$$

Where, the feedback voltage V_{FB} is 1.22 V.

Over-Current Protection and Short-to-Ground Protection

The TPL8032Q product integrates an internal current limit that helps to protect the regulator during fault conditions.

- When the output voltage is pulled down below the regulated voltage, over-current protection starts to work and limit the output current to I_{LIM}.
- When the output voltage is pulled down below the short-to-ground threshold, or shorted to ground directly, short-to-ground protection starts to work and limit the output current to I_{SC}.
- During startup, the output current is limited to I_{SC} before the output voltage ramps higher than the short-to-ground threshold.

Under the over-current conditions, the internal junction temperature ramps up quickly. When the junction temperature is high enough, it will cause the over-temperature protection.

Over-Temperature Protection

The over-temperature protection starts to work when the junction temperature exceeds the thermal shutdown (TSD) threshold, which turns off the regulator immediately. Until when the device cools down and the junction temperature falls below a value, which equals to thermal shutdown threshold minus thermal shutdown hysteresis, the regulator turns on again.

The junction temperature range should be limited according to the Recommended Operating Conditions table. Continuously operating above the junction temperature range will reduce the device lifetime.

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPL8032Q product is a series of 20-V 300-mA high-PSRR, ultra-low noise, low-dropout linear regulator. The following application schematic shows a typical usage of the TPL8032Q series.

Typical Application

The figure below shows the typical application schematic of the TPL8032Q product.

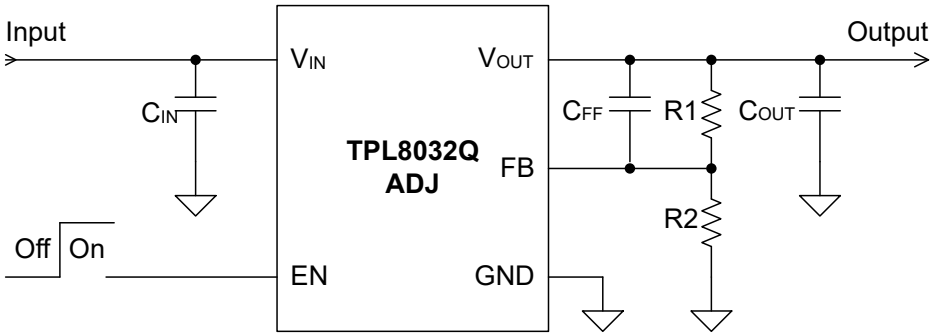


Figure 38. Typical Application Circuit

Input Capacitor and Output Capacitor

3PEAK recommends adding a 10-μF or greater capacitor with a 0.1-μF bypass capacitor in parallel at the IN pin to keep the input voltage stable. The voltage rating of the capacitors must be greater than the maximum input voltage.

To ensure loop stability, the TPL8032Q series requires an output capacitor of 2.2 μF or greater. 3PEAK recommends selecting an X7R type 10-μF ceramic capacitor with low ESR over temperature.

Both input capacitors and output capacitors must be placed as close to the device pins as possible.

Power Dissipation and Thermal Consideration

During normal operation, LDO junction temperature should meet the requirement in the Recommended Operating Conditions table. Using below equations to calculate the power dissipation and estimate the junction temperature.

The power dissipation can be calculated using the Equation 2.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad (2)$$

The junction temperature can be estimated using the Equation 3. θ_{JA} is the junction-to-ambient thermal resistance.

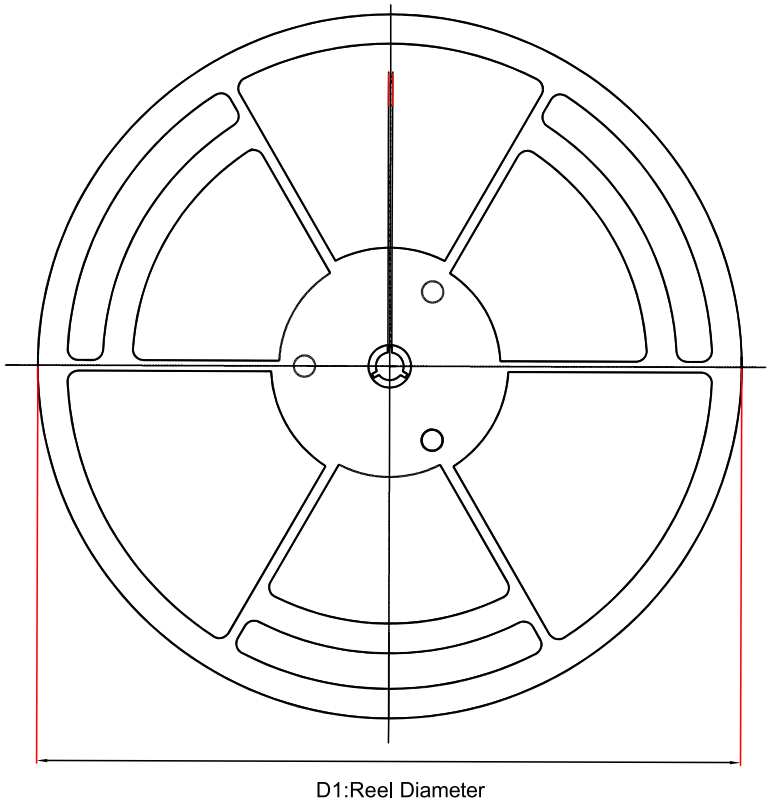
$$T_J = T_A + P_D \times \theta_{JA} \quad (3)$$

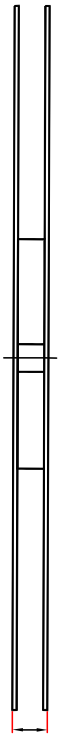
Layout

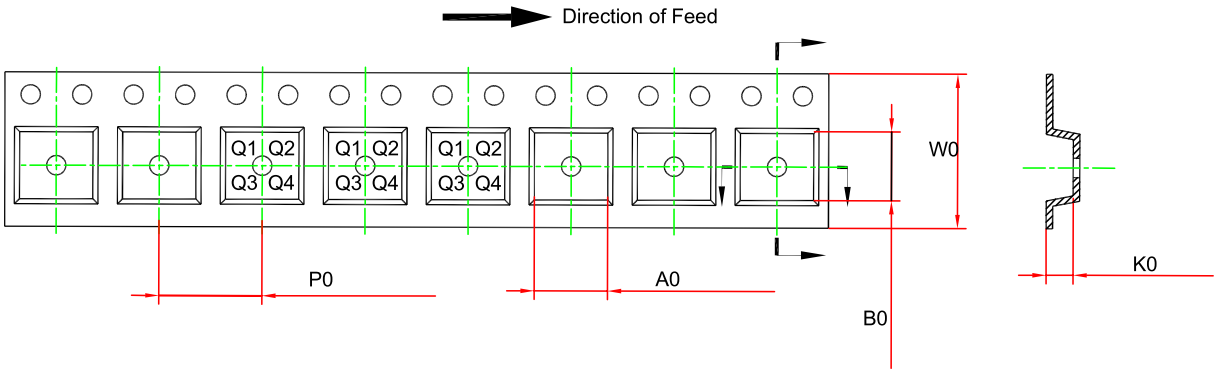
Layout Guideline

- Both input capacitors and output capacitors must be placed to the device pins as close as possible, and the vias between capacitors and device power pins must be avoided.
- It is recommended to bypass the input pin to ground with a 0.1-μF bypass capacitor. The loop area formed by the bypass capacitor connection, the IN pin and the GND pin of the system must be as small as possible.
- It is recommended to use wide and thick copper to minimize I×R drop and heat dissipation.
- Exposed pad must be connected to the PCB ground plane directly, the copper area must be as large as possible.

Tape and Reel Information





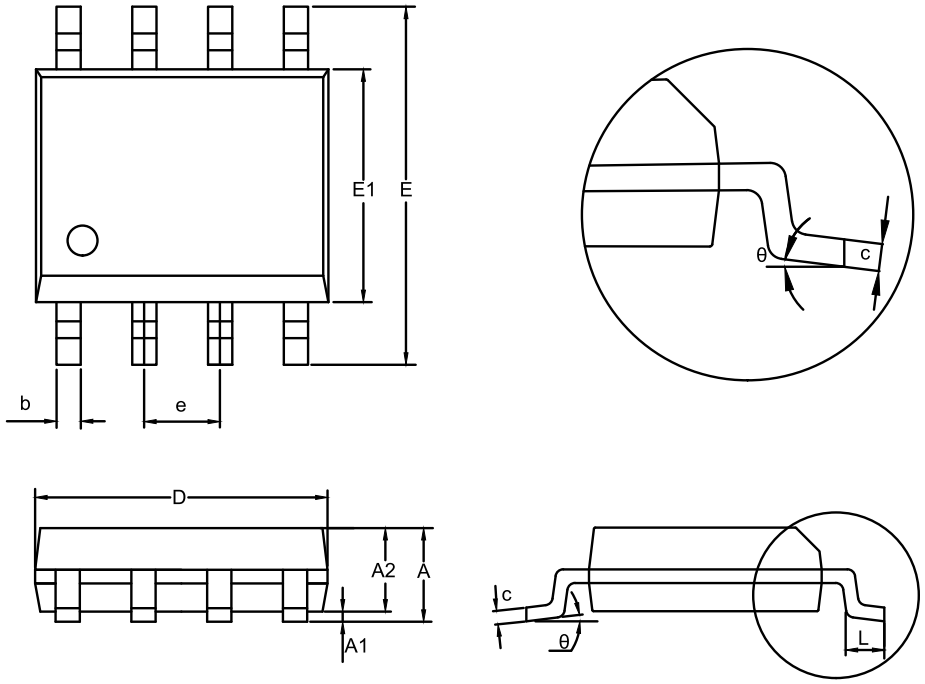


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPL8032ADQ-ES1R-S	ESOP-8	330	17.6	6.4	5.4	2.1	8	12	Q1

Package Outline Dimensions

ESOP8

Package Outline Dimensions ES1(ESOP-8-B)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.000	0.150	0.000	0.006
A2	1.250	1.550	0.049	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
D1	2.800	3.200	0.110	0.126
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
E2	2.400	2.800	0.094	0.110
e	1.270 BSC		0.050 BSC	
L	0.400	1.000	0.016	0.039
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPL8032ADQ-ES1R-S	−40 to 125°C	ESOP8	LBA	MSL3	Tape and Reel, 4,000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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