42-V 300-mA Wide-Input Low Quiescent Current Low-Dropout Linear Regulator with Watchdog Timer

Features

- Qualified for Automotive Applications
  - AEC-Q100 Grade 1, T_A: −40°C to +125°C
  - Junction Temperature, T_J: −40°C to +150°C
- Input Voltage: 4 V to 42 V, with 45-V Transient
- Output Voltage:
  - Fixed 5 V and 3.3 V
- ±2% Output Accuracy over Line Regulation, Load Regulation, and Operating Temperature Range
- 300-mA Maximum Output Current
- Low Dropout Voltage: 500-mV Maximum at 300-mA Load Current
- Low Current Consumption:
  - 0.5-μA Typical Shutdown Current (EN = LOW)
  - 6-μA Typical Quiescent Current (nWDEN = V_{OUT})
- Window and Standard Watchdog Configurable
  - Open/Closed Window Ratio 1:1 or 8:1 Configurable
  - Adjustable Watchdog Period from 10 ms to 2 s
  - Accurate Watchdog Period: ±10% Maximum when t_{WD} ≤ 500 ms
  - nWDEN Pin to Turn On or Turn Off the Watchdog Function
- Adjustable Power-Good Threshold
- Adjustable Power-Good Delay Period
- Stable with 4.7-μF to 500-μF Output Capacitor with ESR Range from 0.001 Ω to 20 Ω
- Integrated Protection:
  - Over-Current Protection
  - Over-Temperature Protection
- Package Option:
  - ETSSOP16

Applications

- Automotive Clusters and Infotainment
- Automotive BCM and HVAC System
- Automotive Electric Gear Shifter
- Automotive Battery Management System

Description

The TPL8536Q series comprises wide-input LDO products with an integrated watchdog timer, capable of delivering up to 300 mA. These devices can operate within a voltage range from 4 V to 42 V, with a maximum transient voltage of 45 V. Their ability to function reliably with a minimum voltage of 4 V makes them suitable for cold-crank and start-stop scenarios.

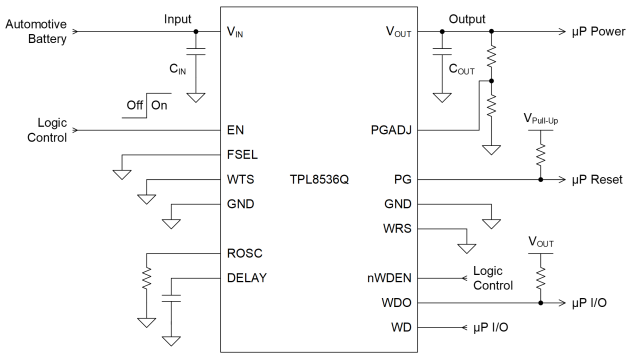
The TPL8536Q series offers 5-V and 3.3-V fixed output voltage options, with a maximum shutdown current of only 2 μA. When the watchdog function is disabled, these devices have a low typical quiescent current of just 6 μA.

The TPL8536Q series features the window watchdog and the standard watchdog with an accurate watchdog period. The watchdog period, the window ratio, and the power-good reset threshold are fully adjustable through external configuration. Furthermore, these devices include integrated over-current and over-temperature protection. In terms of output capacitors, the TPL8536Q series is compatible with a broad range from 4.7 μF to 500 μF with an ESR range spanning from 0.001 Ω to 20 Ω.

With the features above, the TPL8536Q series is an ideal power supply for microprocessors in a reliable system.

The TPL8536Q series of products operate in the ambient temperature range from –40°C to +125°C. Additionally, the TPL8536Q series provides a thermal-enhanced ETSSOP16 package to enable sustained operation despite significant dissipation across the device.

Typical Application Circuit



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Product Family Table

Order Number	Output Voltage (V)	Package
TPL853650Q-TSBR-S	5.0 V	ETSSOP16
TPL853633Q-TSBR-S	3.3 V	ETSSOP16

Revision History

Date	Revision	Notes
2023-07-09	Rev.Pre.0	Preliminary Datasheet
2023-09-19	Rev.Pre.1	Updated Test Waveforms
2023-12-13	Rev.Pre.2	Updated Electrical Characteristics
2024-07-10	Rev.Pre.3	Updated ESD Information
2024-09-01	Rev.A.0	Initial Released
2025-08-25	Rev.A.1	Added description to POD information required by packaging reference standards, and the actual product remains unchanged
2026-04-08	Rev.A.2	Corrected the I/O information for the WTS Pin in the Pin Configuration and Functions, and the actual product remains unchanged

Pin Configuration and Functions

TPL8536Q
ETSSOP-16 Package
Top View

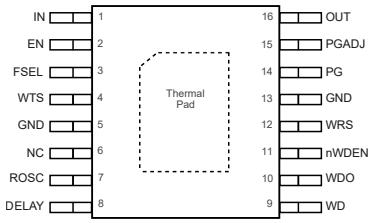


Table 1. Pin Functions: TPL8536Q

Pin No.	Name	I/O	Description
8	DELAY	O	Power-good delay adjustment pin. Connecting a capacitor from the DELAY pin to GND to set the PG delay time.
2	EN	I	Enable pin. Drive EN high to turn on the regulator; drive EN low to turn off the regulator.
3	FSEL	I	Frequency selection pin. Pull the FSEL pin HIGH to select the low-frequency oscillator and pull the FSEL pin LOW to select the high-frequency oscillator.
5, 13	GND	G	Ground reference pin. Connect the GND pin to the PCB ground plane directly.
1	IN	I	Input voltage pin. Bypass IN to GND with a 1-μF or greater capacitor.
6	NC	-	No internal connection.
11	nWDEN	I	Watchdog function enabling pin. Pull the nWDEN pin HIGH to disable the watchdog function and pull the nWDEN pin LOW to enable the watchdog function.
16	OUT	O	Regulated output voltage pin. Bypass OUT to GND with a 4.7-μF or greater capacitor.
14	PG	O	Power-good indication pin. PG pin is open-drain output and must be connected to V_{OUT} or pull-up voltage through an external resistor.
15	PGADJ	O	Powe-good threshold adjustment pin. Connect a resistor divider between the PGADJ and OUT pins to set the power-good threshold. Connect this pin to GND to set the threshold to 90.3% of V_{OUT}.
7	ROSC	O	Internal oscillator setting pin. Connect a resistor from ROSC to GND to set the watchdog period. The watchdog will report a fault when leaving this pin open or connecting this pin to GND at the watchdog output (WDO).
9	WD	I	Watchdog signal input pin.
10	WDO	O	Watchdog status output pin. Open-drain output pin. Pull this pin up to OUT through a resistor. The WDO pin outputs a LOW signal if a fault occurs.
12	WRS	I	Window watchdog ratio selection pin. Pull the WRS pin HIGH to set the open/closed window ratio to 8:1 and pull the WRS pin LOW to set the open/closed window ratio to 1:1.
4	WTS	I	Watchdog type selection pin. Pull the WTS pin HIGH to select the standard watchdog and pull the WTS pin LOW to select the window watchdog.

(1) Thermal Pad **MUST** be connected to PCB ground plane directly.

Specifications

Absolute Maximum Ratings

Parameter		Min	Max	Unit
IN, EN, FSEL, WTS		−0.3	45	V
OUT, PG, PGADJ, DELAY, ROSC, nWDEN, WRS, WD, WDO		−0.3	6	V
T_J	Junction Temperature Range	−40	150	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) All voltage values are with respect to GND.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	AEC Q100-002	±2	kV
CDM	Charged Device Model ESD	AEC Q100-011	±1	kV

Recommended Operating Conditions

Parameter		Min	Max	Unit
IN		4	42	V
EN, FSEL, WTS		0	V_{IN}	V
OUT		0	5.5	V
PG, PGADJ, DELAY, ROSC, nWDEN, WRS, WD, WDO		0	5.5	V
C_{OUT}	Output Capacitor Requirements	4.7	500	μF
ESR	Output Capacitor ESR Requirements	0.001	20	Ω
T_A	Ambient Temperature Range	−40	125	°C
T_J	Junction Temperature Range	−40	150	°C

Thermal Information

Package Type	θ_{JA}	θ_{JB}	$\theta_{JC,top}$	Unit
ETSSOP16	37.8	18	52.6	°C/W

Electrical Characteristics

All test conditions: V_{IN} = 14 V, V_{EN} = 2 V, C_{IN} = C_{OUT} = 10 μF, I_{OUT} = 0.1 mA. T_A = −40°C to +125°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply Input Voltage and Current						
V_{IN}	Input Supply Voltage Range (1)		V_{IN_MIN}		42	V
UVLO	V_{IN} Under-Voltage Lockout Threshold	V_{IN} rising, V_{EN} = 2 V, I_{OUT} = 0.1 mA			2.8	V
	Hysteresis			250		mV
I_{SD}	Shutdown Current	V_{EN} = 0 V		0.5	4	μA
I_Q	Quiescent Current	I_{OUT} = 0 mA, V_{nWDEN} = V_{OUT}		6	15	μA
		I_{OUT} = 0 mA, V_{nWDEN} = GND		14	28	μA
		I_{OUT} = 0.5 mA, V_{nWDEN} = V_{OUT}		7.5	20	μA
		I_{OUT} = 0.5 mA, V_{nWDEN} = GND		17.5	32	μA
EN, WTS, FSEL Voltage and Current						
V_{IH}	High-Level Input Voltage		2		V_{IN}	V
V_{IL}	Low-Level Input Voltage		0		0.7	V
V_{HYS}	Hysteresis			150		mV
I_{EN}	EN Pin Leakage Current	V_{EN} = 2 V to 42 V	−1		1	μA
nWDEN Voltage and Current						
V_{IH}	High-Level Input Voltage	Watchdog function disable	2		5.5	V
V_{IL}	Low-Level Input Voltage	Watchdog function enable	0		0.7	V
I_{nWDEN}	Pull-Down Current of nWDEN pin				1	μA
Watchdog Oscillator						
V_{ROSC}	Voltage Reference of Oscillator		0.95	1	1.05	V
Watchdog Operation (WD, WDO, WRS)						
V_{IH}	High-Level Input Voltage	For WD and WRS pins	70%		100%	×V_{OUT}
V_{IL}	Low-level Input Voltage	For WD and WRS pins	0%		30%	×V_{OUT}
V_{HYS}	Hysteresis			10%		×V_{OUT}
I_{WD}	WD Pin Pull Down Current	V_{WD} = 5 V		1	4	μA
V_{OL_WDO}	WDO Pin Output Low-Level Voltage	I_{WDO} = 5 mA			0.4	V
I_{LKG_WDO}	WDO Pin Leakage Current	WDO pin pulled to V_{OUT} through 10-kΩ resistor			1	μA
t_{WD}	Watchdog Duration	R_{ROSC} = 20 kΩ ±1%, FSEL = LOW	9.5	10	10.5	ms
		R_{ROSC} = 20 kΩ ±1%, FSEL = HIGH	47.5	50	52.5	ms

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Tolerance Of Watchdog Duration	R_{ROSC} = 20 kΩ ±1% to 50 kΩ ±1%	−5%		5%	
t_{WD_SS}	Watchdog Input Signal Duration	t_{WD} ≤ 500 ms	100			μs
		500 ms < t_{WD} ≤ 2 s (3)	400			μs
t_{WD_HOLD}	Watchdog Output Resetting Time (Percentage of Settled Watchdog Window Duration)			20%		×t_{WD}
t_{WD_RST}	Watchdog Output Resetting Time (Percentage of Settled Watchdog Window Duration)	R_{ROSC} = 20 kΩ ±1%, FSEL = LOW	1.9	2	2.1	ms
		R_{ROSC} = 20 kΩ ±1%, FSEL = HIGH	9.5	10	10.5	ms
PG Voltage and Current						
V_{TH_PG}	Default PG Pin Threshold	PGADJ is connected to GND, V_{OUT} increasing	88%	90.3%	94%	×V_{OUT}
	PG Hysteresis	PGADJ is connected to GND, V_{OUT} decreasing		3%		×$_{VOUT}$
V_{OL_PG}	PG Pin Output Low-Level Voltage	PG pulled low, force 5 mA to PG pin			0.4	V
I_{LKG_PG}	PG Pin Leakage Current	PG pulled to V_{OUT} through a 10-kΩ resistor			1	μA
PGADJ						
V_{REF_PGADJ}	Switching Voltage for The Power-Good Adjust Pin	V_{OUT} falling	1.02	1.065	1.10	V
	PGADJ Hysteresis			34		mV
PG delay time						
I_{DLY_CHG}	DELAY Capacitor Charging Current		3	6.3	10	μA
V_{TH_DLY}	DELAY Pin Threshold to Release PG (High)	DELAY voltage ramping up	0.95	1	1.05	V
I_{DLY_DIS}	DELAY Capacitor Discharging Current	V_{DELAY} = 1 V	0.5			mA
t_{DEG}	PG Deglitch Time		55	160	350	μs
t_{DLY_FIX}	Fixed PG Delay Time	C_{DELAY} = open	50	340	600	μs
t_{DLY}	Adjustable PG Delay Time	C_{DELAY} = 100 nF		16		ms
Output Voltage and Current						
V_{OUT}	Output Accuracy	V_{IN} = V_{OUT} + 1 V to 42 V, I_{OUT} = 0 to 300 mA	−2%		2%	
ΔV_{OUT}	Line Regulation	V_{IN} = 6 V to 42 V, I_{OUT} = 1 mA	−5		5	mV
	Load Regulation	I_{OUT} = 1 mA to 300 mA	−0.9%		0.9%	×V_{OUT}
V_{DO}	Dropout Voltage (2)	I_{OUT} = 200 mA, V_{OUT} = 5 V		170	350	mV

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		I_{OUT} = 300 mA, V_{OUT} = 5 V		260	500	mV
		I_{OUT} = 200 mA, V_{OUT} = 3.3 V		210	400	mV
		I_{OUT} = 300 mA, V_{OUT} = 3.3 V		310	600	mV
I_{OUT}	Output Current Range	V_{OUT} in regulation	0		300	mA
I_{CL}	Output Current Limit	V_{OUT} short to GND	550	700	1000	mA
t_{SU}	Start-Up Time (3)	V_{OUT} = 5 V, I_{OUT} = 1 mA		4		ms
PSRR	Power Supply Rejection Ratio (3)	I_{OUT} = 10 mA, f = 100 Hz		65		dB
		I_{OUT} = 10 mA, f = 1 kHz		50		dB
		I_{OUT} = 10 mA, f = 100 kHz		40		dB
		I_{OUT} = 10 mA, f = 1 MHz		60		dB
Temperature Range						
T_{SD}	Thermal Shutdown Threshold (3)			175		°C
	Thermal Shutdown Hysteresis (3)			20		°C

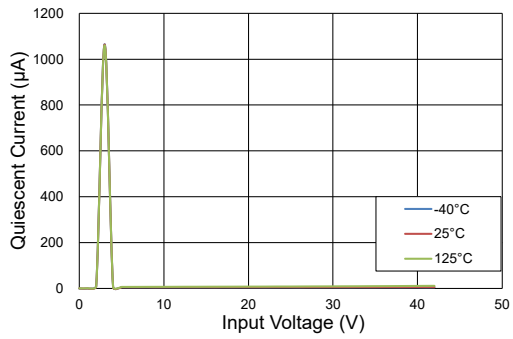
(1) V_{IN_MIN} = 4 V or V_{OUT_NOM} + V_{DO}, whichever is greater.

(2) Dropout voltage is the minimum input-to-output voltage differential needed to maintain regulation at a specified output current. Dropout voltage is measured when the output voltage has dropped 100 mV from the nominal value. In dropout, the output voltage will be equal to (V_{IN} – V_{DO}).

(3) Not tested during production, guaranteed by design.

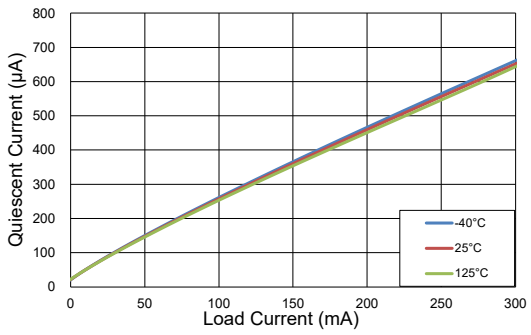
Typical Performance Characteristics

All test conditions: V_{IN} = 14 V, C_{IN} = C_{OUT} = 10 μF, V_{EN} = 2 V, I_{OUT} = 0.1 mA. T_A = 25°C, unless otherwise noted.



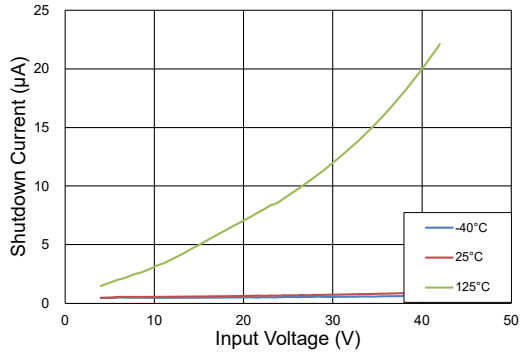
V_{OUT} = 3.3 V

Figure 1. Quiescent Current vs Input Voltage



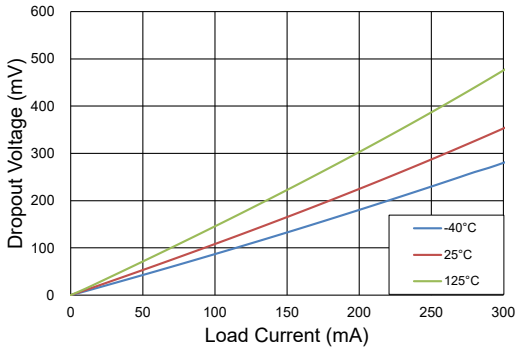
V_{OUT} = 3.3 V

Figure 2. Quiescent Current vs Load Current



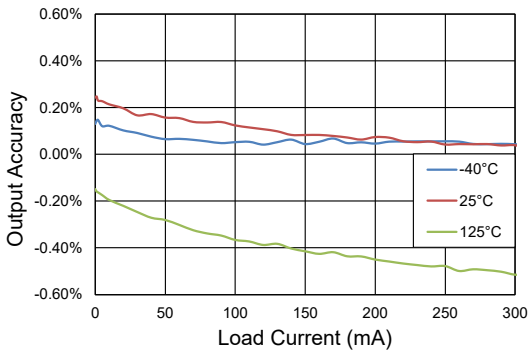
V_{EN} = 0 V

Figure 3. Shutdown Current vs Input Voltage



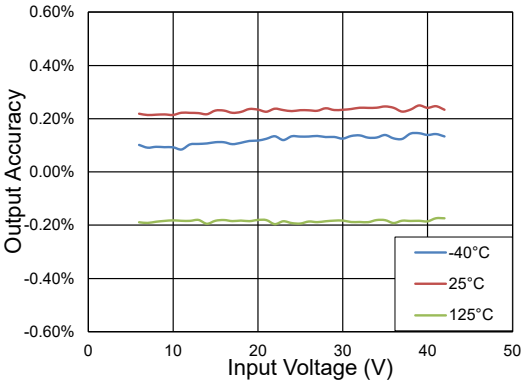
V_{OUT} = 3.3 V

Figure 4. Dropout Voltage vs Load Current



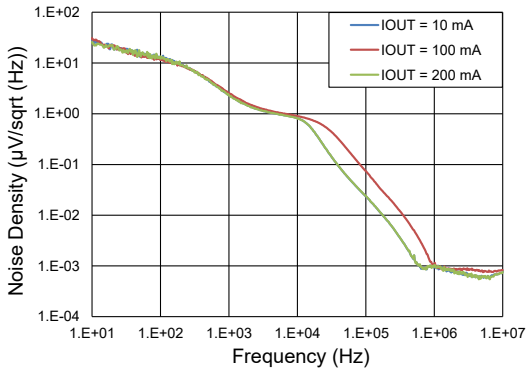
V_{OUT} = 3.3 V

Figure 5. Load Regulation



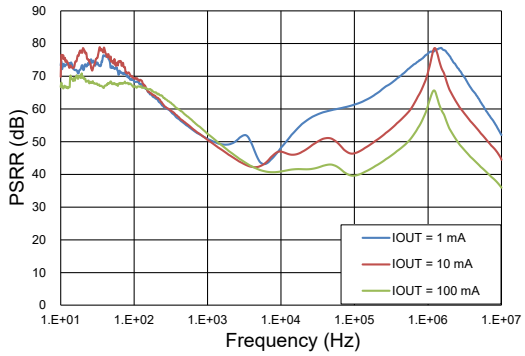
V_{OUT} = 3.3 V

Figure 6. Line Regulation



V_{OUT} = 3.3 V

Figure 7. Noise



V_{OUT} = 3.3 V

Figure 8. PSRR

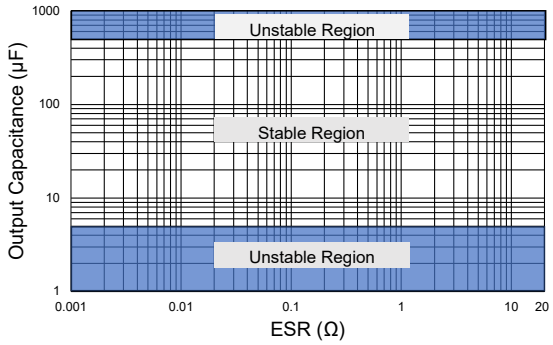
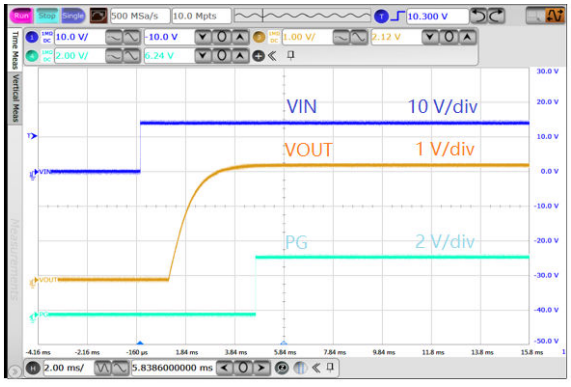


Figure 9. Output Capacitance Stability Range



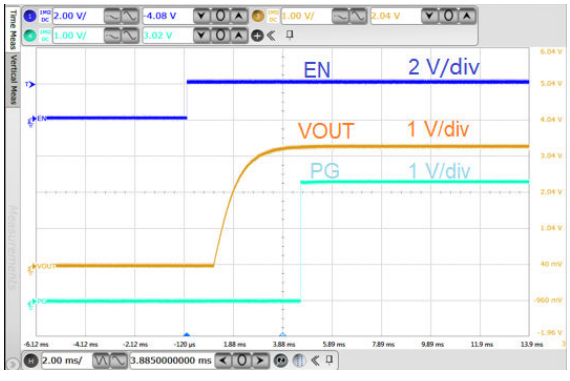
V_{nWDEN} = 2 V to 0 V, V_{FSEL} = 0 V, R_{ROSC} = 20 kΩ, t_{WD} = 10 ms. No watchdog service signal during the open window.

Figure 10. Watchdog Fault Waveform



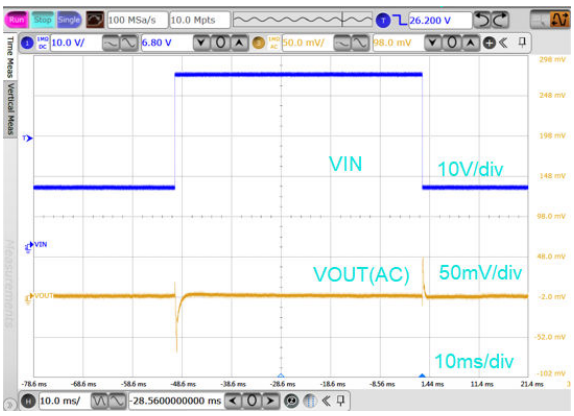
V_{EN} = V_{IN} = 0 V to 14 V

Figure 11. Startup Waveform



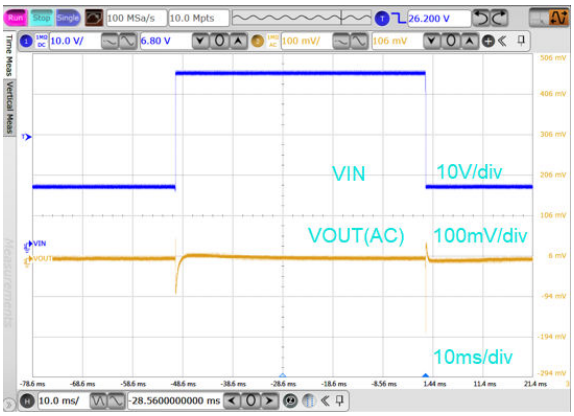
V_{IN} = 14 V, V_{EN} = 0 V to 2 V

Figure 12. Startup Waveform



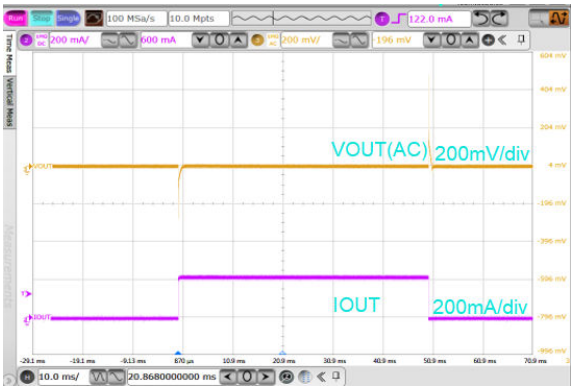
V_{IN} = 14 V to 42 V, I_{OUT} = 0 mA

Figure 13. Line Transient



V_{IN} = 14 V to 42 V, I_{OUT} = 75 mA

Figure 14. Line Transient



V_{IN} = 14 V, I_{OUT} = 1 mA to 200 mA

Figure 15. Load Transient

Detailed Description

Overview

The TPL8536Q series comprises wide-input LDO products with an integrated watchdog timer, capable of delivering up to 300 mA. These devices can operate within a voltage range from 4 V to 42 V, with a maximum transient voltage of 45 V. Their ability to function reliably with a minimum voltage of 4 V makes them suitable for use in cold-crank and start-stop scenarios.

The TPL8536Q series offers both 5-V and 3.3-V fixed output voltage options, with a typical shutdown current of only 0.5 μA. When the watchdog function is disabled, these devices have an exceptionally low quiescent current of just 6 μA.

The TPL8536Q series devices feature the window watchdog and the standard watchdog with an accurate watchdog period. The watchdog period, the window ratio, and the power-good reset threshold are fully adjustable through external configuration. Furthermore, these devices include integrated over-current and over-temperature protection. In terms of output capacitors, the TPL8536Q series is compatible with a broad range, ranging from 4.7 μF to 500 μF, with an ESR range spanning from 0.001 Ω to 20 Ω.

With the features above, the TPL8536Q series is an ideal power supply for microprocessors in a reliable system.

Functional Block Diagram

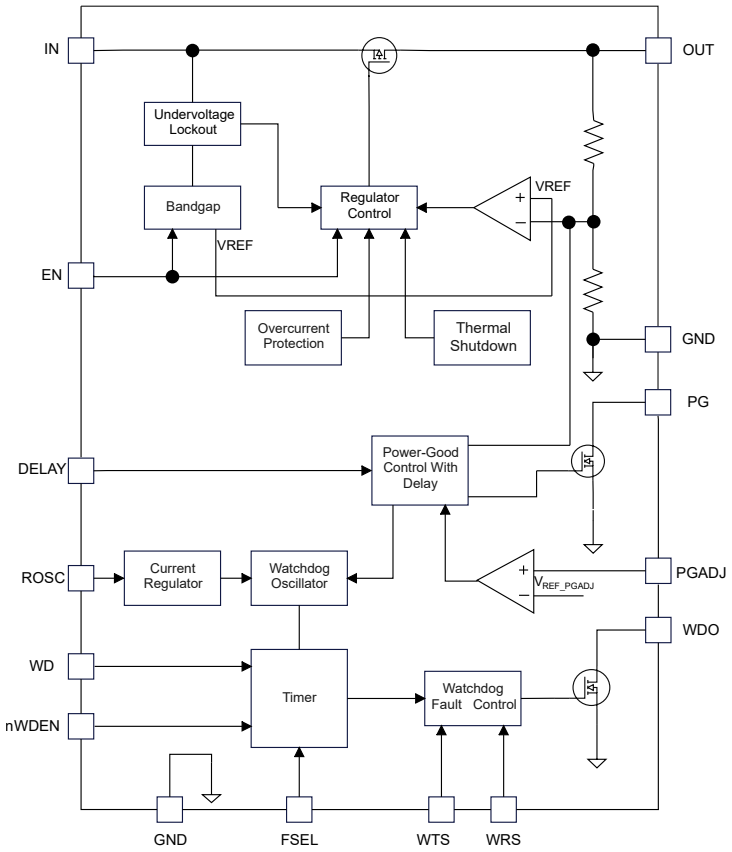


Figure 16. Functional Block Diagram

Feature Description

Enable (EN)

The enable pin (EN) is active high. Connect this pin to the GPIO of an external processor or a digital logic control circuit to enable and disable the device. Or connect this pin to the IN pin for self-bias applications.

Under-Voltage Lockout (UVLO)

The TPL8536Q series uses an under-voltage lockout circuit to keep the output shut off until the internal circuitry operates properly. Refer to the Electrical Characteristics table for UVLO threshold and hysteresis.

Regulated Output Voltage (OUT)

The TPL8536Q series is available in fixed voltage versions of 5 V and 3.3 V. When the input voltage is higher than V_{OUT_NOM} + V_{DO}, the output pin is the regulated output based on the selected voltage version. When the input voltage falls below V_{OUT_NOM} + V_{DO}, the output pin tracks the input voltage minus the dropout voltage.

Adjustable Power-Good Threshold (PG, PGADJ)

The PG pin is an open-drain output with an external pull-up resistor to the regulated supply, and the PGADJ pin is a power-good threshold adjustment pin.

Connecting the PGADJ pin to GND sets the power-good threshold value to default, V_{TH_PG}.

The power-good threshold is also adjustable from 1.065 V to 5 V by using an external resistor divider between PGADJ and OUT. The threshold can be calculated using the following equations:

$$V_{PG_ADJ_falling} = V_{REF_PGADJ} \times \frac{R_1 + R_2}{R_2} \quad (1)$$

$$V_{PG_ADJ_rising} = \left(V_{REF_PGADJ} + 34\ mV\ (typical)\right) \times \frac{R_1 + R_2}{R_2} \quad (2)$$

where:

- $V_{PG_ADJ_rising}$ and $V_{PG_ADJ_falling}$ are the adjustable power-good threshold.
- V_{REF_PGADJ} is the internal comparator reference voltage of the PGADJ pin, 1.065 V typical.

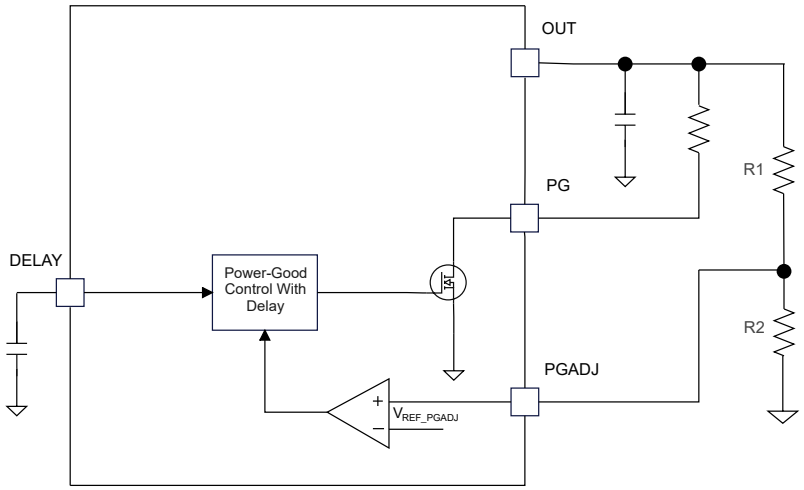


Figure 17. Adjustable Power-Good Threshold Configuration

Adjustable Power-Good Delay Timer (DELAY)

The power-good delay period is determined by the value set by an external capacitor on the DELAY pin before turning the PG pin high. The constant current charges an external capacitor until the voltage exceeds a threshold, Equation 3 determines the power-good delay period:

$$t_{DLY} = \frac{C_{DELAY} \times 1\ V}{6.3\ \mu A} \quad (3)$$

where t_{DLY} is the adjustable power-good delay period and C_{DELAY} is the value of the power-good delay capacitor.

Over-Current Protection

The TPL8536Q series integrates an internal current limit that helps to protect the regulator during the fault conditions, e.g., the output is shorted to ground, or the output is forced below V_{OUT_NOM}. The output voltage is not regulated when the device is in current limit, and $V_{OUT} = I_{CL} \times R_{LOAD}$.

Over-Temperature Protection

The over-temperature protection starts to work when the junction temperature exceeds the thermal shutdown (T_{SD}) threshold, which turns off the regulator immediately. When the device cools down and the junction temperature falls below the thermal shutdown threshold minus thermal shutdown hysteresis, the regulator turns on again.

The junction temperature range should be limited according to the Recommended Operating Conditions table, and continuous operation above the junction temperature range reduces the lifetime of the device.

Integrated Watchdog

The TPL8536Q series has an integrated watchdog with fault (WDO) output option. Both window watchdog and standard watchdog are available. The operation of the watchdog timer, the handling of fault conditions, and the differences between window watchdog and standard watchdog timers are explained below.

Window Watchdog (WTS, ROSC, FSEL and WRS)

When the watchdog type selection (WTS) pin is connected to a low voltage level, the TPL8536Q series works in the window watchdog mode. The duration of the watchdog window can be set by connecting an external resistor (R_{ROSC}) to GND at

the ROSC pin and setting the voltage level at the FSEL pin. The current through the R_{ROSC} resistor determines the clock frequency of the internal oscillator. The duration of the watchdog window (the watchdog timer period) can be changed by changing the resistor value. A high voltage level at the FSEL pin sets the watchdog window to 5 times as long as that of a low voltage level with the same external component configuration.

The duration of the watchdog window and the duration of the fault output are multiples of the internal oscillator frequency, as shown by the following equations:

FSEL low

$$t_{WD} = R_{ROSC} \times 0.5 \times 10^{-6} \quad (4)$$

FSEL high

$$t_{WD} = R_{ROSC} \times 2.5 \times 10^{-6} \quad (5)$$

Watchdog initialization

$$t_{WD_initialization} = 8 \times t_{WD} \quad (6)$$

Open and closed windows

$$t_{WD} = t_{OW} + t_{CW} \quad (7)$$

WRS low

$$t_{OW} = t_{CW} = 50\% \times t_{WD} \quad (8)$$

WRS high

$$t_{OW} = 8 \times t_{CW} = \frac{8}{9} \times t_{WD} \quad (9)$$

where:

- t_{WD} is the duration of the watchdog window.
- R_{ROSC} is the resistor connected to the ROSC pin.
- $t_{WD_initialization}$ is the duration of the watchdog initialization.
- t_{OW} is the duration of the open watchdog window.
- t_{CW} is the duration of the closed watchdog window.

For all the foregoing items, the unit of resistance is Ω and the unit of time is s.

The following table illustrates several periods of watchdog window with typical conditions.

FSEL	R_{ROSC} (kΩ)	I_{ROSC} (μA)	t_{WD} (ms)	Watchdog Period Tolerance
High	800	1.25	2000	30%
	200	5	500	10%
	100	10	250	8%
	40	25	100	5%
	20	50	50	5%
Low	100	10	50	8%
	40	25	20	5%
	20	50	10	5%

For both 5-V and 3.3-V output versions, the period of watchdog window (TWD) can also support from 0.5-s to 2-s range. The ROSC value can be calculated using the equations above.

Each watchdog window consists of an open window and a closed window. When the window ratio selection WRS pin is low, the width of each open window t_{OW} and closed window t_{CW} is approximately 50% of the watchdog window t_{WD}. When the WRS pin is high, the ratio between window opening and window closing is approximately 8:1. However, there is an exception: the first open window after the watchdog initialization $t_{WD_initialization}$ is eight times the duration of the watchdog window. During this initial open window, the monitor must receive service signals via software, external microcontroller, etc.

When servicing the watchdog during a closed window or not servicing during an open window the watchdog fault occurs.

The window watchdog is able to monitor the frequency of the watchdog service signal (WD) to ensure it remains within specified limits. In the event that the WD signal frequency falls outside the predetermined range, a WDO low-voltage fault is triggered.

The following figure illustrates a normal operation of the window watchdog for the TPL8536Q, specifically when the WRS is low. Once the output voltage stabilizes and the PG signal goes high, the window watchdog activates when an external signal pulls the nWDEN (watchdog enable pin) to a low state. This triggers the watchdog initialization, and the device then waits for a WD service signal during the initial window, which is eight times the duration of t_{WD}. During this initialization open window, applying a service signal to the WD pin resets the watchdog counter, initiating a closed window period. It's crucial to note that watchdog service should not occur during this closed window to prevent a fault condition. To maintain proper operation and avoid faults, watchdog service must be performed during the subsequent open window.

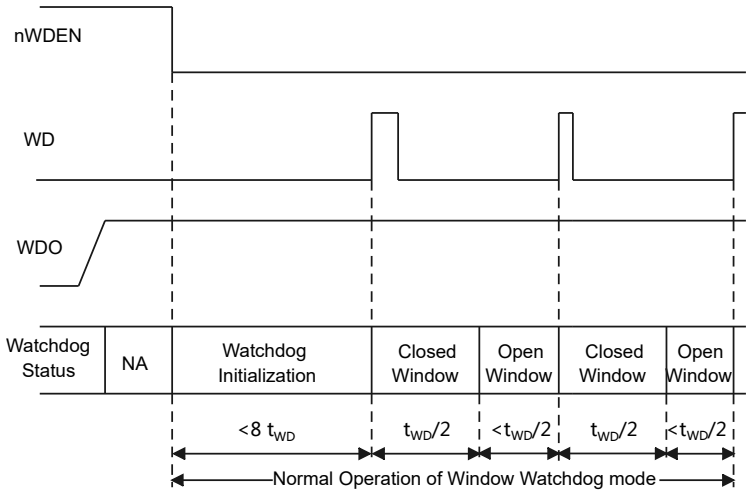


Figure 18. Normal Operation of Window Watchdog

The following figure shows three different fault conditions:

Fault 1: No WD service signal in WD initialization. WDO is triggered after the maximum initialization window duration eight times of t_{WD}.

Fault 2：WD service signal in closed window. WDO is triggered after receiving a WD rising edge during the closed window.

Fault 3：No WD service signal in the open window. WDO is triggered after the maximum open-window duration of the half of t_{WD}.

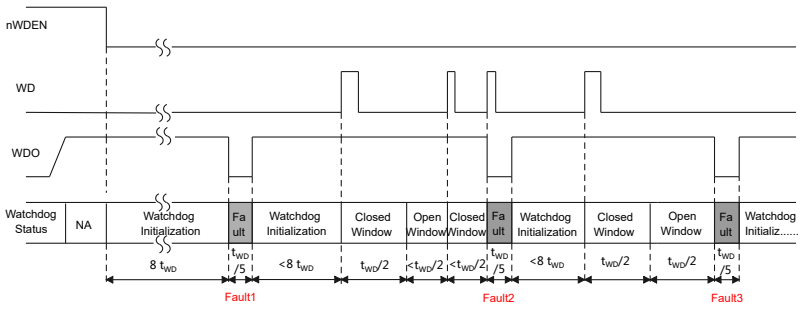


Figure 19. Fault Conditions of Window Watchdog

Standard Watchdog (WTS, ROSC, and FSEL)

These devices operate in the standard watchdog mode when the watchdog type selection (WTS) pin is connected to a high voltage level. Similar to the window watchdog mode, users can set the duration of the watchdog window by adjusting the value of the external resistor (R_{ROSC}) at the ROSC pin and setting the voltage level at the FSEL pin.

FSEL low

$$t_{WD} = R_{ROSC} \times 0.5 \times 10^{-6} \quad (10)$$

FSEL high

$$t_{WD} = R_{ROSC} \times 2.5 \times 10^{-6} \quad (11)$$

Watchdog initialization

$$t_{WD_initialization} = 8 \times t_{WD} \quad (12)$$

where:

- t_{WD} is the duration of the watchdog window.
- R_{ROSC} is the resistor connected to the ROSC pin.
- $t_{WD_initialization}$ is the duration of the watchdog initialization.

There is no closed window in standard watchdog mode compared with window watchdog.

The standard watchdog is able to monitor the frequency of the watchdog service signal (WD) to ensure it remains lower than a certain value. In the event that the WD signal frequency is lower than the set value, a WDO low-voltage fault is triggered.

The following figure illustrates the normal operation of the standard watchdog for the TPL8536Q. Once the output voltage stabilizes and the PG signal goes high, the standard watchdog activates when an external signal pulls the nWDEN (watchdog enable pin) to a low state. This triggers the watchdog initialization, and the device then waits for a WD service signal during the initial window, which is eight times the duration of t_{WD}. During this initialization open window, applying a service signal to the WD pin resets the watchdog counter, initiating another open window period. It's crucial to note that a WD service signal must occur during every open window to prevent the fault condition.

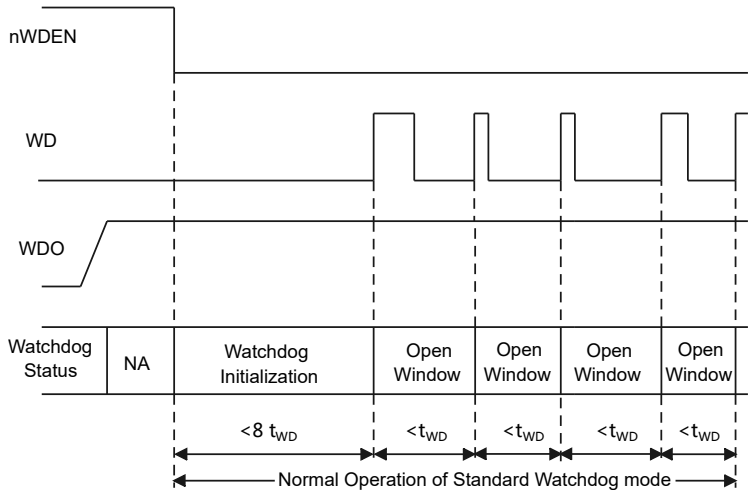


Figure 20. Normal Operation of Standard Watchdog

The following figure shows two different fault conditions:

Fault 1: No WD service signal in WD initialization. WDO is triggered after the maximum initialization window duration eight times of t_{WD}.

Fault 2：No WD service signal in open window time. WDO is triggered after the maximum open-window duration t_{WD}.

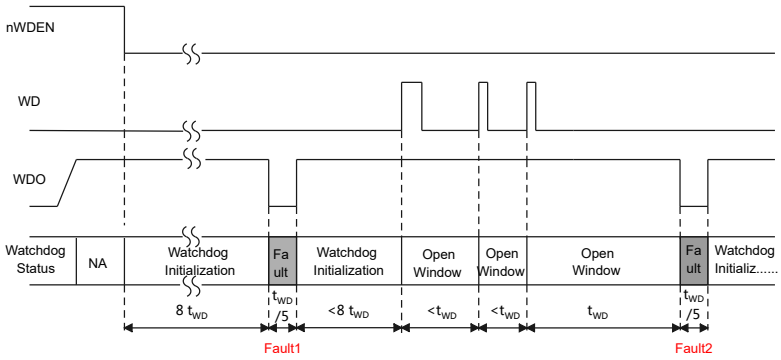


Figure 21. Fault Conditions of Standard Watchdog

Watchdog Service Signal and Watchdog Fault Outputs (WD and WDO)

The watchdog service signal (WD) must stay high for at least 100 μs when t_{WD} ≤ 500 ms. The watchdog service signal (WD) must stay high for at least 400 μs when 500 ms < t_{WD} ≤ 2 s.

The WDO pin is the fault output terminal. When a watchdog fault occurs, the devices pull WDO low for a duration of t_{WD_HOLD}.

$$t_{WD_HOLD} = 20\% \times t_{WD} \quad (13)$$

ROSC Status Detection (ROSC)

When a watchdog function is enabled, if the ROSC pin is shorted to GND or open, the watchdog output (WDO) pin remains low, indicating a fault status.

Watchdog Enable (PG and nWDEN)

When PG (power good) is high, an external circuit can apply a logic signal to the nWDEN pin to disable or enable the watchdog. A low input to this pin turns the watchdog on, while a high input turns the watchdog off.

When PG is low, the watchdog is disabled and the watchdog-fault output WDO pin stays in the high-impedance state.

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK' s component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK' s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPL8536Q is a series of 42-V 300-mA wide-input low-quiescent current low-dropout linear regulators with a watchdog timer. The following application schematic shows a typical usage of the TPL8536Q series.

Typical Application

Figure 22 shows the typical application schematic of the TPL8536Q series.

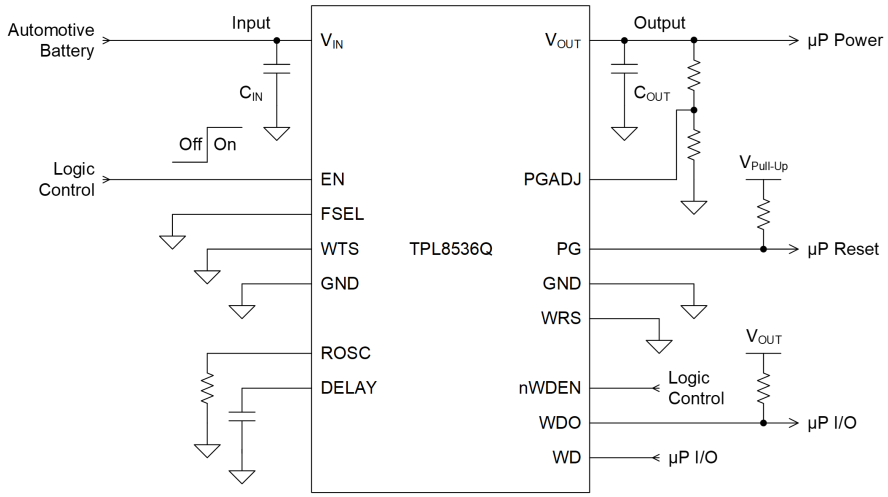


Figure 22. Typical Application Circuit

Input Capacitor and Output Capacitor

3PEAK recommends adding a 10-µF or greater capacitor with a 0.1-µF bypass capacitor in parallel at the IN pin to keep the input voltage stable. The voltage rating of the capacitors must be greater than the maximum input voltage.

To ensure loop stability, the TPL8536Q series requires an output capacitor of 4.7 µF to 500 µF with an ESR range from 0.001 Ω to 20 Ω. 3PEAK recommends selecting an X7R type 10-µF ceramic capacitor with low ESR over temperature.

Both input capacitors and output capacitors must be placed as close to the device pins as possible.

Power Dissipation and Thermal Consideration

During normal operation, the LDO junction temperature should meet the requirement in the Recommended Operating Conditions table. Use the below equations to calculate the power dissipation and estimate the junction temperature.

The power dissipation can be calculated using Equation 14.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad (14)$$

The junction temperature can be estimated using Equation 15. θ_{JA} is the junction-to-ambient thermal resistance.

$$T_J = T_A + P_D \times \theta_{JA} \quad (15)$$

Layout

Layout Guideline

- Both input and output capacitors must be placed to the device pins as close as possible, and the vias between capacitors and device power pins must be avoided.
- It is recommended to bypass the input pin to ground with a 0.1-μF bypass capacitor. The loop area formed by the bypass capacitor connection, the IN pin, and the GND pin of the system must be as small as possible.
- It is recommended to use wide and thick copper to minimize I×R drop and heat dissipation.

Layout Example

The following figure shows a layout example of the TPL8536Q.

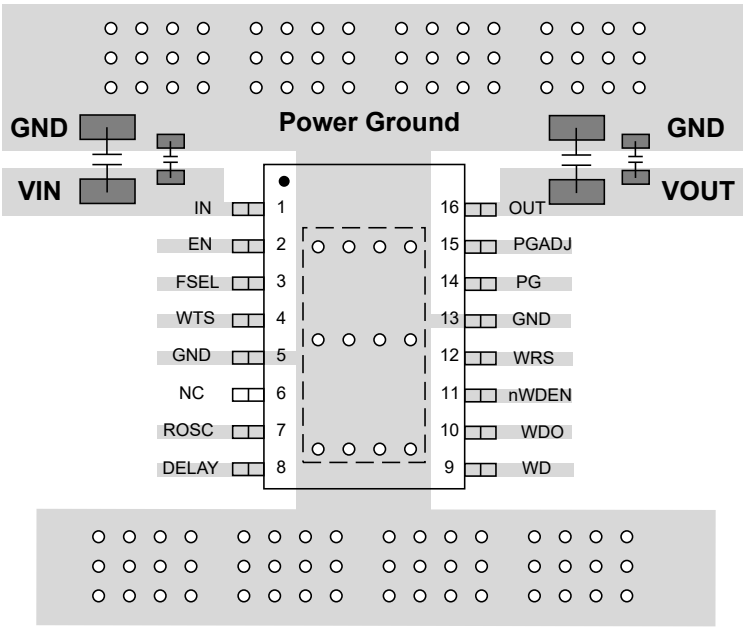
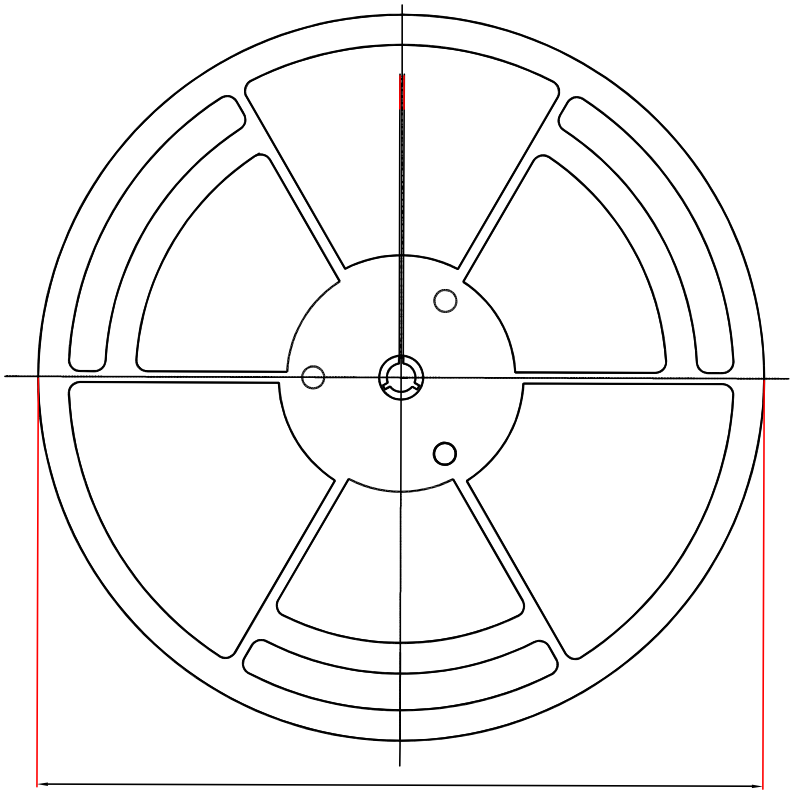
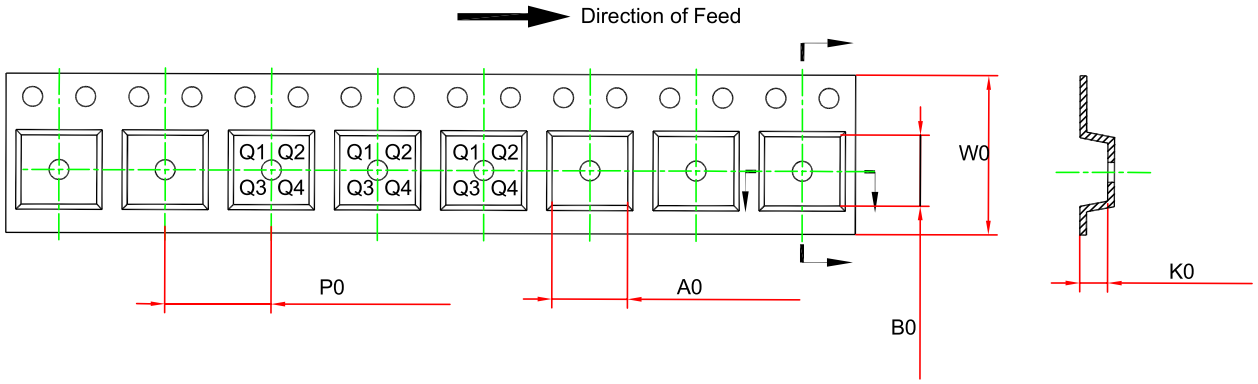


Figure 23. TPL8536Q Layout Example

Tape and Reel Information





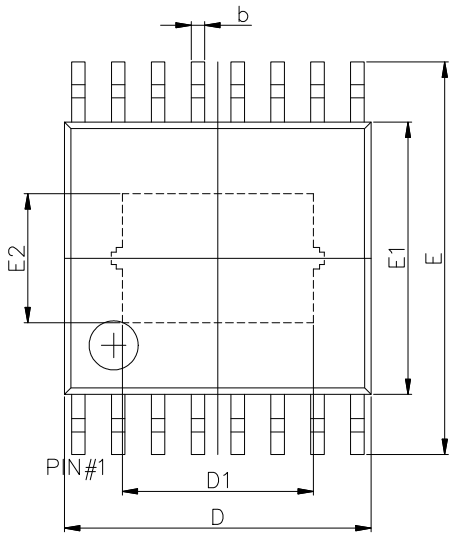


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPL853650Q-TSBR-S	ETSSOP16	330	17.6	6.8	5.4	1.5	8	12	Q1
TPL853633Q-TSBR-S	ETSSOP16	330	17.6	6.8	5.4	1.5	8	12	Q1

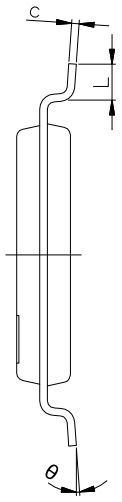
Package Outline Dimensions

ETSSOP16

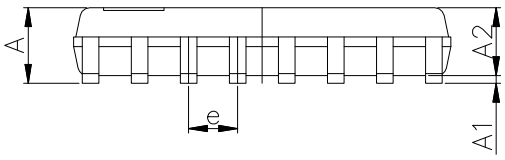
Package Outline Dimensions TSB(ETSSOP-16-D)



Top View



Side View



Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	---	1.100	---	0.043
A1	0.050	0.150	0.002	0.006
A2	0.850	0.950	0.033	0.037
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.900	5.100	0.193	0.201
D1	3.015	3.215	0.119	0.127
E	6.200	6.600	0.244	0.260
E1	4.300	4.500	0.169	0.177
E2	2.005	2.205	0.079	0.087
e	0.650 BSC		0.026 BSC	
L	0.500	0.700	0.020	0.028
θ	1°	7°	1°	7°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-153.
4. The thermal pad is on Bottom side of the product.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPL853650Q-TSBR-S	−40 to 125°C	ETSSOP16	L3650	MSL3	3,000	Green
TPL853633Q-TSBR-S	−40 to 125°C	ETSSOP16	L3633	MSL3	3,000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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