2-A Output, High-PSRR, Low-Noise LDO Regulator

Features

- Input Voltage Range:
  - 1.4 V to 6.5 V
- Output Voltage Range:
  - Adjustable Output Voltage: 0.8 V to 5.2 V
- ±1% Output Accuracy over Line, Load Regulation, and Operating Temperature Range
- 2-A Maximum Output Current
- Dropout Voltage: 80 mV typ at 2 A
- PSRR:
  - 70 dB at 1 kHz
  - 40 dB at 500 kHz
- 6-μV_{RMS} Output Voltage Noise
- Excellent Transient Response
- Enable Control
- Adjustable Soft-Start Control with Charging Current Options
- Open-Drain Power-Good Output
- Stable with a 22-µF or Greater Ceramic Capacitor
- Over-Current Protection
- Over-Temperature Protection
- Operating Temperature: −40°C to +125°C
- Package Options:
  - DFN2.5X2.5-10

Applications

- Communication: CPU, ASIC, FPGA, CPLD, DSP
- High-Performance Analog: ADC, DAC, LVDS, VCO
- Noise-Sensitive Imaging: CMOS Sensors, Video ASICs

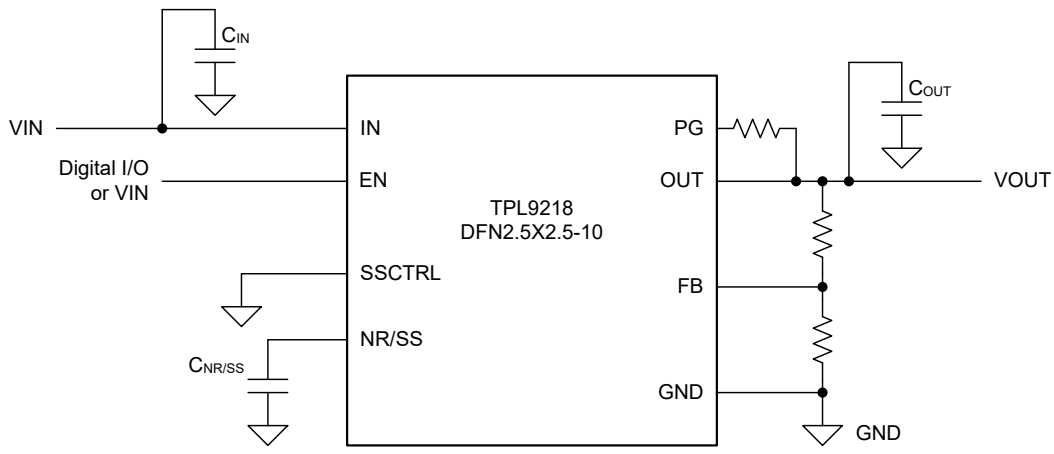
Description

The TPL9218 product is a 2-A high-current, 6-μV_{RMS} low-noise, high-PSRR, and high-accuracy linear regulator with a typically 80-mV ultra-low dropout voltage in the 2-A load condition. The TPL9218 product supports adjustable output voltage ranging from 0.8 V to 5.2 V with external resistor dividers.

Ultra-low noise, high-PSRR, and high-output current capabilities make the TPL9218 product an ideal power supply for noise-sensitive applications, such as high-speed communication facilities, test and measurement devices, or high-definition imaging equipment. Accurate output voltage tolerance, output voltage remote sensing, excellent transient response, and flexible soft-start control ensure the TPL9218 product an optimal power supply for large-scale processors and digital loads, such as CPU, ASIC, FPGA, CPLD, and DSP.

The TPL9218 product provides a 10-pin 2.5×2.5 DFN package with guaranteed operating junction temperature ranging from −40°C to +125°C.

Typical Application Circuit



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Product Family Table

Order Number	Output Voltage (V)	Package
TPL9218AD-DF5R-S	Adjustable (0.8 V to 5.2 V)	DFN2.5X2.5-10

Revision History

Date	Revision	Notes
2022-11-30	Rev.Pre.0	Preliminary Revision.
2023-01-15	Rev.A.0	Initial Released.
2023-11-16	Rev.A.1	Update typical performance characteristics.
2024-04-01	Rev.A.2	Update the typical value of $I_{NR/SS}$

Pin Configuration and Functions

TPL9218-S
DFN2.5X2.5-10 Package
Top View

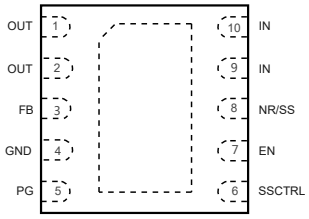


Table 1. Pin Functions: TPL9218

Pin No.	Pin Name	I/O	Description
7	EN	I	Regulator enable pin. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. For automatic startup, connect EN to IN directly.
3	FB	I	Output voltage feedback pin. Connect to an external resistor divider to adjust the output voltage. A 10-nF feed-forward capacitor from FB to OUT (as close as possible to the FB pin) is recommended to maximize regulator ac performance.
4	GND	–	Ground reference pin. Connect the GND pin to PCB ground plane directly.
9, 10	IN	I	Input voltage pin. A 10-μF or larger ceramic capacitor from IN to ground (as close as possible to the IN pin) is required to reduce the jitter from the previous-stage power supply.
8	NR/SS	I	Noise-reduction and soft-start pin. A 10-nF or larger capacitor from NR/SS to GND (as close as possible to NR/SS pin) is recommended to maximize ac performance.
1, 2	OUT	O	Regulated output voltage pin. A 22-μF or larger ceramic capacitor from OUT to ground (as close as possible to OUT pin) is required to ensure regulator stability.
5	PG	O	Open-drain power-good output pin. Leave the PG pin open when not used.
6	SSCTRL	I	Output voltage soft-start control pin. Connect this pin to GND or IN to set the NR/SS pin charging current. Connect SSCTRL pin to GND when not used.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
IN, EN, PG		−0.3	7	V
OUT		−0.3	V_{IN} + 0.3 (2)	V
NR/SS, FB		−0.3	3.6	V
SSCTRL		−0.3	V_{IN} + 0.3	V
T_J	Maximum Junction Temperature	−40	150	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) The absolute maximum rating is V_{IN} + 0.3 V or 7.0 V, whichever is smaller.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±4	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Typ	Max	Unit
IN	Input Voltage	1.4		6.5	V
OUT	Output Voltage	0.8		5.2	V
C_{IN}	Input Capacitor	10			μF
C_{OUT}	Output Capacitor	22			μF
$C_{NR/SS}$	NR/SS Capacitor		10	1000	nF
R_{PG}	Power-good Pull-up Resistor	10		100	kΩ
T_J	Junction Temperature Range	–40		125	°C

Thermal Information

Package Type	θ_{JA}	$\theta_{JC,BOTTOM}$	Unit
DFN2.5X2.5-10	60	6	°C/W

Electrical Characteristics

All test conditions: T_J = −40°C to +125°C (typical value at T_J = +25°C), V_{IN} = $V_{OUT(NOM)}$ + 0.4 V or 1.4 V, whichever is greater; $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1.1 V, C_{IN} = 10 µF, C_{OUT} = 10 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 0 nF, OUT connect to 50 Ω to ground, PG connected to 100 kΩ to OUT, unless otherwise noted.

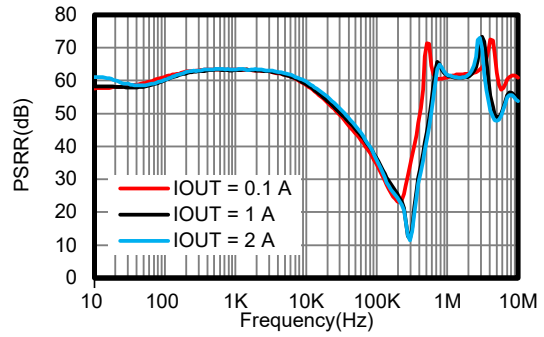
Parameter		Conditions	Min	Typ	Max	Unit
Supply Voltage and Current						
V_{IN} (1)	Input Supply Voltage Range		1.4		6.5	V
UVLO	Input Supply UVLO	V_{IN} rising			1.39	V
	Hysteresis			200		mV
I_{GND}	GND Pin Current	V_{IN} = 6.5 V, I_{OUT} = 5 mA		5	15	mA
		V_{IN} = 1.4 V, I_{OUT} = 2 A		5	15	mA
I_{SD}	Shutdown Current	V_{IN} = 6.5 V, V_{EN} = 0.5 V, PG = open			68	µA
Enable and Power Good						
$V_{IH(EN)}$	EN High-level Input Voltage	Device enable	1.1		6.5	V
$V_{IL(EN)}$	EN Low-level Input Voltage	Device disable	0		0.4	V
I_{EN}	EN Pin Current	V_{IN} = 6.5 V, V_{EN} = 0 V to 6.5 V	−0.5		0.5	µA
V_{PG}	PG Pin Threshold	V_{OUT} falling	82%	84%	88%	× V_{OUT}
	Hysteresis			2%		× V_{OUT}
$V_{OL(PG)}$	PG Low-level Output Voltage	V_{OUT} < V_{PG}, source 1 mA to PG pin			0.4	V
I_{PG}	PG Pin Leakage Current	V_{OUT} > V_{PG}, apply 6.5 V at PG pin			1	µA
Regulated Output Voltage and Current						
V_{OUT}	Output Voltage Range		0.8		5.2	V
	Accuracy (1)	V_{OUT} = 0.8 V to 5.2 V, I_{OUT} = 5 mA to 2 A	−1%		1%	
ΔV_{OUT}	Line Regulation	V_{IN} = 1.4 V to 6.5 V, I_{OUT} = 5 mA		0.03		mV/V
	Load Regulation	V_{IN} = 1.4 V, I_{OUT} = 5 mA to 2 A		0.7		mV/A
V_{FB}	Feedback Voltage			0.8		V
I_{FB}	FB Pin Leakage Current	V_{IN} = 6.5 V, stress V_{FB} = 0.8V	−100		100	nA
$V_{NR/SS}$	NR/SS Pin Voltage			0.8		V
$I_{NR/SS}$	NR/SS charging current	V_{IN} = 6.5 V, $V_{NR/SS}$ = GND, V_{SSCTRL} = GND	4	7.8	9	µA
		V_{IN} = 6.5 V, $V_{NR/SS}$ = GND, V_{SSCTRL} = VIN	65	100	150	µA
I_{LIM}	Output Current Limit	V_{IN} = $V_{OUT(NOM)}$ + 0.4 V, V_{OUT} is forced at 90% × $V_{OUT(NOM)}$	2.1	3.4		A
I_{SC}	Short-circuit Current Limit	R_{LOAD} ≤ 20 mΩ		1.5		A
R_{DIS}	Output Discharge Resistance	V_{EN} = 0		250		Ω
V_{DO}	Dropout Voltage	V_{IN} = 1.4 V, I_{OUT} = 1 A, V_{FB} = 0.8 V − 3%		40	100	mV
		V_{IN} = 1.4 V, I_{OUT} = 2 A, V_{FB} = 0.8 V − 3%		80	200	mV
		V_{IN} = 5.4 V, I_{OUT} = 2 A, V_{FB} = 0.8 V − 3%		80	200	mV
		V_{IN} = 5.6 V, I_{OUT} = 2 A, V_{FB} = 0.8 V − 3%		80	200	mV

Parameter		Conditions		Min	Typ	Max	Unit
PSRR and Noise							
PSRR	Power Supply Ripple Rejection	V_{IN} = 2 V, V_{OUT} = 1.2 V, I_{OUT} = 2 A, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF	f = 1 kHz		70		dB
			f = 10 kHz		60		dB
			f = 500 kHz		40		dB
Noise	Output Noise Voltage	BW = 10 Hz to 100 kHz, V_{IN} = 1.4 V, V_{OUT} = 0.8 V, I_{OUT} = 2 A, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF			6		μV_{RMS}
		BW = 10 Hz to 100 kHz, V_{IN} = 5.4 V, V_{OUT} = 5 V, I_{OUT} = 2 A, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF			10		μV_{RMS}
Temperature Range							
T_{SD}	Thermal Shutdown Threshold	Temperature increasing			160		°C
	Hysteresis				20		°C
T_J	Operating Temperature			−40		125	°C

(1) Minimum V_{IN} = $V_{OUT(NOM)}$ + V_{DO} or 1.4 V, whichever is greater.
(2) Resistor tolerances are not included. The device is not tested under conditions where V_{IN} > V_{OUT} + 2.5 V and I_{OUT} = 2 A because the power dissipation is higher than the maximum rating of the package.

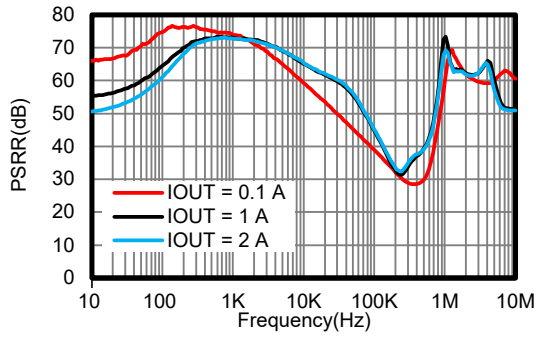
Typical Performance Characteristics

All test conditions: T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.4 V or 1.4 V, whichever is greater; $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1.1 V, C_{IN} = 10 µF, C_{OUT} = 10 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 0 nF, OUT connect to 50 Ω to ground, PG connected to 100 kΩ to OUT, unless otherwise noted.



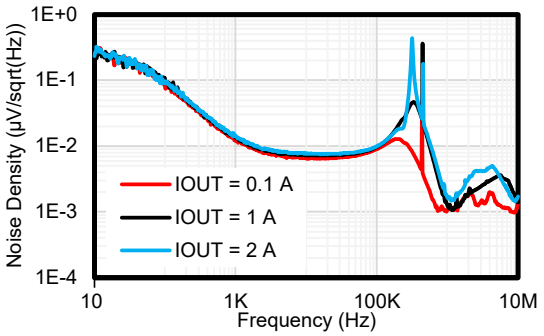
V_{IN} = 1.4 V, V_{OUT} = 0.8 V, C_{IN} = 10 µF, C_{OUT} = 22 µF, $C_{NR/SS}$ = 10 nF, C_{FF}= 10 nF

Figure 1. PSRR



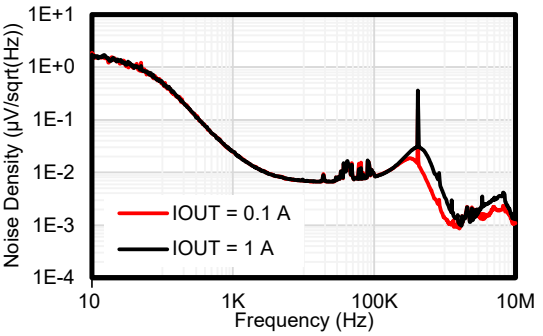
V_{IN} = 5.5 V, V_{OUT} = 5.2 V, C_{IN} = 10 µF, C_{OUT} = 22 µF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF

Figure 2. PSRR



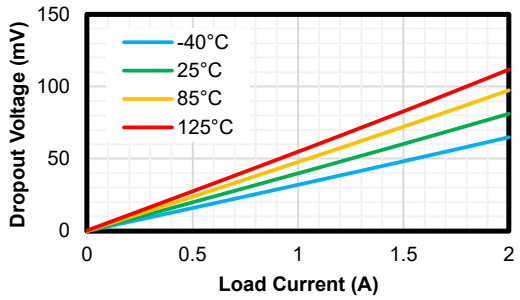
V_{IN} = 1.4 V, V_{OUT} = 0.8 V, C_{IN} = 10 µF, C_{OUT} = 22 µF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF

Figure 3. Noise



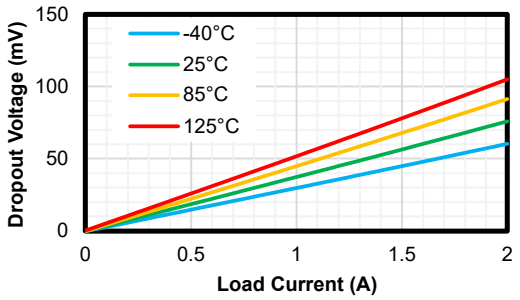
V_{IN} = 5.5 V, V_{OUT} = 5.2 V, C_{IN} = 10 µF, C_{OUT} = 22 µF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF

Figure 4. Noise



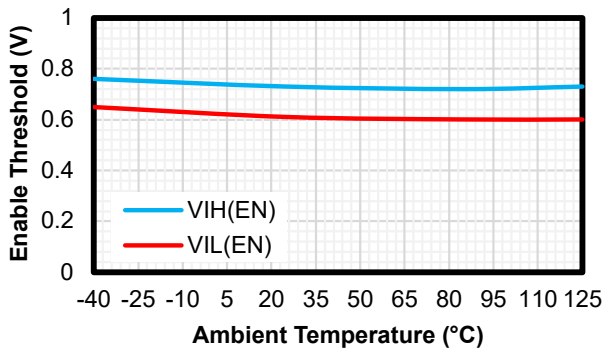
V_{IN} = 1.4 V

Figure 5. Dropout Voltage



V_{IN} = 5.4 V

Figure 6. Dropout Voltage



V_{IN} = 1.4 V

Figure 7. Enable Threshold

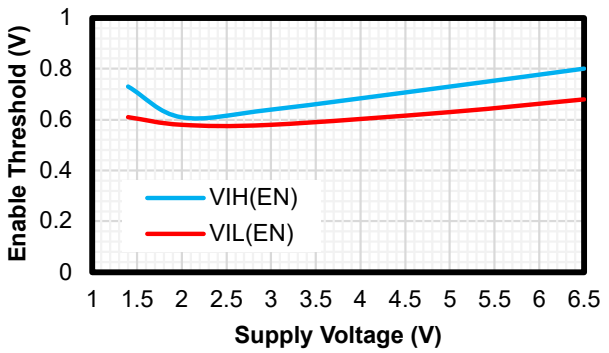


Figure 8. Enable Threshold

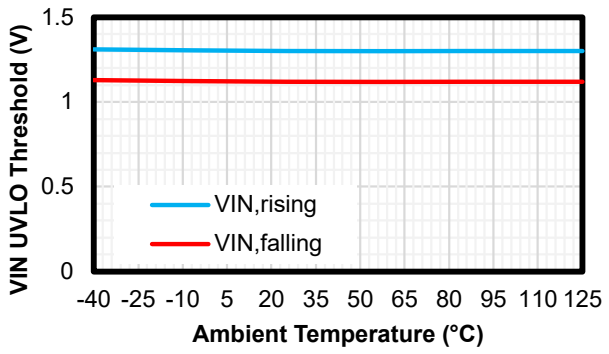


Figure 9. V_{IN} UVLO

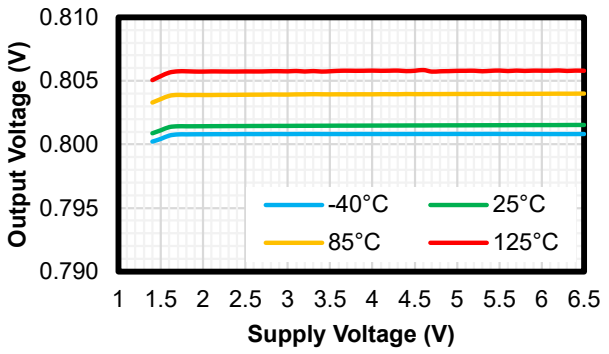


Figure 10. Line Regulation

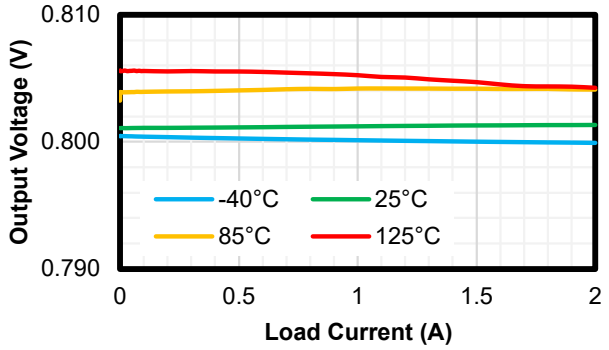
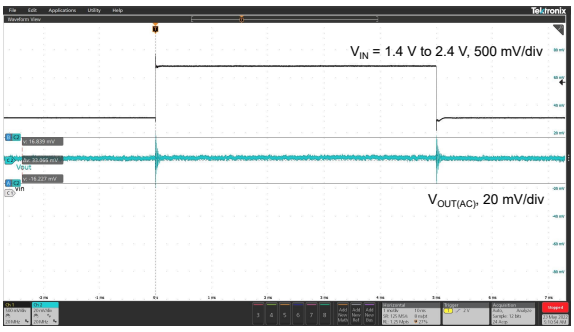
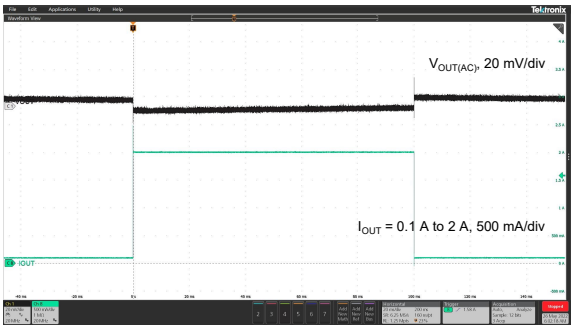


Figure 11. Load Regulation



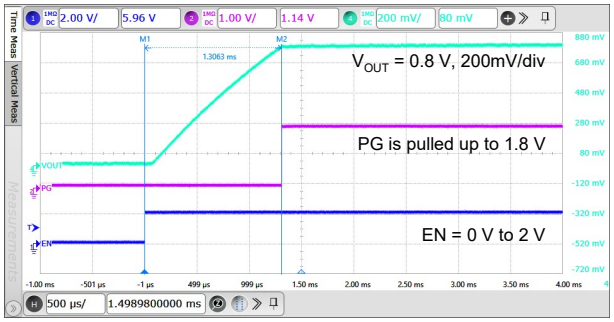
V_{IN} = 1.4 V to 2.4 V, V_{OUT} = 0.8 V, I_{OUT} = 1 A, C_{OUT} = 22 µF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF

Figure 12. Line Transient



V_{IN} = 1.4 V, V_{OUT} = 0.8 V, I_{OUT} = 0.1 A to 2 A, C_{OUT} = 10 µF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF

Figure 13. Load Transient



V_{IN} = 1.4 V, V_{OUT} = 0.8 V, C_{OUT} = 22 µF, $C_{NR/SS}$ = 10 nF, no load

Figure 14. Startup

Detailed Description

Overview

The TPL9218 series of products are 2-A high-current, 3.3-μV_{RMS} low-noise, high-PSRR, and high-accuracy linear regulators with typically 80-mV ultra-low dropout voltage in the 2-A load condition. The TPL9218 product supports adjustable output voltage ranging from 0.8 V to 5.2 V with external resistor dividers.

Ultra-low noise, high-PSRR, and high-output current capabilities make the TPL9218 series an ideal power supply for noise-sensitive applications, such as high-speed communication facilities, test and measurement devices, or high-definition imaging equipment. Accurate output voltage tolerance, output voltage remote sensing, excellent transient response, and flexible soft-start control ensure the TPL9218 series an optimal power supply for large-scale processors and digital loads, such as CPU, ASIC, FPGA, CPLD, and DSP.

Functional Block Diagram

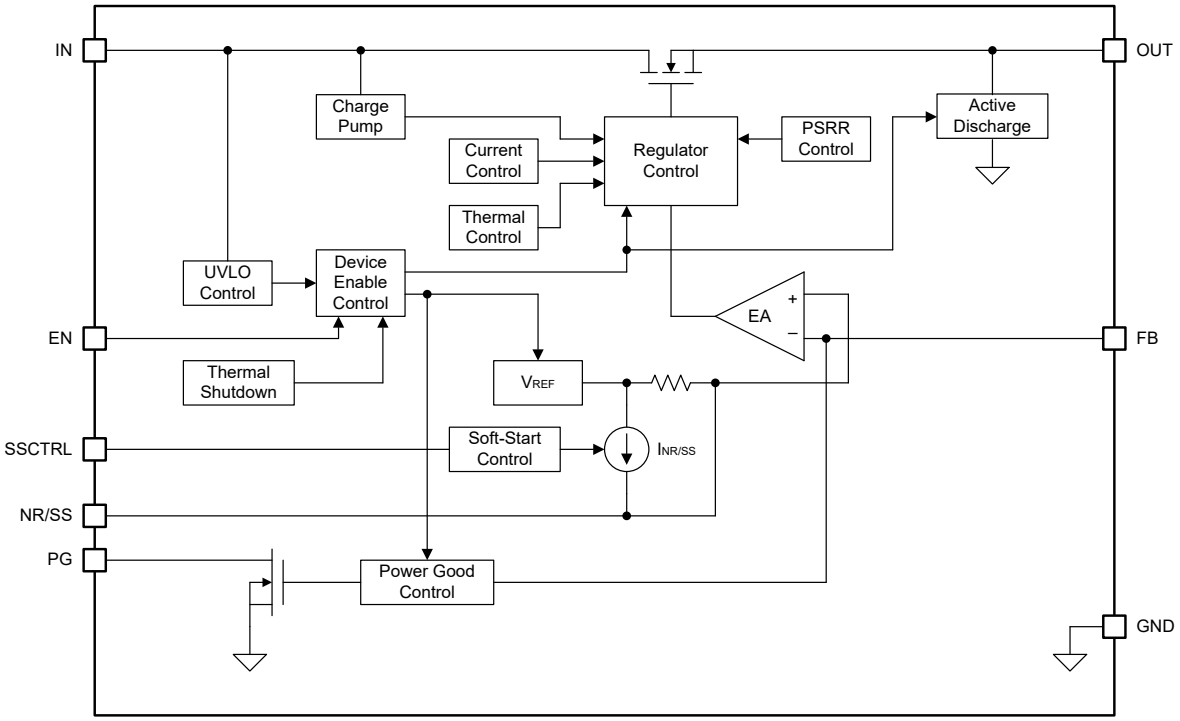


Figure 15. Functional Block Diagram

Feature Description

Enable (EN)

The TPL9218 series provides a device enable pin (EN) to enable or disable the device. Connect the enable pin to the GPIO of an external digital logic control circuit to control the device. When the V_{EN} voltage falls below $V_{IL(EN)}$, the LDO device turns off. When the V_{EN} ramps above $V_{IH(EN)}$, the LDO device turns on.

The TPL9218 series also integrates an active discharge function. During normal operation, when the enable pin is pulled down below $V_{IL(EN)}$, the output voltage is discharged through the internal resistive path.

Under-Voltage Lockout (UVLO)

The TPL9218 series uses an under-voltage lockout circuit to keep the output shut-off until the internal circuitry operates properly.

Adjustable Output Voltage Setting

The TPL9218 series also provides an adjustable output voltage option. Using external resistor dividers, the output voltage of TPL9218 series is determined by the value of the resistors R1 and R2 in Figure 16. Use Equation 1 to calculate the output voltage.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

Where,

- the feedback voltage V_{FB} is 0.8 V
- R1 is the high-side feedback resistor
- R2 is the low-side feedback resistor

Table 2 provides a list of recommended resistor combinations to achieve the common output voltage values.

Table 2. External Resistor Combinations

Target Output Voltage (V)	External Resistors Divider		Calculated Output Voltage (V)
	R1 (kΩ)	R2 (kΩ)	
0.80	0	Open	0.800
0.81	2	160	0.810
0.82	4.02	160	0.820
0.83	6.04	160	0.830
0.84	8.06	160	0.840
0.85	10	160	0.850
0.86	12	160	0.860
0.87	12.4	143	0.869
0.88	12.4	124	0.880
0.89	12	107	0.890
0.90	12.4	100	0.899
0.95	12.4	66.5	0.949
1.00	12.4	49.9	0.999
1.10	12.4	33.2	1.099
1.20	12.4	24.9	1.198
1.50	12.4	14.3	1.494
1.80	12.4	10	1.792
1.90	12.1	8.87	1.891
2.50	12.4	5.9	2.481
2.85	12.1	4.75	2.838
3.00	12.1	4.42	2.990
3.30	11.8	3.74	3.324

Target Output Voltage (V)	External Resistors Divider		Calculated Output Voltage (V)
	R1 (kΩ)	R2 (kΩ)	
3.60	12.1	3.48	3.582
4.50	11.8	2.55	4.502
5.00	12.4	2.37	4.986

Output Soft-Start Control (NR/SS)

The TPL9218 series integrates an adjustable soft-start function to control the output voltage ramp-up slew rate and start-up time. By selecting the external capacitor at the NR/SS pin ($C_{NR/SS}$), the output start-up time can be calculated with Equation 2

$$t_{STRATUP} = 1.25 \times \frac{V_{NR/SS} \times C_{NR/SS}}{I_{NR/SS}} \quad (2)$$

Where,

- the typical value of $V_{NR/SS}$ is 0.8 V
- the typical value of $I_{NR/SS}$ is 7.8 μA
- $C_{NR/SS}$ is the external capacitor at the NR/SS pin

Charge Pump Noise

The TPL9218 series integrates a charge pump to improve the PSRR and transient response under low input voltage conditions. The TPL9218 also generates a minimal amount of noise at the frequency of around 15 MHz. It is recommended to use 10-nF to 100-nF bypass capacitors close to the load a ferrite bead between the LDO output and the load input capacitors, forming a pi-filter to reduce the high-frequency noise level.

Power Good (PG)

The TPL9218 series integrates an open-drain output power good indicator. Connect the PG pin to a pull-up voltage through a resistor from 10 kΩ to 100 kΩ if the power good function is used. Or left the PG pin open if it is not used.

After regulator startup, the PG pin keeps low impendence until the output voltage reaches the power good threshold $V_{PG,TH}$. When the output voltage is higher than $V_{PG,TH}$, the PG pin turns to high output impedance, and PG is pulled up to a high voltage level to indicate the output voltage is ready.

Output Active Discharge

The TPL9218 series integrates an output discharge path from OUT to GND. When the device is disabled, and either EN or VIN is lower than the turn-on threshold, the output will actively discharge the output voltage through an internal resistor of several hundred ohms.

Do not rely on this active discharge circuit for discharging large output capacitors when the input voltage falls below the output voltage. Reverse current flow through the internal power MOSFET can permanently damage the device, and external current protection is essential in this condition.

Over-Current Protection and Short-to-Ground Protection

The TPL9218 series integrates an internal current limit that helps to protect the device during fault conditions.

- When the output is pulled down below the target output voltage, over-current protection starts to work and limit the output current to a typical value of 3.4 A.
- When the output is shorted to ground directly, short-to-ground protection starts to work and limit the output current to I_{SC}.

Under over-current conditions, the internal junction temperature ramps up quickly. When the junction temperature is high enough, it will cause over-temperature protection.

Over-Temperature Protection

The recommended operating junction temperature range is from −40°C to 125°C. When the junction temperature is between 125°C and the thermal shutdown (TSD) threshold, the regulator can still work well, but will reduce the device lifetime for long-term use.

The over-temperature protection works when the junction temperature exceeds the thermal shutdown (TSD) threshold, which turns off the regulator immediately. When the device cools down and the junction temperature falls below a value, which equals to thermal shutdown threshold minus thermal shutdown hysteresis, the regulator turns on again.

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPL9218 series of products are 2-A high-current, low-noise, high-PSRR, and high-accuracy linear regulators with a maximum 200-mV ultra-low dropout voltage in the 2-A load condition. The following application schematic shows the typical usage of the TPL9218.

Typical Application

Adjustable Output Operation

Figure 16 shows the typical application schematics of the TPL9218 series with adjustable output operation. Refer to the section Adjustable Output Voltage Setting to set the output voltage.

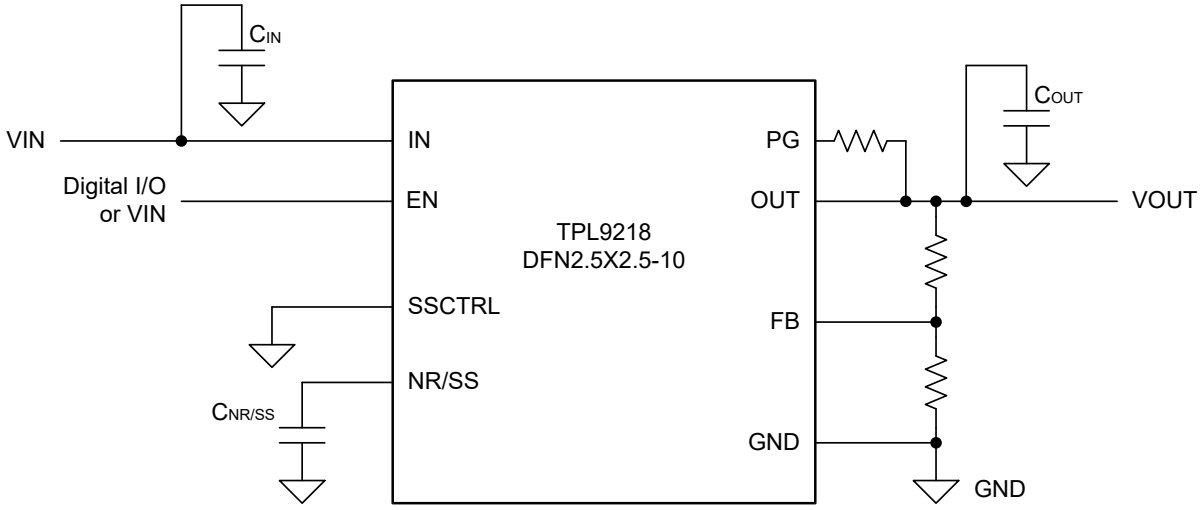


Figure 16. Adjustable Output

Input Capacitor and Output Capacitor

The TPL9218 series is designed to be stable with low equivalent series resistance (ESR) ceramic capacitors at the input, output, and noise-reduction pin (NR/SS). It is recommended to use ceramic capacitors with X7R-, X5R-, and COG-rated dielectric materials to get good capacitive stability across corresponding temperature ranges.

3PEAK recommends adding a 10-µF or greater capacitor with a 0.1-µF bypass capacitor in parallel at the IN pin to keep the input voltage stable. The voltage rating of the capacitors must be greater than the maximum input voltage.

To ensure loop stability, the TPL9218 series requires a 10-µF or greater output capacitor. 3PEAK recommends selecting an X7R-type 22-µF ceramic capacitor with low ESR over temperature.

Both input capacitors and output capacitors must be placed as close to the device pins as possible.

Power Dissipation

During normal operation, LDO junction temperature should not exceed 125°C. Using below equations to calculate the power dissipation and estimate the junction temperature.

The power dissipation can be calculated using Equation 3 .

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad (3)$$

The junction temperature can be estimated using Equation 4. θ_{JA} is the junction-to-ambient thermal resistance.

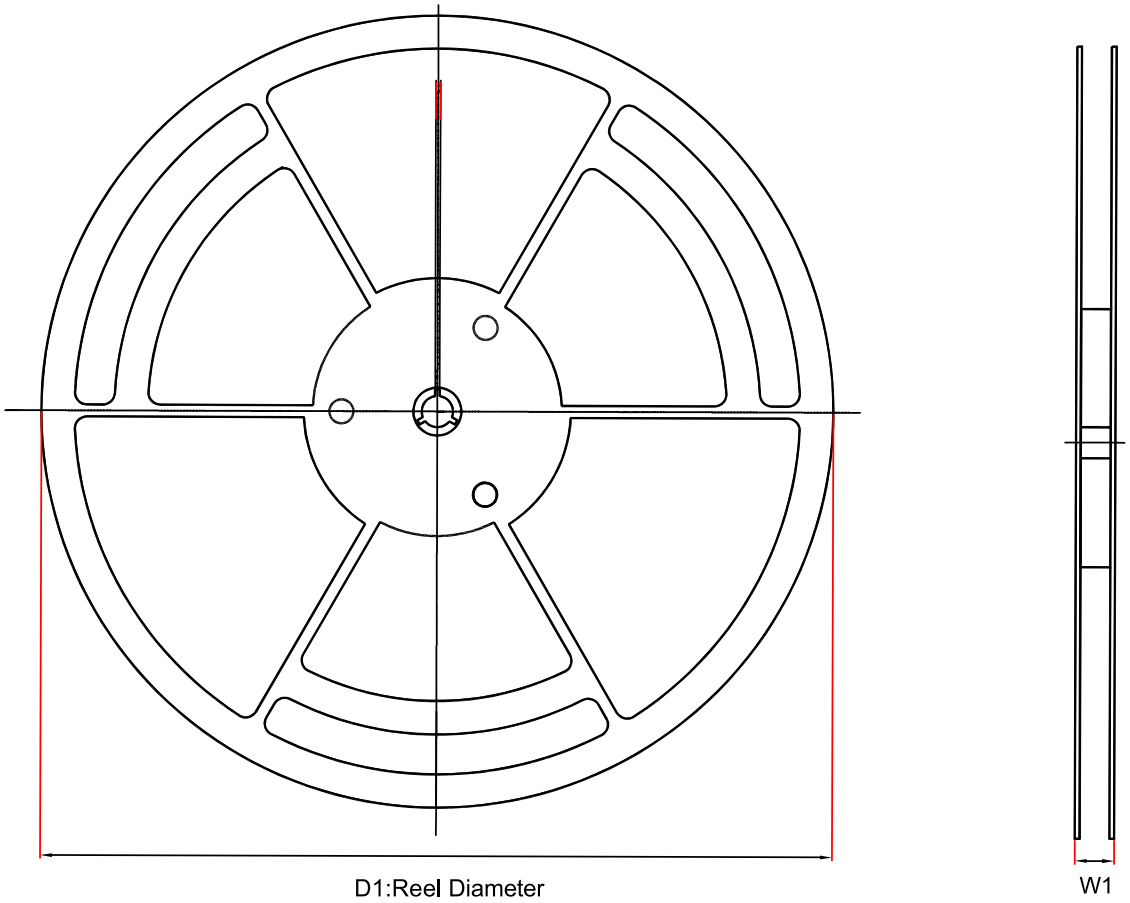
$$T_J = T_A + P_D \times \theta_{JA} \quad (4)$$

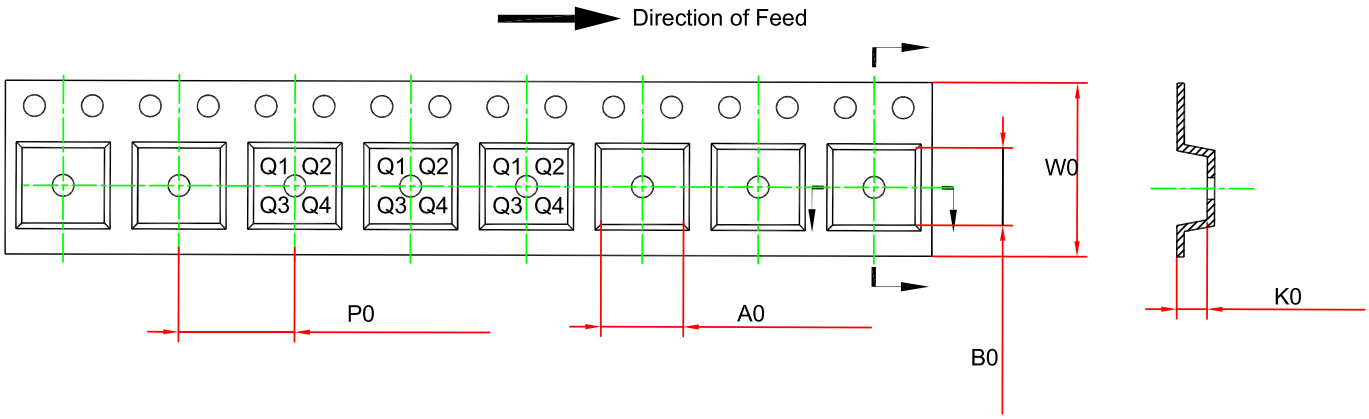
Layout

Layout Guideline

- Both input capacitors and output capacitors must be placed to the device pins as close as possible, and the vias between capacitors and device power pins must be avoided.
- It is recommended to bypass the input pin to ground with a 0.1-μF bypass capacitor. The loop area formed by the bypass capacitor connection, the IN pin and the GND pin of the system must be as small as possible.
- It is recommended to use wide and thick copper to minimize I×R drop and heat dissipation.
- Exposed pad must be connected to the PCB ground plane directly, the copper area must be as large as possible.

Tape and Reel Information



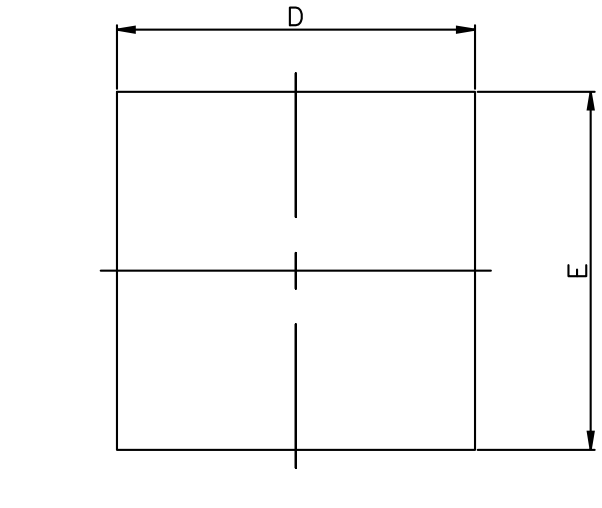


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPL9218AD-DF5R-S	DFN2.5X2.5-10	180	12.3	2.7	2.7	0.7	4	8	Q2

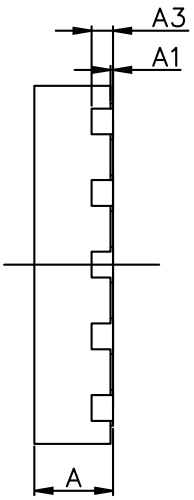
Package Outline Dimensions

DFN2.5X2.5-10

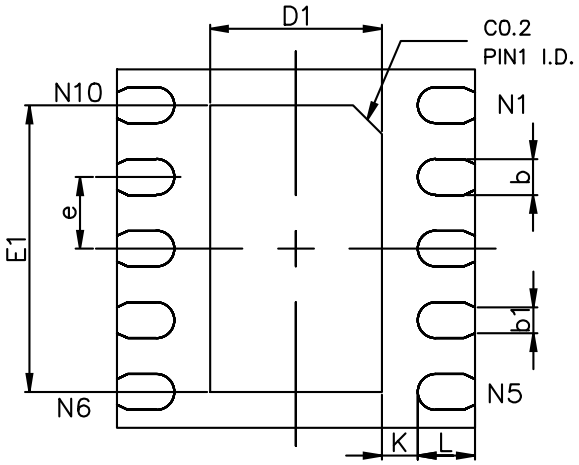
Package Outline Dimensions DF5(DFN2.5X2.5-10-A)



TOP VIEW



SIDE VIEW



BOTTOM VIEW

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.500	0.600	0.020	0.024
A1	0.000	0.050	0.000	0.002
b1	0.180 REF		0.007 REF	
b	0.200	0.300	0.008	0.012
A3	0.100	0.200	0.004	0.008
D	2.400	2.600	0.094	0.102
D1	1.100	1.300	0.043	0.051
E	2.400	2.600	0.094	0.102
E1	1.900	2.100	0.075	0.083
e	0.500 BSC		0.020BSC	
L	0.350	0.450	0.014	0.018

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPL9218AD-DF5R-S	−40 to 125°C	DFN2.5X2.5-10	L91	MSL3	4,000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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