3-A Output, High-PSRR, Low-Noise LDO Regulator

Features

- Input Voltage Range
  - Without BIAS: 1.4 V to 6.5 V
  - With BIAS: 1.1 V to 6.5 V
- Output Voltage Options:
  - Fixed Output Voltage: 0.5 V to 3.65 V
  - Adjustable Output Voltage: 0.5 V to 5.2 V
- ±1% Output Accuracy over Line Regulation, Load Regulation, and Operating Temperature Range With BIAS
- 3-A Maximum Output Current
- Low Dropout Voltage: 300 mV Maximum at 3 A
- High PSRR:
  - 65 dB at 1 kHz
  - 60 dB at 1 MHz
- 4-μV_{RMS}Output Voltage Noise
- Excellent Transient Response
- Enable and Adjustable Soft-Start Control
- Open-Drain Power-Good (PG) Output
- Stable with 10-µF or Greater Ceramic Output Capacitor
- Over-Current Protection
- Over-Temperature Protection
- Temperature Range: –40°C to +125°C
- Package Options:
  - QFN3.5X3.5-20

Applications

- Wireless Communication: CPU, ASIC, FPGA, CPLD, DSP
- High-Performance Analog: ADC, DAC, LVDS, VCO
- Noise-Sensitive Imaging: CMOS Sensors, Video ASICs

Description

The TPL9305 is a 3-A high-current, 4-μV_{RMS} low-noise, high-PSRR, high-accuracy linear regulator with maximum 300-mV ultra-low dropout voltage at 3-A load condition. The TPL9305 supports both fixed output voltage ranging from 0.5 V to 3.65 V and adjustable output voltage ranging from 0.5 V to 5.2 V with an external resistor divider.

Ultra-low noise, high PSRR, and high-output-current capabilities make the TPL9305 an ideal power supply for noise-sensitive applications, such as high-speed communication facilities, test and measurement devices, or high-definition imaging equipment. Accurate output voltage tolerance, output voltage remote sensing, excellent transient response, and adjustable soft-start control ensure the TPL9305 an optimal power supply for the large-scale processors or digital loads, such as ASIC, FPGA, CPLD, and DSP.

The TPL9305 provides a 20-pin QFN3.5X3.5 package with guaranteed operating junction temperature ranging (T_J) from −40°C to +125°C.

Typical Application Circuit

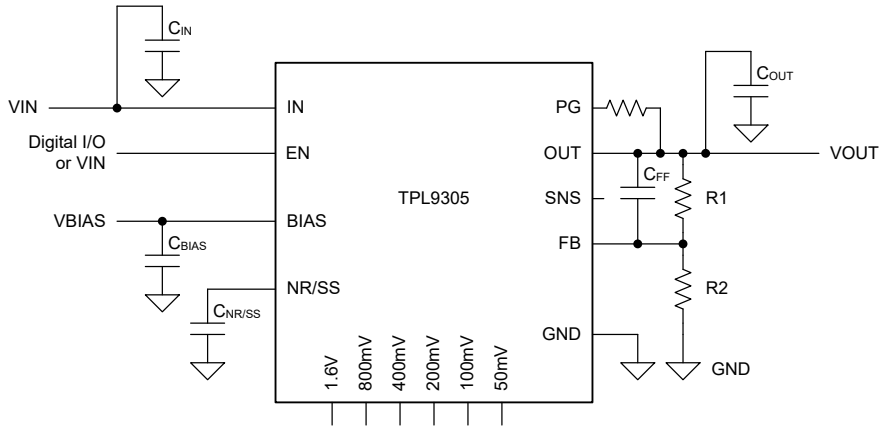


Table of Contents

Features 1
Applications 1
Description 1
Typical Application Circuit 1
Product Family Table 3
Revision History 3
Pin Configuration and Functions 4
Specifications 5
Absolute Maximum Ratings (1) 5
ESD, Electrostatic Discharge Protection 5
Recommended Operating Conditions 6
Thermal Information 6
Electrical Characteristics 7
Typical Performance Characteristics 10
Detailed Description 14
Overview 14
Functional Block Diagram 14
Feature Description 14
Application and Implementation 19
Application Information 19
Typical Application 19
Layout 21
Layout Guideline 21
Tape and Reel Information 22
Package Outline Dimensions 23
QFN3.5X3.5-20 23
Order Information 24
IMPORTANT NOTICE AND DISCLAIMER 25

Product Family Table

Order Number	Output Voltage (V)	Package
TPL9305AD-QF6R-S	Adjustable (0.5 V to 5.2 V)	QFN3.5X3.5-20

Revision History

Revision	Notes
Rev.Pre.0	Preliminary revision.
Rev.A.0	Initial released.
Rev.A.1	Corrected data in Electrical Characteristics, Typical Performance Characteristics and Feature Description.
Rev.A.2	• Corrected $\theta_{JC,\ Bottom}$ 16.9 to $\theta_{JC,\ TOP}$ 43.8 °C/W. • Updated the min spec of $I_{NR/SS}$ from 6 to 4 uA.

Pin Configuration and Functions

TPL9305
QFN3.5X3.5-20 Package
Top View

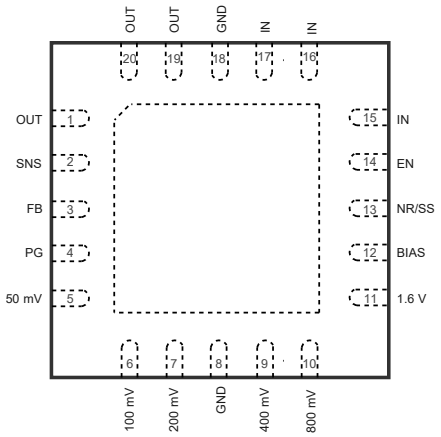


Table 1. Pin Functions: TPL9305

Pin No.	Pin Name	I/O	Description
5, 6, 7, 9, 10, 11	50mV, 100mV, 200mV, 400mV, 800mV, 1.6V	I	Fixed output voltage configuration pins. Connect these pins to ground to increase the output voltage. Leave these pins open when using the external resistor divider.
12	BIAS	I	BIAS input pin. A 10-μF capacitor or larger must be connected between this pin and ground. Leave BIAS pin open or tied to ground when not used.
14	EN	I	Regulator enable pin. Drive EN high to turn on the regulator; drive EN low to turn off the regulator.
3	FB	I	Output voltage feedback pin. Connect to an external resistor divider to adjust the output voltage. A 10-nF feed-forward capacitor from FB to OUT (as close as possible to FB pin) is recommended to maximize regulator ac performance.
8, 18	GND	–	Ground reference pin. Connect the GND pin to PCB ground plane directly.
15, 16, 17	IN	I	Input supply pin. A 10-μF or greater ceramic capacitor from IN to ground (as close as possible to IN pin) is required.
13	NR/SS	I	Noise-reduction and soft-start control pin. A 10-nF or greater capacitor from NR/SS to GND (as close as possible to NR/SS pin) is required.
1, 19, 20	OUT	O	Regulated output voltage pin. A 10-μF or greater ceramic capacitor from OUT to ground (as close as possible to OUT pin) is required.
4	PG	O	Open-drain power-good output pin. Leave the PG pin open when not used.
2	SNS	I	Output voltage sense input pin. Connect this pin to the load side of the output trace only when using the fixed output voltage. Leave SNS pin open when using the external resistor divider.

(1) Exposed PAD must be connected to a large-area ground plane to maximize the thermal performance.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
IN, BIAS, EN, PG		−0.3	7	V
OUT, SNS		−0.3	V_{IN} + 0.3	V
NR/SS, FB		−0.3	3.6	V
50 mV, 100 mV, 200 mV, 400 mV, 800 mV, 1.6 V		−0.3	V_{OUT} + 0.3	V
T_J	Maximum Junction Temperature	−40	150	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) All voltage values are with respect to GND.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±4	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Typ	Max	Unit
IN	Input Voltage	1.1		6.5	V
BIAS	BIAS Voltage	3		6.5	V
EN	Enable Voltage	0		6.5	V
OUT	Output Voltage	0.5		5.2	V
C_{IN}	Input Capacitor	10			μF
C_{OUT}	Output Capacitor	10	22		μF
C_{FF}	Feed-forward Capacitor		10	1000	nF
$C_{NR/SS}$	NR/SS Capacitor		10		nF
R_{PG}	Power-good Pull-up Resistor	10		100	kΩ
R_1	High-Side Resistor of the Resistor Divider		12.1		kΩ
R_2	Low-Side Resistor of the Resistor Divider			160	kΩ
T_J	Junction Temperature Range	−40		125	°C

Thermal Information

Package Type	θ_{JA}	$\theta_{JC,TOP}$	Unit
QFN3.5X3.5-20	46.1	43.8	°C/W

Electrical Characteristics

All test conditions: T_J = −40°C to +125°C (typical value at T_J = +25°C), V_{IN} = $V_{OUT(NOM)}$ + 0.4 V or 1.4 V, whichever is greater; V_{BIAS} = open, $V_{OUT(NOM)}$ = 0.5 V, V_{EN} = 1.1 V, C_{IN} = 10 µF, C_{OUT} = 10 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 0 nF, OUT connect to 50 Ω to ground, PG connected to 100 kΩ to OUT, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
Supply Input Voltage and Current						
V_{IN} (1)	Input Voltage Range		1.1		6.5	V
V_{BIAS}	Bias Voltage Range	V_{IN} = 1.1 V	3		6.5	V
$UVLO_{IN1}$	V_{IN} UVLO with BIAS	V_{IN} rising with V_{BIAS} = 3 V			1.09	V
	Hysteresis	V_{BIAS} = 3 V		200		mV
$UVLO_{IN2}$	V_{IN} UVLO without BIAS	VIN rising			1.39	V
	Hysteresis			200		mV
$UVLO_{BIAS}$	V_{BIAS} UVLO	V_{BIAS} rising, V_{IN} = 1.1 V			2.9	V
	Hysteresis	V_{IN} = 1.1 V		200		mV
I_{GND}	Ground Current	V_{IN} = 6.5 V, I_{OUT} = 5 mA		5	15	mA
		V_{IN} = 1.4 V, I_{OUT} = 3 A		5	15	mA
		V_{IN} = 1.1 V, V_{BIAS} = 3 V, I_{OUT} = 3 A		5	15	mA
I_{SD}	Shutdown Current	V_{IN} = 6.5 V, V_{EN} = 0.4 V, PG = open			68	µA
I_{BIAS}	BIAS Pin Current	V_{IN} = 1.1 V, V_{BIAS} = 6.5 V, I_{OUT} = 3 A		2.5	5	mA
Enable and Power Good						
$V_{IH(EN)}$	EN High-Level Input	Device enable	1.1		6.5	V
$V_{IL(EN)}$	EN Low-Level Input	Device disable	0		0.4	V
I_{EN}	EN Leakage Current	V_{IN} = 6.5 V, V_{EN} = 0 V to 6.5 V	−0.2		0.2	µA
V_{PG}	PG Threshold	V_{OUT} falling		81%		× V_{OUT}
	Hysteresis			2%		× V_{OUT}
$V_{OL(PG)}$	PG Low-Level Output	V_{OUT} < V_{PG}, source 1 mA to PG pin			0.4	V
I_{PG}	PG Leakage Current	V_{OUT} > V_{PG}, apply 6.5 V at PG pin			1	µA

(1) Minimum V_{IN} = $V_{OUT(NOM)}$ + V_{DO} or 1.4 V or 1.1 V with V_{BIAS} = 3 V, whichever is greater.

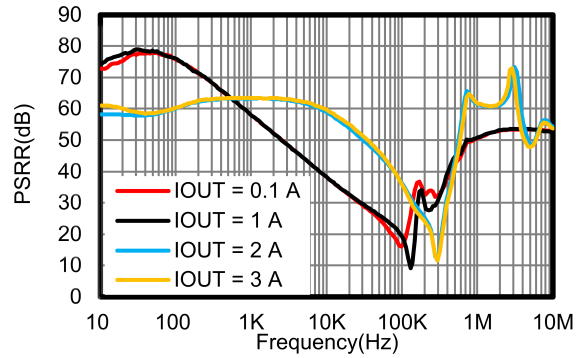
Parameter		Conditions		Min	Typ	Max	Unit
Regulated Output Voltage and Current							
V_{FB}	Feedback Voltage				0.5		V
I_{FB}	FB Leakage Current	V_{IN} = 6.5 V, stress V_{FB} = 0.5 V		−100		100	nA
$V_{NR/SS}$	NR/SS Voltage				0.5		V
$I_{NR/SS}$	NR/SS Charging Current	V_{IN} = 6.5 V, $V_{NR/SS}$ = GND		4	5.6	9	μA
V_{OUT}	Output Voltage Range	Fixed		0.5		3.65	V
		Adjustable		0.5		5.2	V
	Accuracy (2)(3)	V_{OUT} = 0.5 V to 5.2 V, I_{OUT} = 5 mA to 3 A		−1%		1%	
ΔV_{OUT}	Line Regulation	V_{IN} = 1.4 V to 6.5 V, I_{OUT} = 5 mA			0.03		mV/V
	Load Regulation	V_{IN} = 1.1 V, V_{BIAS} = 3 V to 6.5 V, I_{OUT} = 5 mA to 3 A			0.7		mV/A
		I_{OUT} = 5 mA to 3 A			0.8		mV/A
V_{DO}	Dropout Voltage without BIAS	V_{IN} = 1.4 V, I_{OUT} = 1 A, V_{FB} = 0.5 V – 3%			40	100	mV
		V_{IN} = 1.4 V, I_{OUT} = 2 A, V_{FB} = 0.5 V – 3%			80	200	mV
		V_{IN} = 1.4 V, I_{OUT} = 3 A, V_{FB} = 0.5 V – 3%			120	300	mV
		V_{IN} = 5.6 V, I_{OUT} = 3 A, V_{FB} = 0.5 V – 3%			120	300	mV
	Dropout Voltage with BIAS	V_{IN} = 1.1 V, V_{BIAS} = 5 V, I_{OUT} = 1 A, V_{FB} = 0.5 V – 3%			40	100	mV
		V_{IN} = 1.1 V, V_{BIAS} = 5 V, I_{OUT} = 2 A, V_{FB} = 0.5 V – 3%			80	200	mV
		V_{IN} = 1.1 V, V_{BIAS} = 5 V, I_{OUT} = 3 A, V_{FB} = 0.5 V – 3%			120	300	mV
I_{LIM}	Output Current Limit	V_{OUT} forced at 0.9 × $V_{OUT(NOM)}$		3.7	4.7		A
PSRR and Noise							
PSRR	Power Supply Ripple Rejection	I_{OUT} = 3 A, $C_{NR/SS}$ = 100 nF, C_{FF} = 100 nF, C_{OUT} = 47 μF || 10μF || 10μF	f = 1 kHz, V_{BIAS} = 3 V		65		dB
			f = 1 MHz, V_{BIAS} = 3 V		60		dB
			f = 1 kHz		65		dB
			f = 1 MHz		60		dB

(1) Minimum V_{IN} = $V_{OUT(NOM)}$ + V_{DO} or 1.4 V or 1.1 V with V_{BIAS} = 3 V, whichever is greater.
(2) External resistor tolerances are not included.
(3) The device is not tested under conditions where V_{IN} > V_{OUT} + 1.7 V and I_{OUT} = 3 A, because the power dissipation is higher than the maximum rating of the package.

Parameter		Conditions	Min	Typ	Max	Unit
PSRR and Noise						
V_N	Output Noise Voltage	BW = 10 Hz to 100 kHz, V_{IN} = 1.1 V, V_{OUT} = 0.5 V, V_{BIAS} = 5 V, I_{OUT} = 3 A, $C_{NR/SS}$ = 100 nF, C_{FF} = 10 nF, C_{OUT} = 47 µF || 10µF || 10µF		4		μV_{RMS}
		BW = 10 Hz to 100 kHz, V_{OUT} = 5 V, I_{OUT} = 3 A, $C_{NR/SS}$ = 100 nF, C_{FF} = 100 nF, C_{OUT} = 47 µF || 10µF || 10µF		8		μV_{RMS}
		BW = 10 Hz to 100 kHz, V_{OUT} = 5 V, I_{OUT} = 3 A, $C_{NR/SS}$ = 100 nF, C_{FF} = 10 nF, C_{OUT} = 47 µF || 10µF || 10µF		10		μV_{RMS}
Temperature Range						
T_{SD}	Thermal Shutdown	Temperature increasing		160		°C
I_{FB}	Hysteresis			20		°C

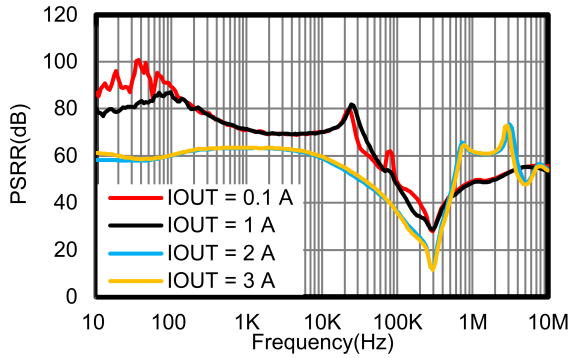
Typical Performance Characteristics

All test conditions: T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.4 V or 1.4 V, whichever is greater; $V_{OUT(NOM)}$ = 0.5 V, V_{EN} = 1.1 V, C_{IN} = 10 µF, C_{OUT} = 10 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 0 nF, OUT connect to 50 Ω to ground, PG connected to 100 kΩ to OUT, unless otherwise noted.



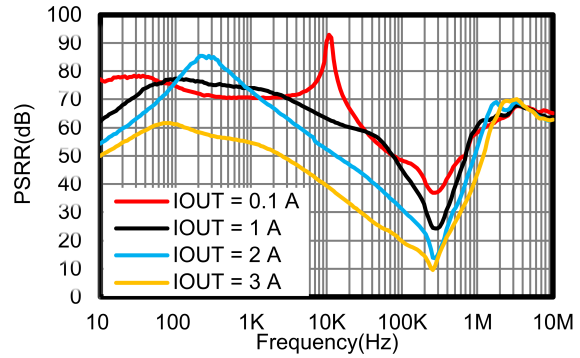
V_{IN} = 1.4 V, V_{OUT} = 0.5 V = 10 nF

Figure 1. PSRR



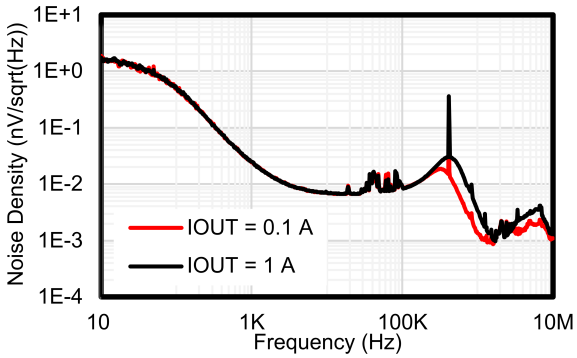
V_{IN} = 1.1 V, V_{BIAS} = 3 V, V_{OUT} = 0.5 V

Figure 2. PSRR



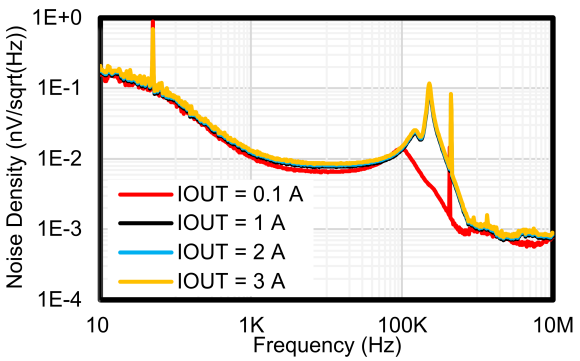
V_{IN} = 5.5 V, V_{OUT} = 5.2 V, without V_{BIAS}

Figure 3. PSRR



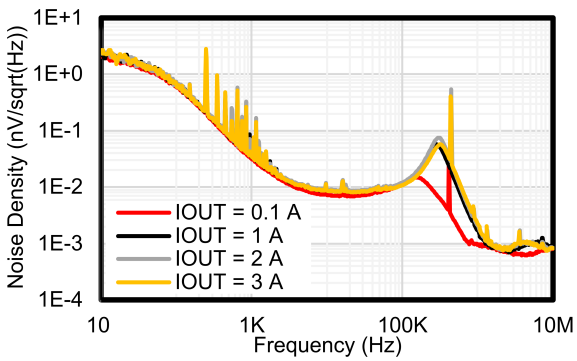
V_{IN} = 1.1 V, V_{OUT} = 0.5 V

Figure 4. V_{BIAS} PSRR



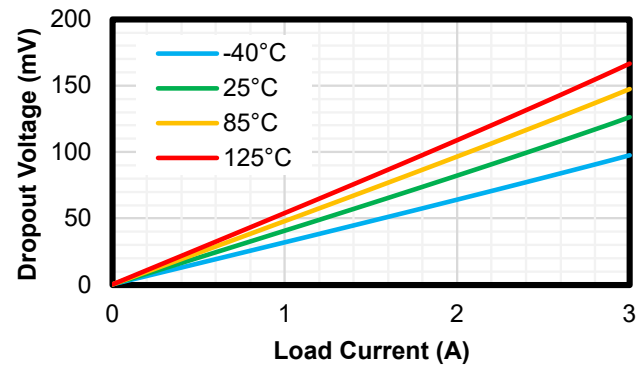
V_{IN} = 1.4 V, V_{OUT} = 0.5 V

Figure 5. Noise



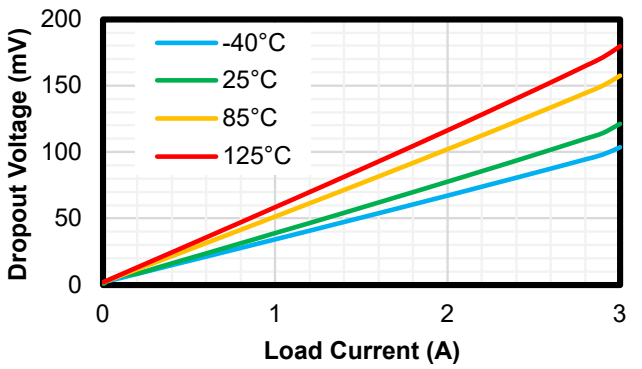
V_{IN} = 5.5 V, V_{OUT} = 5.2 V

Figure 6. Noise



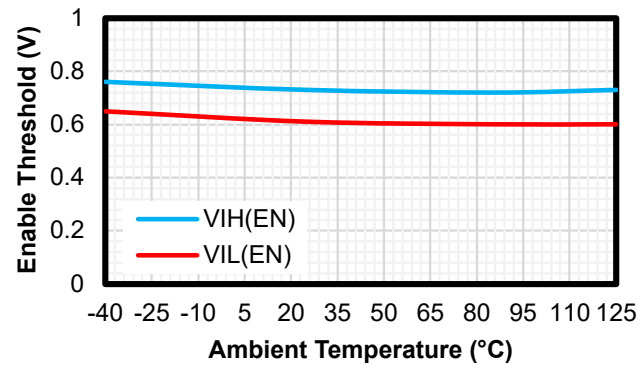
V_{IN} = 1.4 V

Figure 7. Dropout Voltage vs Output Current



V_{IN} = 5.5 V

Figure 8. Dropout Voltage vs Output Current



V_{IN} = 1.4 V

Figure 9. EN Threshold vs Temperature

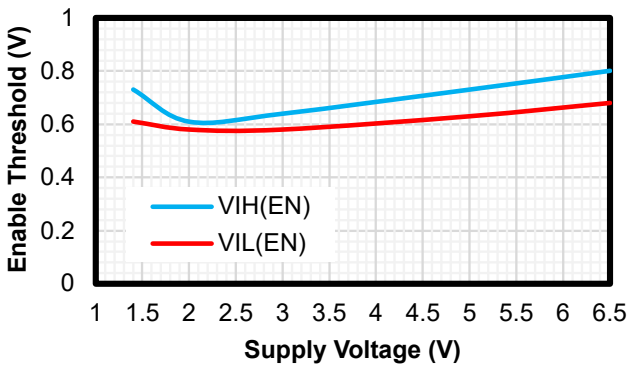
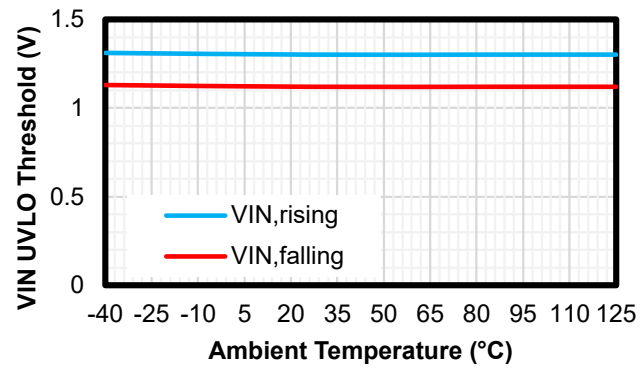
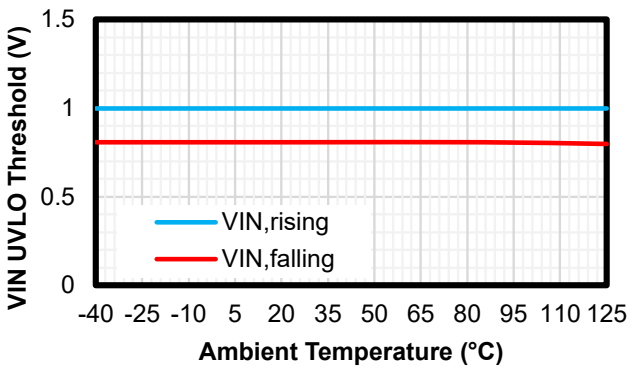


Figure 10. Enable Threshold vs Input Voltage



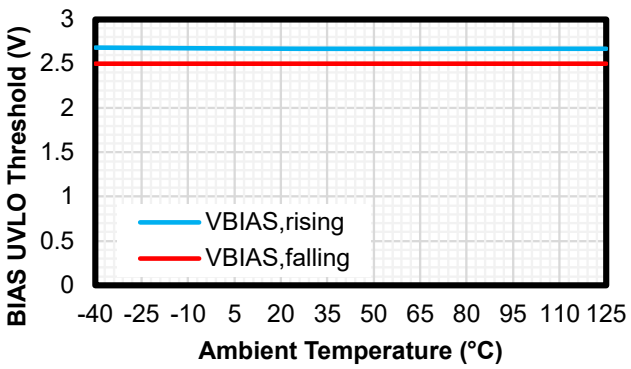
Without V_{BIAS}

Figure 11. UVLOIN1 vs. Temperature



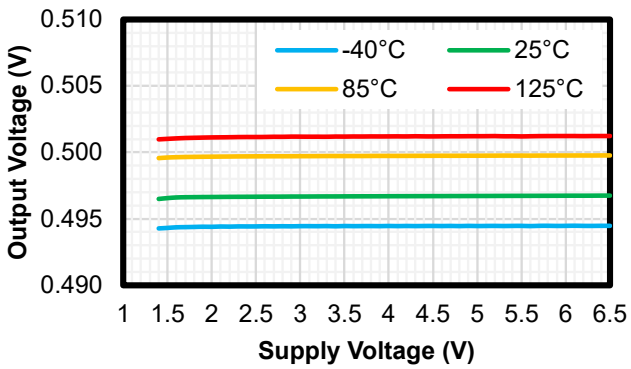
With V_{BIAS} = 3 V

Figure 12. UVLOIN2 vs. Temperature



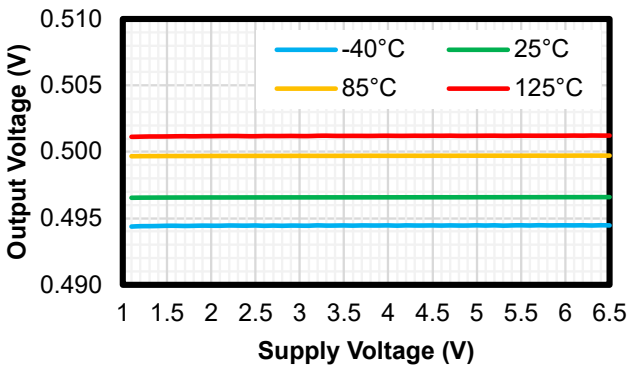
With V_{IN} = 1.1 V

Figure 13. BIAS UVLO vs. Temperature



Without V_{BIAS}

Figure 14. Line Regulation



With V_{BIAS} = 3 V

Figure 15. Line Regulation

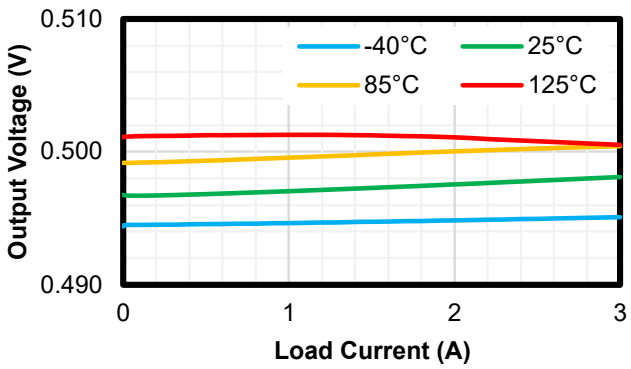
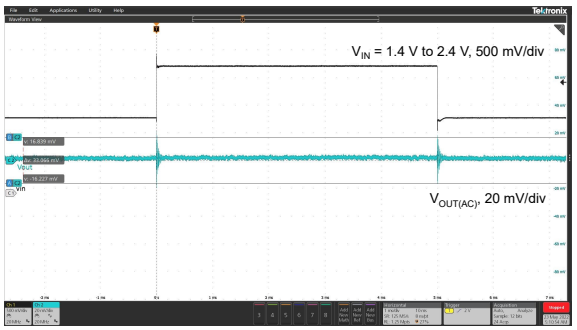
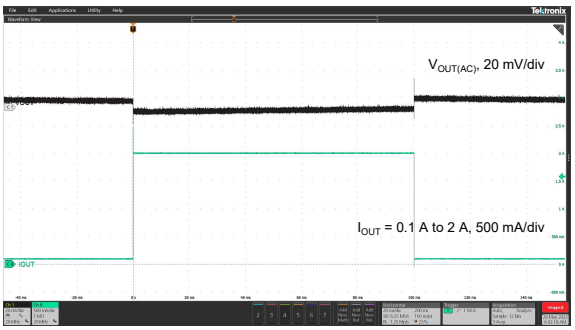


Figure 16. Load Regulation



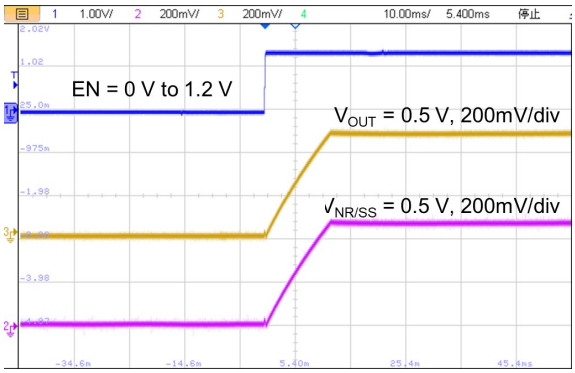
V_{IN} = 1.4 V to 2.4 V, V_{OUT} = 0.5 V, I_{OUT} = 1 A

Figure 17. Line Transient



V_{IN} = 1.4 V, V_{OUT} = 0.5 V, I_{OUT} = 0.1 A to 2 A

Figure 18. Load Transient



V_{IN} = 1.4 V, V_{OUT} = 0.5 V, $C_{NR/SS}$ = 100 nF, no load

Figure 19. Startup

Detailed Description

Overview

The TPL9305 is a 3-A high-current, 4-μV_{RMS} low-noise, high-PSRR, high-accuracy linear regulator with maximum 300-mV ultra-low dropout voltage at 3-A load condition. The TPL9305 supports both fixed output voltage ranging from 0.5 V to 3.65 V and adjustable output voltage ranging from 0.5 V to 5.2 V with an external resistor divider.

Ultra-low noise, high PSRR, and high output current capabilities make the TPL9305 an ideal power supply for noise-sensitive applications, such as high-speed communication facilities, test and measurement devices, and high-definition imaging equipment. Accurate output voltage tolerance, output voltage remote sensing, excellent transient response, and adjustable soft-start control ensure the TPL9305 an optimal power supply for the large-scale processors or digital loads, such as ASIC, FPGA, CPLD, and DSP.

Functional Block Diagram

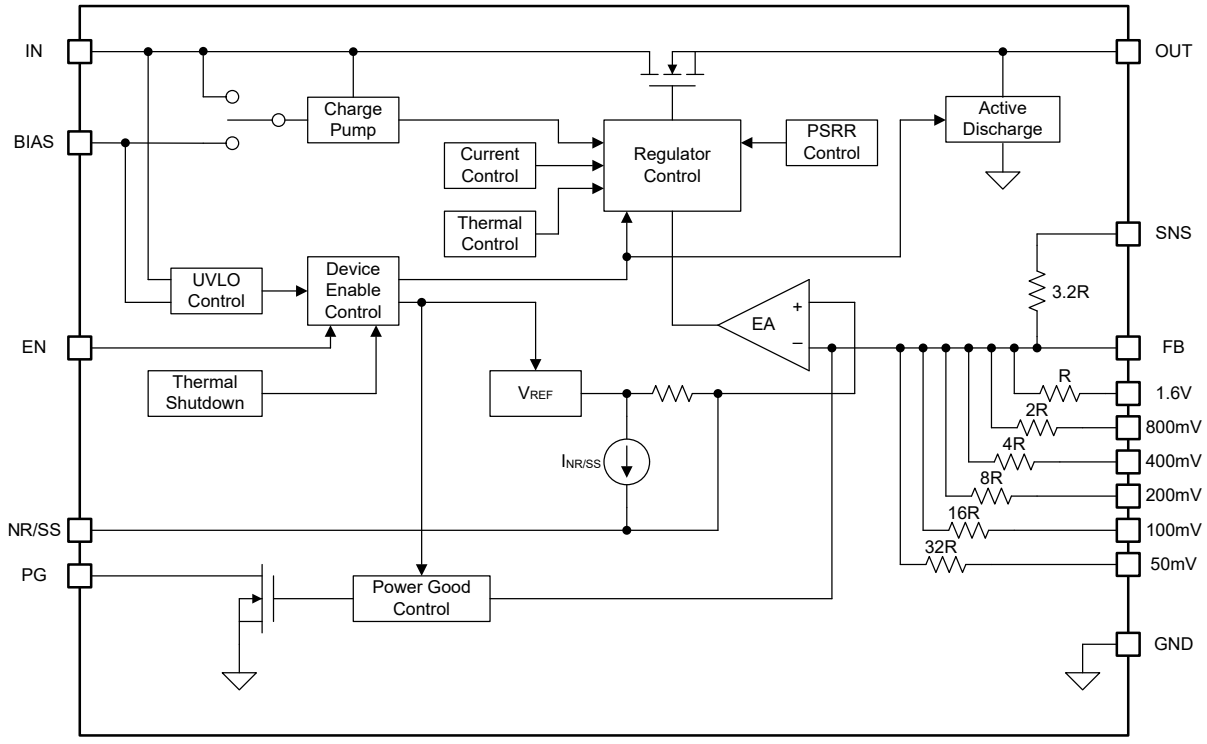


Figure 20. Functional Block Diagram

Feature Description

Enable (EN)

The TPL9305 provides a device with an enable pin (EN) to enable or disable the device. Connect the enable pin to the GPIO of an external digital logic control circuit to control the device. When the V_{EN} voltage falls below $V_{IL(EN)}$, the LDO device turns off, and when the V_{EN} ramps above $V_{IH(EN)}$, the LDO device turns on.

The TPL9305 also integrates an active discharge function. During normal operation, when the enable pin is pulled down below $V_{IL(EN)}$, the output voltage is discharged through the internal resistive path.

Under-Voltage Lockout (UVLO)

The TPL9305 uses an under-voltage lockout circuit to keep the output shut-off until the internal circuitry operates properly.

Voltage Regulation (OUT, FB)

The TPL9305 provides two options to set the output voltages: fixed output voltage configured by the programming pins, and adjustable output voltage configured by external resistors.

Fixed Output Voltage Setting

The TPL9305 integrates resistor divider internally to set the fixed output voltage. The fixed output voltage can be set from 0.5 V to 3.65 V by connecting the output voltage setting pins (pin 5 to pin 11) to ground or left them open. Use Equation 1 to calculate the output voltage.

$$V_{OUT} = V_{NR/SS} + V_{Pin_Setting} \quad (1)$$

Table 2 provides a full list of different output voltage targets and the corresponding pin settings.

Table 2. Fixed Output Voltage Setting

V_{OUT} (V)	50 mV	100 mV	200 mV	400 mV	800 mV	1.6 V	VOUT (V)	50 mV	100 mV	200 mV	400 mV	800 mV	1.6 V
Pin	5	6	7	9	10	11	Pin	5	6	7	9	10	11
0.5	Open	Open	Open	Open	Open	Open	2.1	Open	Open	Open	Open	Open	GND
0.55	GND	Open	Open	Open	Open	Open	2.15	GND	Open	Open	Open	Open	GND
0.6	Open	GND	Open	Open	Open	Open	2.2	Open	GND	Open	Open	Open	GND
0.65	GND	GND	Open	Open	Open	Open	2.25	GND	GND	Open	Open	Open	GND
0.7	Open	Open	GND	Open	Open	Open	2.3	Open	Open	GND	Open	Open	GND
0.75	GND	Open	GND	Open	Open	Open	2.35	GND	Open	GND	Open	Open	GND
0.8	Open	GND	GND	Open	Open	Open	2.4	Open	GND	GND	Open	Open	GND
0.85	GND	GND	GND	Open	Open	Open	2.45	GND	GND	GND	Open	Open	GND
0.9	Open	Open	Open	GND	Open	Open	2.5	Open	Open	Open	GND	Open	GND
0.95	GND	Open	Open	GND	Open	Open	2.55	GND	Open	Open	GND	Open	GND
1	Open	GND	Open	GND	Open	Open	2.6	Open	GND	Open	GND	Open	GND
1.05	GND	GND	Open	GND	Open	Open	2.65	GND	GND	Open	GND	Open	GND
1.1	Open	Open	GND	GND	Open	Open	2.7	Open	Open	GND	GND	Open	GND
1.15	GND	Open	GND	GND	Open	Open	2.75	GND	Open	GND	GND	Open	GND
1.2	Open	GND	GND	GND	Open	Open	2.8	Open	GND	GND	GND	Open	GND
1.25	GND	GND	GND	GND	Open	Open	2.85	GND	GND	GND	GND	Open	GND
1.3	Open	Open	Open	Open	GND	Open	2.9	Open	Open	Open	Open	GND	GND
1.35	GND	Open	Open	Open	GND	Open	2.95	GND	Open	Open	Open	GND	GND
1.4	Open	GND	Open	Open	GND	Open	3	Open	GND	Open	Open	GND	GND
1.45	GND	GND	Open	Open	GND	Open	3.05	GND	GND	Open	Open	GND	GND
1.5	Open	Open	GND	Open	GND	Open	3.1	Open	Open	GND	Open	GND	GND
1.55	GND	Open	GND	Open	GND	Open	3.15	GND	Open	GND	Open	GND	GND

1.6	Open	GND	GND	Open	GND	Open	3.2	Open	GND	GND	Open	GND	GND
1.65	GND	GND	GND	Open	GND	Open	3.25	GND	GND	GND	Open	GND	GND
1.7	Open	Open	Open	GND	GND	Open	3.3	Open	Open	Open	GND	GND	GND
1.75	GND	Open	Open	GND	GND	Open	3.35	GND	Open	Open	GND	GND	GND
1.8	Open	GND	Open	GND	GND	Open	3.4	Open	GND	Open	GND	GND	GND
1.85	GND	GND	Open	GND	GND	Open	3.45	GND	GND	Open	GND	GND	GND
1.9	Open	Open	GND	GND	GND	Open	3.5	Open	Open	GND	GND	GND	GND
1.95	GND	Open	GND	GND	GND	Open	3.55	GND	Open	GND	GND	GND	GND
2	Open	GND	GND	GND	GND	Open	3.6	Open	GND	GND	GND	GND	GND
2.05	GND	GND	GND	GND	GND	Open	3.65	GND	GND	GND	GND	GND	GND

Table 3. External Resistor Combinations

Target Output Voltage (V)	External Resistors Divider		Calculated Output Voltage (V)
	R1 (kΩ)	R2 (kΩ)	
0.50	0	Open	0.500
0.55	12.4	124	0.550
0.60	12.4	62	0.600
0.65	12.4	41.2	0.650
0.70	12.4	31	0.700
0.75	12.4	24.8	0.750
0.80	12.4	20.5	0.802
0.85	12.4	17.8	0.848
0.90	12.4	15.4	0.903
0.95	12	13.3	0.951
1.00	12.4	12.4	1.000
1.10	12	10	1.100
1.20	12.4	8.87	1.199
1.50	12.4	6.2	1.500
1.80	12.4	4.77	1.800
2.00	12.4	4.12	2.005
2.10	12	3.74	2.104
2.50	12.4	3.1	2.500
3.00	12	2.4	3.000
3.30	12.4	2.21	3.305
3.60	12.4	2	3.600
4.50	12.4	1.55	4.500
5.00	12.4	1.38	4.993
5.20	12.7	1.35	5.204

Adjustable Output Voltage Setting

The TPL9305 also provides an adjustable output voltage option. Using external resistors divider, the output voltage of TPL9305 is determined by the value of the resistor R1 and R2 in Figure 21. Use the Equation 2 to calculate the output voltage.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) \quad (2)$$

Where,

- the feedback voltage V_{FB} is 0.5 V
- R1 is the high-side feedback resistor
- R2 is the low-side feedback resistor

Table 3 provides a list of recommended resistor combinations to achieve the common output voltage values.

Output Soft-Start Control (NR/SS)

The TPL9305 integrates a programmable soft-start function to control the output voltage ramp-up slew rate and start-up time. By selecting the external capacitor at the NR/SS pin (CNR/SS), the output start-up time can be calculated with Equation 3.

$$t_{STRATUP} = 1.25 \times \frac{V_{NR/SS} \times C_{NR/SS}}{I_{NR/SS}} \quad (3)$$

Where,

- the typical value of $V_{NR/SS}$ is 0.5 V
- the typical value of $I_{NR/SS}$ is 7.8 uA
- $C_{NR/SS}$ is the external capacitor at the NR/SS pin

Charge Pump Noise

The TPL9305 integrates a charge pump to improve the PSRR and transient response under low input voltage conditions. The charge pump circuit generates a minimal amount of noise at the frequency of around 15 MHz. It is recommended to use 10-nF to 100-nF bypass capacitors close to the load a ferrite bead between the LDO output and the load input capacitors, forming a pi-filter to reduce the high-frequency noise level.

Power Good (PG)

The TPL9305 integrates an open-drain output power good indicator. Connect the PG pin to a pull-up voltage through a resistor from 10 kΩ to 100 kΩ if the power good function is used. Left the PG pin open if it is not used.

After regulator startup, the PG pin keeps low impendence until the output voltage reaches the power good threshold $V_{PG,TH}$. When the output voltage is higher than $V_{PG,TH}$, the PG pin turns to high output impedance, and PG is pulled up to a high voltage level to indicate the output voltage is ready

Output Active Discharge

The TPL9305 integrates an output discharge path from OUT to GND. When the device is disabled, the output will actively discharge the output voltage through an internal resistor of several hundred ohms.

Do not rely on this active discharge circuit for discharging large output capacitors when the input voltage falls below the output voltage. Reverse current flow through internal power MOSFET can permanently damage the device, and external current protection is essential at this condition.

Over-Current Protection and Short-to-Ground Protection

The TPL9305 series integrates an internal current limit that helps to protect the device during fault conditions. When the output is pulled down below the target output voltage, over-current protection starts to work and limit the output current to a typical value of 4.7 A.

Under over-current conditions, the internal junction temperature ramps up quickly. When the junction temperature is high enough, it will cause over-temperature protection.

Over-Temperature Protection

The recommended operating junction temperature range is from −40°C to 125°C. When the junction temperature is between 125°C and the thermal shutdown (TSD) threshold, the regulator can still work well, but will reduce the device lifetime for long-term use.

The over-temperature protection works when the junction temperature exceeds the thermal shutdown (TSD) threshold, which turns off the regulator immediately. When the device cools down and the junction temperature falls below the value, which equals to thermal shutdown threshold minus thermal shutdown hysteresis, the regulator turns on again.

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPL9305 is a 3-A high-current, low-noise, high-PSRR, high-accuracy linear regulator with a maximum 300-mV ultra-low dropout voltage at 3-A load condition. The following application schematic shows the typical usage of the TPL9305.

Typical Application

Adjustable Output Operation

Figure 21 shows a typical application schematic of the TPL9305 with adjustable output operation. Refer to section Adjustable Output Voltage Setting to set the output voltage.

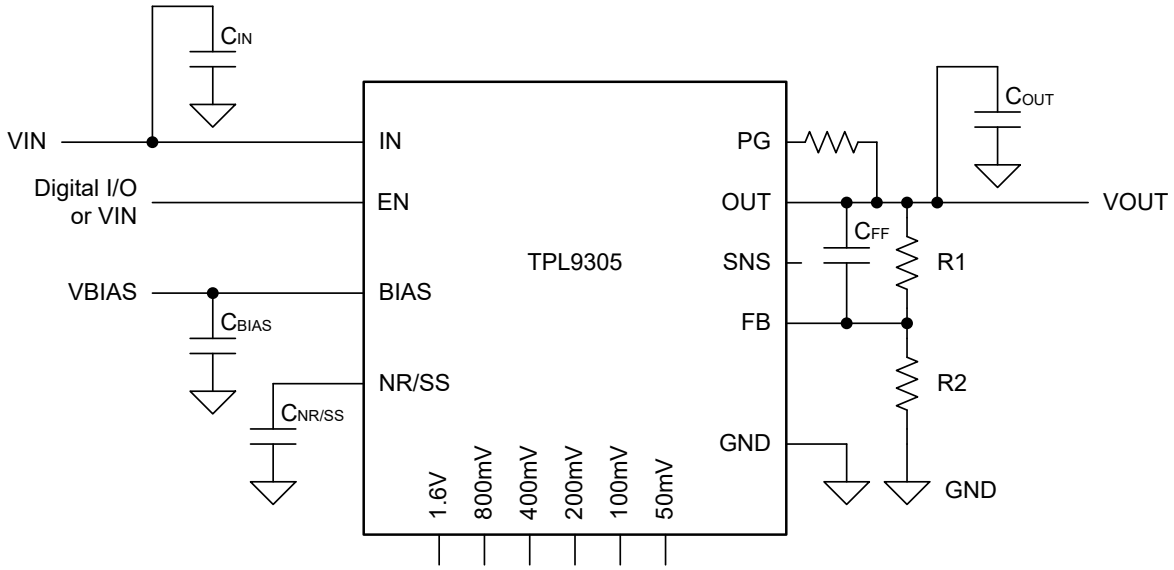


Figure 21. Adjustable Output Operation

Fixed Output Operation

Figure 22 shows a typical application schematic of the TPL9305 with fixed output operation. Refer to the section Fixed Output Voltage Setting to set the output voltage. In this example, output voltage is set to 1.5 V ($V_{NR/SS}$+ 0.8 V + 0.2 V).

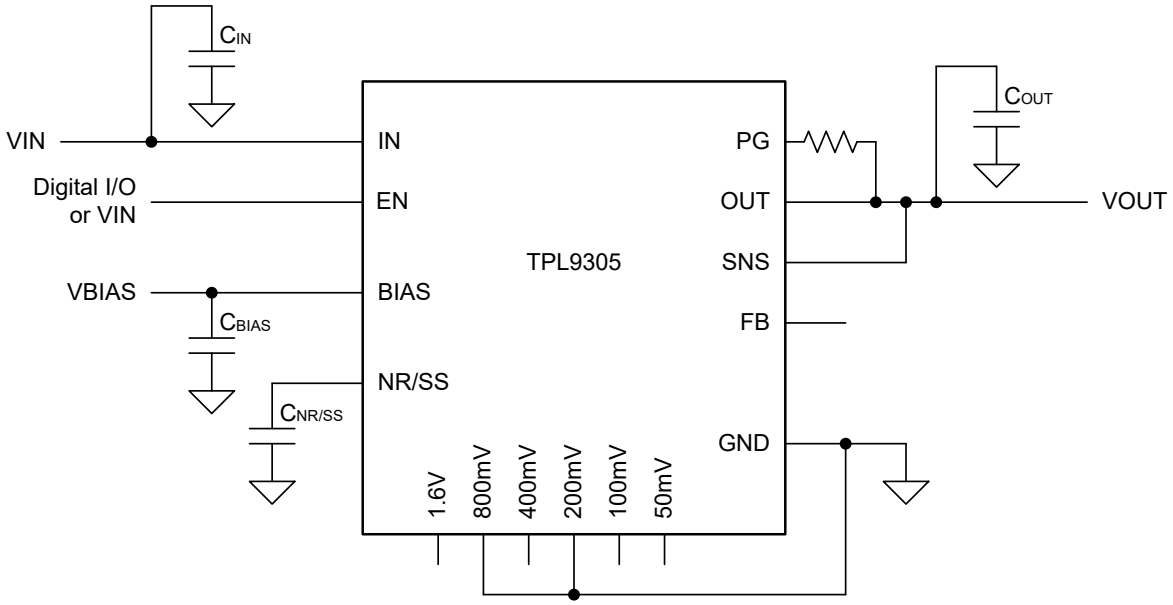


Figure 22. Fixed 1.5-V Output Voltage Operation

Input Capacitor and Output Capacitor

The TPL9305 is designed to be stable with low equivalent series resistance (ESR) ceramic capacitors at the input, output, and noise-reduction pin (NR/SS). It is recommended to use ceramic capacitors with X7R-, X5R-, and COG-rated dielectric materials to get good capacitive stability across temperature ranges.

3PEAK recommends adding a 10-μF or greater capacitor with a 0.1-μF bypass capacitor in parallel at the IN pin to keep the input voltage stable. The voltage rating of the capacitors must be greater than the maximum input voltage.

To ensure loop stability, the TPL9305 requires an output capacitor with a minimum effective capacitance value of 10 μF. 3PEAK recommends selecting an X7R-type 22-μF ceramic capacitor with low ESR over temperature.

Both input capacitors and output capacitors must be placed as close to the device pins as possible.

Power Dissipation

During normal operation, LDO junction temperature should not exceed 125°C. Using below equations to calculate the power dissipation and estimate the junction temperature.

The power dissipation can be calculated using Equation 4 .

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad (4)$$

The junction temperature can be estimated using Equation 5. θ_{JA} is the junction-to-ambient thermal resistance.

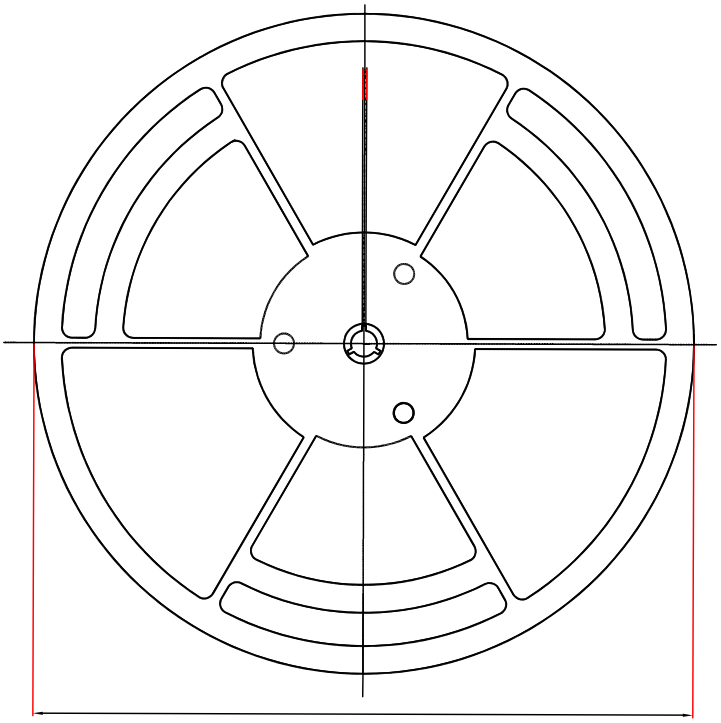
$$T_J = T_A + P_D \times \theta_{JA} \quad (5)$$

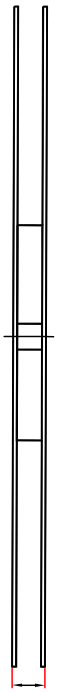
Layout

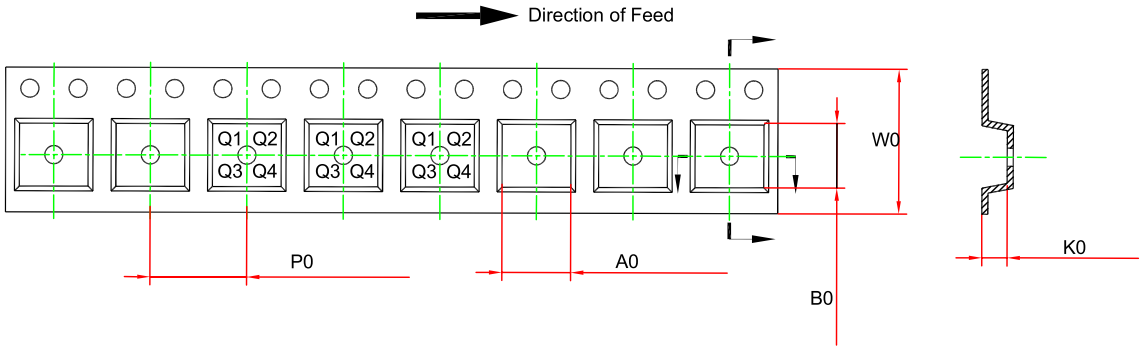
Layout Guideline

- Both input capacitors and output capacitors must be placed to the device pins as close as possible, and the vias between capacitors and device power pins must be avoided.
- It is recommended to bypass the input pin to ground with a 0.1-μF bypass capacitor. The loop area formed by the bypass capacitor connection, the IN pin and the GND pin of the system must be as small as possible.
- It is recommended to use wide and thick copper to minimize I×R drop and heat dissipation.
- Exposed pad must be connected to the PCB ground plane directly, the copper area must be as large as possible.

Tape and Reel Information





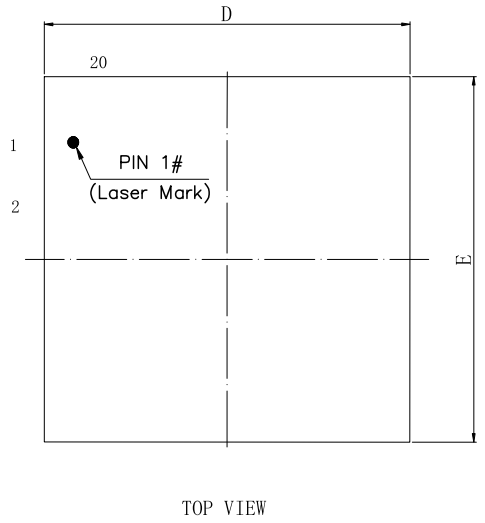


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPL9305AD-QF6R-S	QFN3.5X3.5-20	330	17.6	3.8	3.8	1.1	8	12	Q2

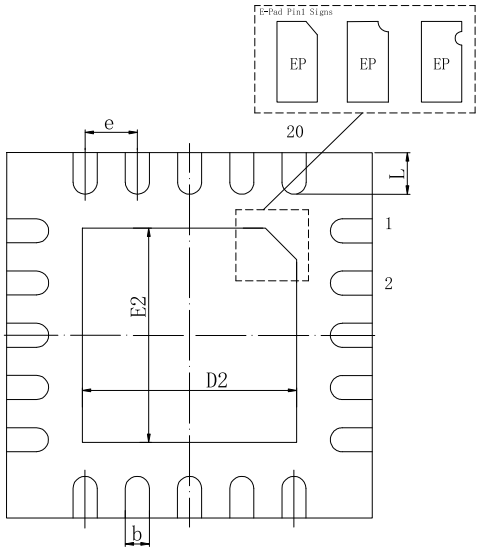
Package Outline Dimensions

QFN3.5X3.5-20

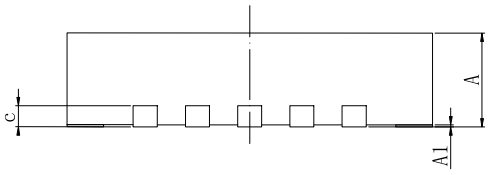
Package Outline Dimensions QF6(QFN3.5X3.5-20-A)



TOP VIEW



BOTTOM VIEW



SIDE VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
b	0.180	0.300	0.007	0.012
c	0.203 REF		0.008 REF	
D	3.400	3.600	0.134	0.142
E	3.400	3.600	0.134	0.142
e	0.500 BSC		0.020 BSC	
L	0.250	0.450	0.010	0.018
D2	2.050	2.250	0.081	0.089
E2	2.050	2.250	0.081	0.089

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPL9305AD-QF6R-S	–40°C to +125°C	QFN3.5X3.5-20	L935A	MSL3	Tape and Reel, 4,000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

IMPORTANT NOTICE AND DISCLAIMER

Copyright© 3PEAK 2012-2026. All rights reserved.

Trademarks. Any of the 思瑞浦 or 3PEAK trade names, trademarks, graphic marks, and domain names contained in this document /material are the property of 3PEAK. You may NOT reproduce, modify, publish, transmit or distribute any Trademark without the prior written consent of 3PEAK.

Performance Information. Performance tests or performance range contained in this document/material are either results of design simulation or actual tests conducted under designated testing environment. Any variation in testing environment or simulation environment, including but not limited to testing method, testing process or testing temperature, may affect actual performance of the product.

Disclaimer. 3PEAK provides technical and reliability data (including data sheets), design resources (including reference designs), application or other design recommendations, networking tools, security information and other resources "As Is". 3PEAK makes no warranty as to the absence of defects, and makes no warranties of any kind, express or implied, including without limitation, implied warranties as to merchantability, fitness for a particular purpose or non-infringement of any third-party's intellectual property rights. Unless otherwise specified in writing, products supplied by 3PEAK are not designed to be used in any life-threatening scenarios, including critical medical applications, automotive safety-critical systems, aviation, aerospace, or any situations where failure could result in bodily harm, loss of life, or significant property damage. 3PEAK disclaims all liability for any such unauthorized use.

This page intentionally left blank

ENTEGRECİ

Bu belge www.entegreci.com üzerinden sunulmaktadır.

Elektronik komponent tedarikinde Entegreci

Entegreci, Eskişehir merkezli, Türkiye geneline satış yapan bir elektronik komponent mağazasıdır. Entegreler (IC), mikrodenetleyiciler, transistörler, diyotlar, pasif elemanlar, konnektörler, modüller ve geliştirme kartları tek adetten seri üretim adetlerine kadar satılır. Ürün sayfalarında güncel stok durumunu, fiyatı ve datasheet bağlantısını bulabilirsiniz.

Parça koduyla arama

Üretici parça numarasını yazın; stok ve fiyatı hemen görün.

www.entegreci.com

Ürün kategorileri

Entegreden kapasitöre tüm elektronik komponent kategorileri.

Kategorilere göz atın

Üreticiler

Aradığınız üreticinin ürünlerini tek sayfada inceleyin.

Üreticileri görün

Toplu alım ve teklif

Listede olmayan ya da yüksek adetli parçalar için teklif isteyin.

Teklif isteyin

www.entegreci.com | **destek@entegreci.com** | **0850 305 90 34**

Entegreci is an online electronic components store based in Türkiye. Search by manufacturer part number to see stock, prices and datasheets for integrated circuits, microcontrollers, transistors, passive components and connectors, or request a quote for parts that are not listed.

Bu sayfa Entegreci tarafından eklenmiştir. Belgenin önceki sayfaları asıl yayıncısına aittir ve içeriği değiştirilmemiştir; en güncel sürüm için belgenin yayıncısına başvurun.