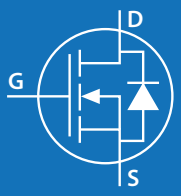
EPC2037 – Enhancement Mode Power Transistor

V_{DS}, 100 V
$R_{DS(on)}$, 550 mΩ
I_D, 1.7 A



EFFICIENT POWER CONVERSION

RoHS Halogen-Free

Revised August 21, 2024

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Application Notes:

- Easy-to-use and reliable gate, Gate Drive ON = 5 V typical, OFF = 0 V (negative voltage not needed)
- Top of FET is electrically connected to source

Questions: Ask a GaN Expert

Maximum Ratings			
PARAMETER		**VALUE**	**UNIT**
V_{DS}	Drain-to-Source Voltage (Continuous)	100	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	120	
I_D	Continuous (T_A = 25°C, $R_{\theta JA}$ = 44°C/W)	1.7	A
	Pulsed (25°C, T_{PULSE} = 300 µs)	2.4	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	–4	
	Recommended Gate-to-Source Voltage Operating Range*	4.5 – 5.5	
T_J	Operating Temperature	–40 to 150	°C
T_{STG}	Storage Temperature	–40 to 150	

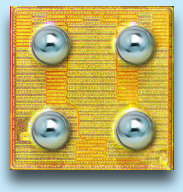
*Operating at less than 4 V_{GS} is not recommended.

Thermal Characteristics			
PARAMETER		**TYP**	**UNIT**
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	14	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	79	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	100	

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details

Static Characteristics (T_J = 25°C unless otherwise stated)						
PARAMETER		**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 125 µA	100			V
I_{DSS}	Drain-Source Leakage	V_{GS} = 0 V, V_{DS} = 80 V		10	100	µA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V		0.1	1	mA
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V		10	100	µA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 0.08 mA	0.8	1.5	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 0.1 A		400	550	mΩ
V_{SD}	Source-Drain Forward Voltage#	V_{GS} = 0 V, I_S = 0.5 A		2.5		V

Defined by design. Not subject to production test.
All measurements were done with substrate connected to source.



Die size: 0.9 x 0.9 mm

EPC2037 eGaN® FETs are supplied only in passivated die form with solder bumps.

Applications

- High speed DC-DC conversion
- Wireless power transfer
- Lidar/pulsed power applications
- Class-D audio

Benefits

- Ultra high efficiency
- Ultra low $R_{DS(on)}$
- Ultra low Q_G
- Ultra small footprint

Scan QR code or click link below for more information including reliability reports, device models, demo boards!

https://l.ead.me/EPC2037

Dynamic Characteristics# (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 50 V		14	17	pF
C_{RSS}	Reverse Transfer Capacitance			0.1		
C_{OSS}	Output Capacitance			6.5	10	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	V_{GS} = 0 V, V_{DS} = 0 to 50 V		9.5		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			12		
R_G	Gate Resistance			0.5		Ω
Q_G	Total Gate Charge	V_{GS} = 5 V, V_{DS} = 50 V, I_D = 0.1 A		115	145	pC
Q_{GS}	Gate-to-Source Charge	V_{DS} = 50 V, I_D = 0.1 A		32		
Q_{GD}	Gate-to-Drain Charge			25		
$Q_{G(TH)}$	Gate Charge at Threshold			24		
Q_{OSS}	Output Charge	V_{GS} = 0 V, V_{DS} = 50 V		600	900	
Q_{RR}	Source-Drain Recovery Charge			0		

Defined by design. Not subject to production test.
All measurements were done with substrate connected to source.
Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.
Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.

Figure 1: Typical Output Characteristics at 25°C

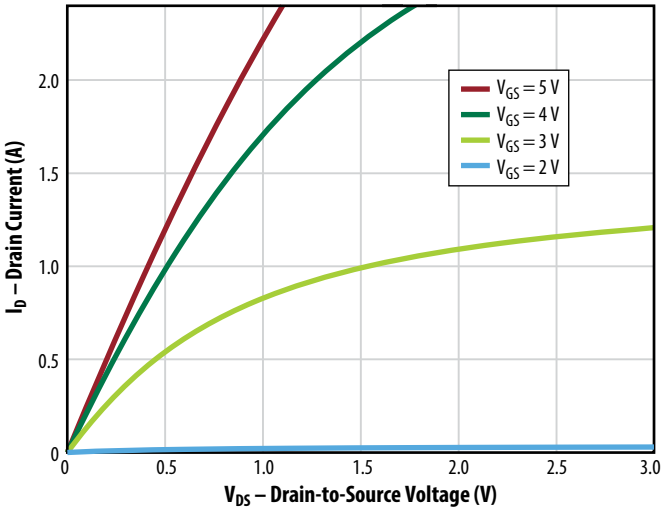


Figure 2: Typical Transfer Characteristics

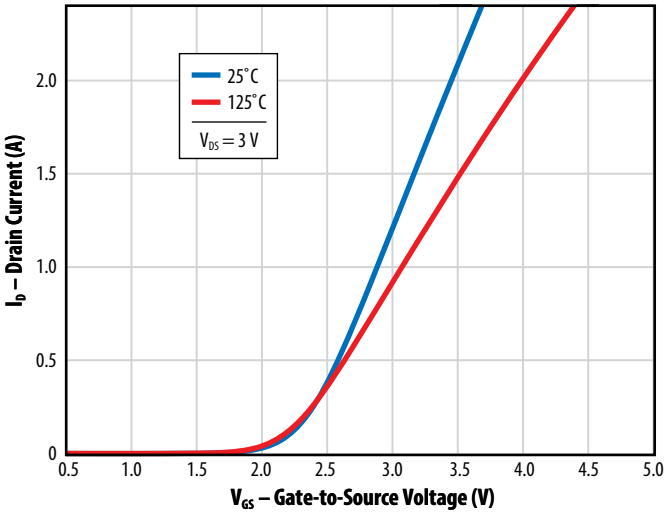


Figure 3: Typical $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

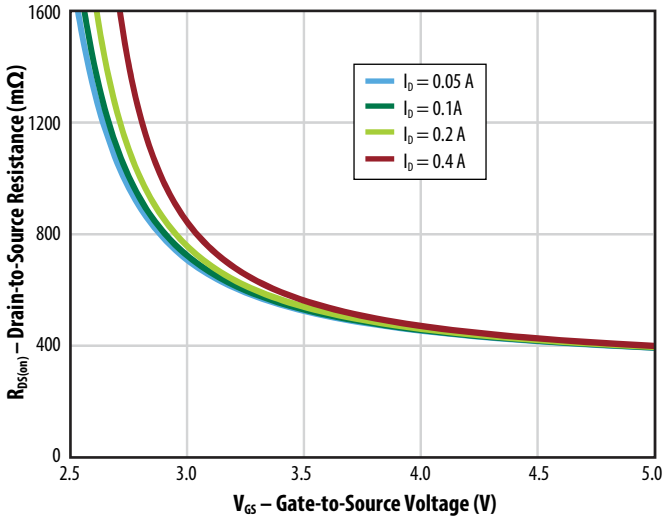


Figure 4: Typical $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

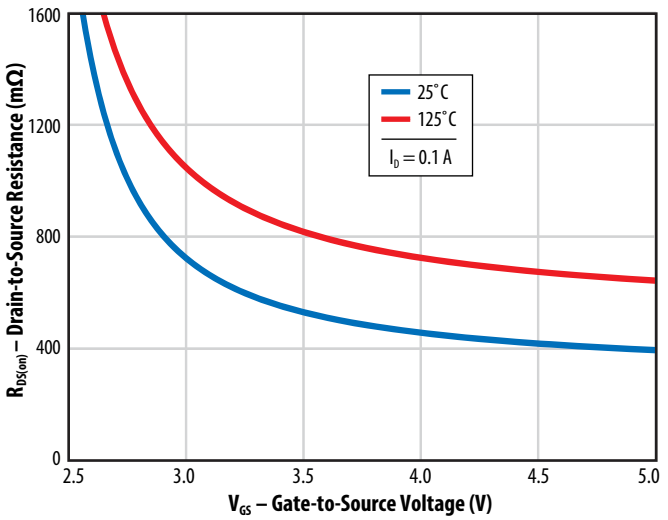


Figure 5a: Typical Capacitance (Linear Scale)

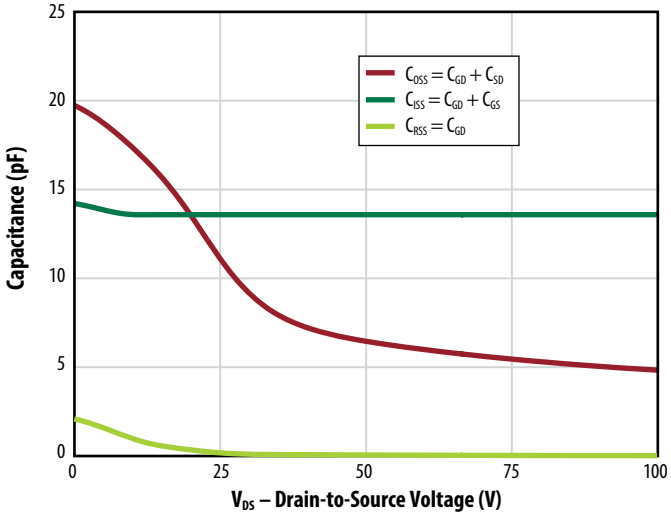


Figure 5b: Typical Capacitance (Log Scale)

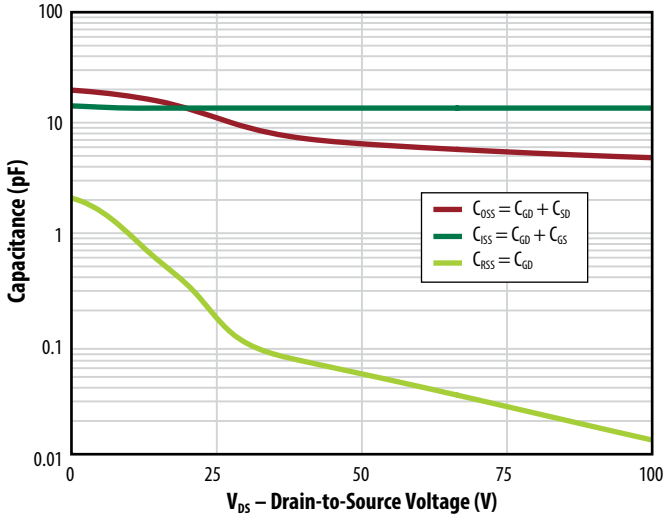


Figure 6: Typical Gate Charge

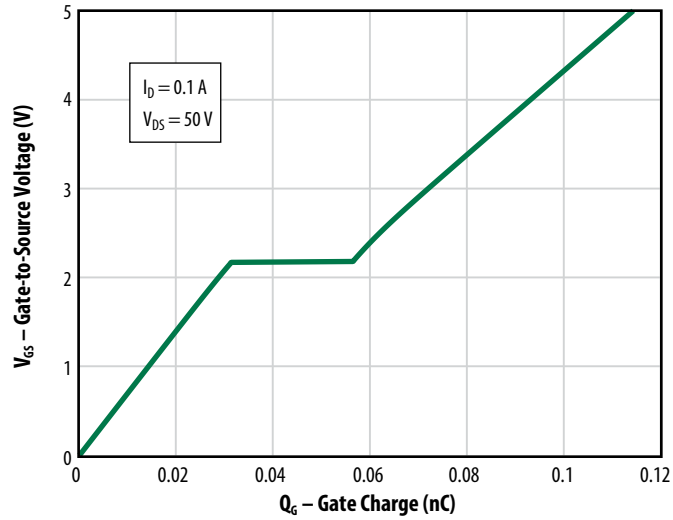
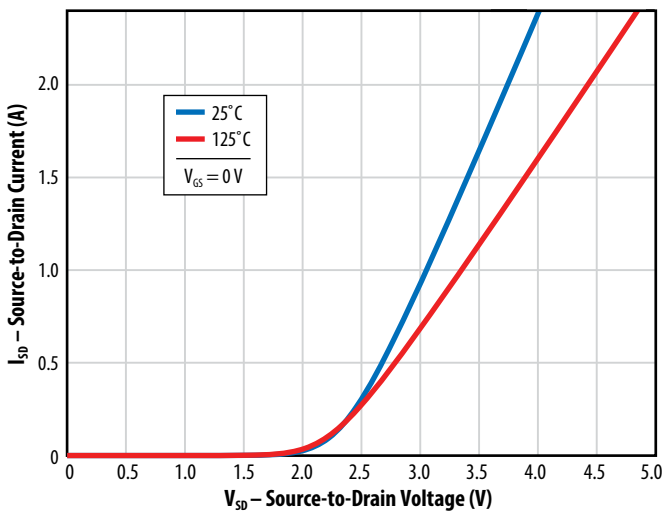


Figure 7: Typical Reverse Drain-Source Characteristics



Note: Negative gate drive voltage increases the reverse drain-source voltage. EPC recommends 0 V for OFF.

Figure 8: Typical Normalized On-State Resistance vs. Temp.

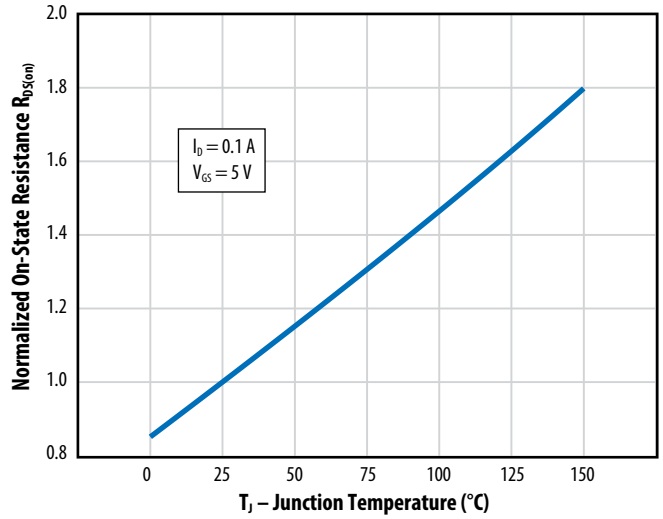


Figure 9: Typical Normalized Threshold Voltage vs. Temp.

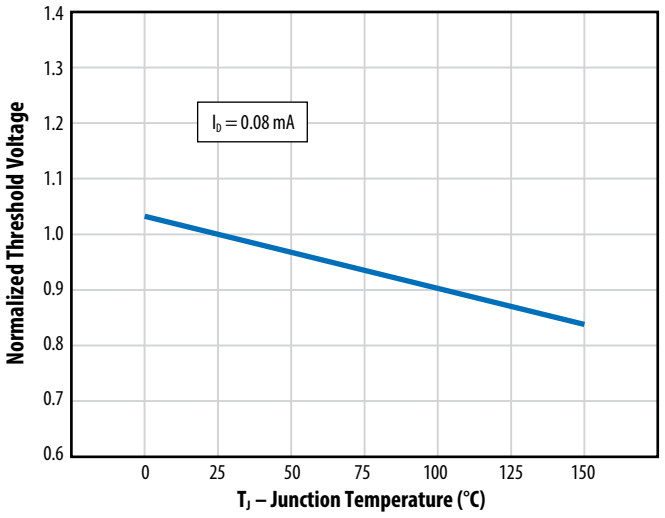
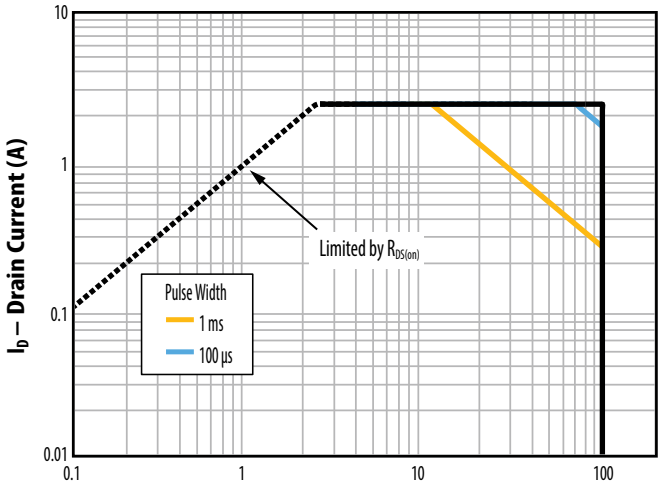
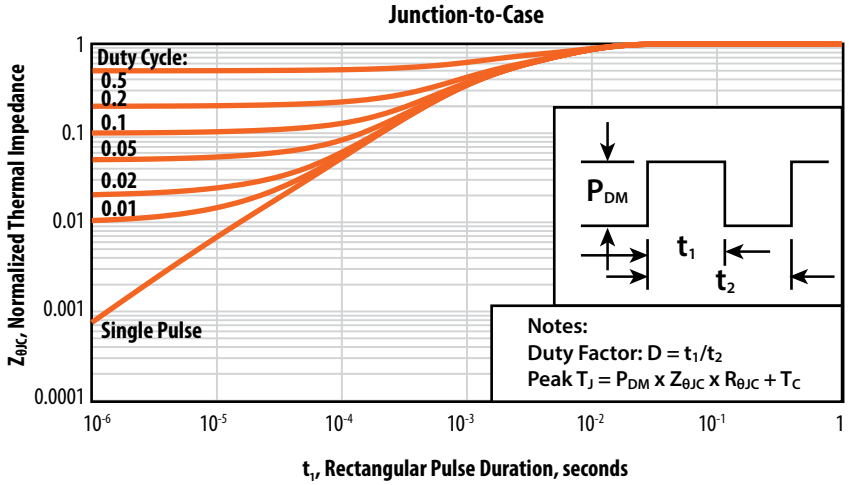


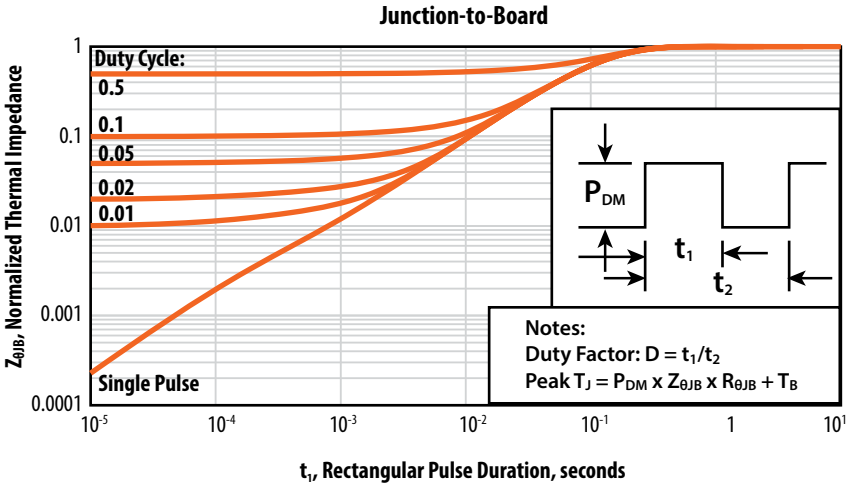
Figure 10: Safe Operating Area



T_J = Max Rated, T_C = +25°C, Single Pulse

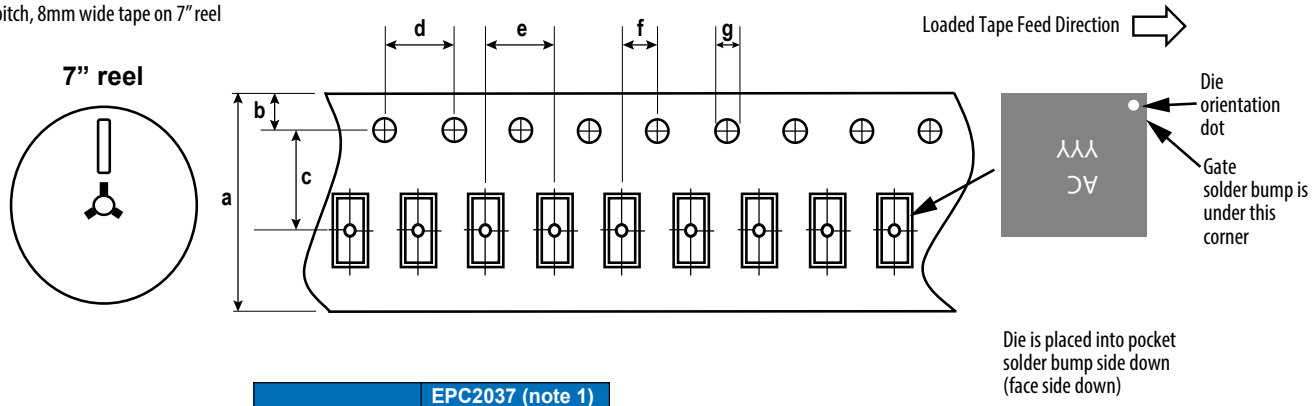
Figure 11: Typical Transient Thermal Response Curves





TAPE AND REEL CONFIGURATION

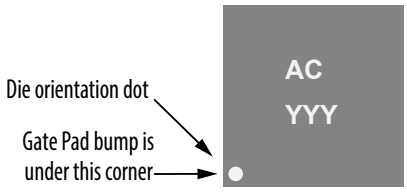
4mm pitch, 8mm wide tape on 7" reel



	EPC2037 (note 1)		
Dimension (mm)	**target**	**min**	**max**
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (see note)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (see note)	2.00	1.95	2.05
g	1.5	1.5	1.6

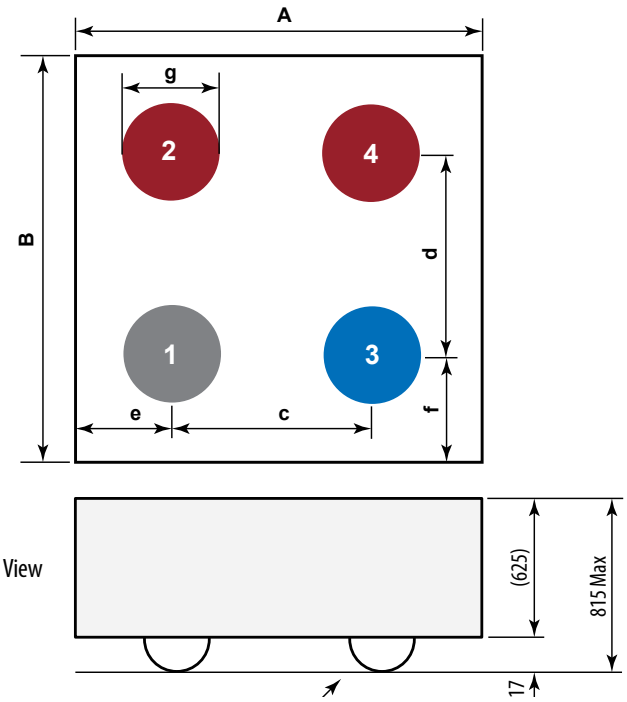
Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.
Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

DIE MARKINGS



Part Number	Laser Markings	
	Part # Marking Line 1	Lot_Date Code Marking line 2
EPC2037	AC	YYY

DIE OUTLINE
Solder Bump View



Side View

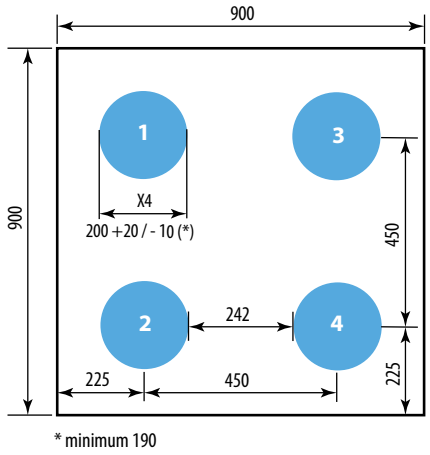
DIM	MIN	Nominal	MAX
A	870	900	930
B	870	900	930
c	450	450	450
d	450	450	450
e	210	225	240
f	210	225	240
g	187	208	229

Pads 1 is Gate;

Pad 3 is Drain;

Pads 2, 4 are Source

RECOMMENDED LAND PATTERN
(measurements in µm)



* minimum 190

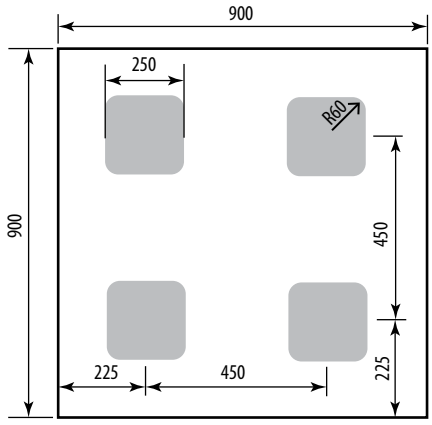
The land pattern is solder mask defined.

Pads 1 is Gate;

Pad 3 is Drain;

Pads 2, 4 are Source

RECOMMENDED STENCIL DRAWING
(measurements in µm)



Recommended stencil should be 4mil (100 µm) thick, must be laser cut, openings per drawing.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Additional assembly resources available at https://epc-co.com/epc/design-support

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