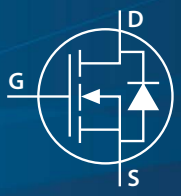
EPC2053 – Enhancement Mode Power Transistor

V_{DS}, 100 V

$R_{DS(on)}$, 3.8 mΩ

I_D, 48 A



EFFICIENT POWER CONVERSION

RoHS Halogen-Free

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Application Notes:

- Easy-to-use and reliable gate
- Gate Drive ON = 5-5.25 V typical (negative voltage not needed)
- Recommended dead time (half-bridge circuit) ≤ 30 ns for best efficiency
- Top of FET is electrically connected to source

Questions: Ask a GaN Expert

Maximum Ratings			
PARAMETER		**VALUE**	**UNIT**
V_{DS}	Drain-to-Source Voltage (Continuous)	100	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	120	
I_D	Continuous (T_A = 25°C)	48	A
	Pulsed (25°C, T_{PULSE} = 300 µs)	246	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
	Recommended Gate-to-Source Voltage Operating Range*	4.5 – 5.5	
T_J	Operating Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-40 to 150	

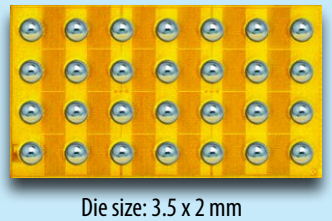
*Operating at less than 4 V_{GS} is not recommended. If V_{GS} ≤ 4 V is required, please contact EPC for technical support.

Thermal Characteristics			
PARAMETER		**TYP**	**UNIT**
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.7	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	4.7	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	53	

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board. See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

Static Characteristics (T_J = 25°C unless otherwise stated)						
PARAMETER		**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 0.4 mA	100			V
I_{DSS}	Drain-Source Leakage	V_{GS} = 0 V, V_{DS} = 80 V		0.07	0.3	mA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V		0.03	4	
	Gate-to-Source Forward Leakage#	V_{GS} = 5 V, T_J = 125°C		0.7	9	
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V		0.03	0.3	
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 9 mA	0.8	1.4	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 25 A		3.1	3.8	mΩ
V_{SD}	Source-Drain Forward Voltage#	V_{GS} = 0 V, I_S = 0.5 A		1.9		V

Defined by design. Not subject to production test.



Die size: 3.5 x 2 mm

EPC2053 eGaN® FETs are supplied in passivated die form with solder bumps.

Applications

- 48 V Servers
- Lidar/Pulsed Power
- Isolated Power Supplies
- Point of Load Converters
- Class D Audio
- LED Lighting
- Low Inductance Motor Drive

Benefits

- Higher Switching Frequency – Lower switching losses and lower drive power
- Higher Efficiency – Lower conduction and switching losses, zero reverse recovery losses
- Ultra Small Footprint - Higher power density

Scan QR code or click link below for more information including reliability reports, device models, demo boards!

https://l.ead.me/EPC2053

Dynamic Characteristics# (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	V_{DS} = 50 V , V_{GS} = 0 V		1453	1924	pF
C_{RSS}	Reverse Transfer Capacitance			10.4		
C_{OSS}	Output Capacitance			642	963	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	V_{DS} = 0 to 50 V, V_{GS} = 0 V		749		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			903		
R_G	Gate Resistance			0.6		Ω
Q_G	Total Gate Charge	V_{DS} = 50 V, V_{GS} = 5 V, I_D = 25 A		11.4	14.8	nC
Q_{GS}	Gate to Source Charge	V_{DS} = 50 V, I_D = 25 A		4.1		
Q_{GD}	Gate to Drain Charge			1.5		
$Q_{G(TH)}$	Gate Charge at Threshold			3.2		
Q_{OSS}	Output Charge	V_{GS} = 0 V, V_{DS} = 50 V		45	68	
Q_{RR}	Source-Drain Recovery Charge			0		

Defined by design. Not subject to production test.
All measurements were done with substrate connected to source.
Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50 V.
Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50 V.

Figure 1: Typical Output Characteristics at 25°C

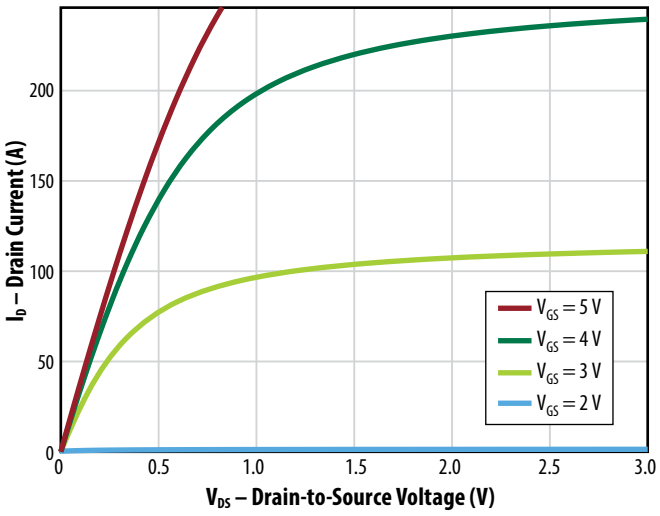


Figure 2: Typical Transfer Characteristics

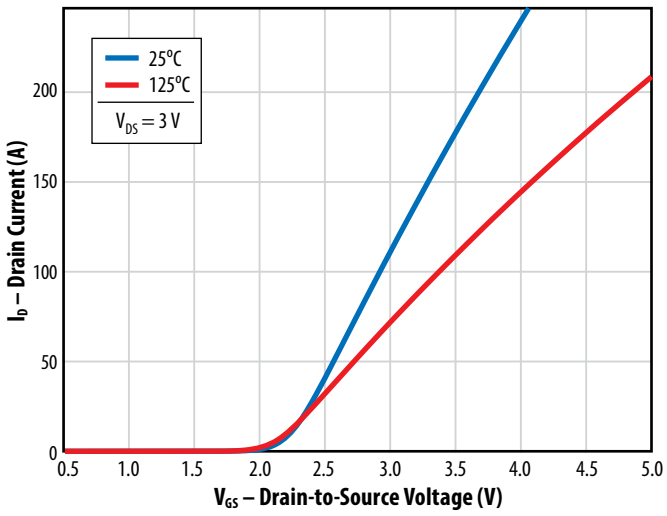


Figure 3: Typical $R_{DS(on)}$ vs. V_{GS} for Various Currents

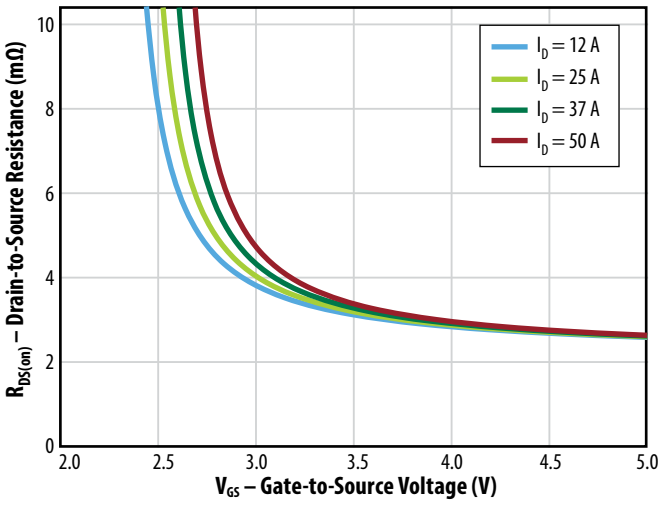


Figure 4: Typical $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

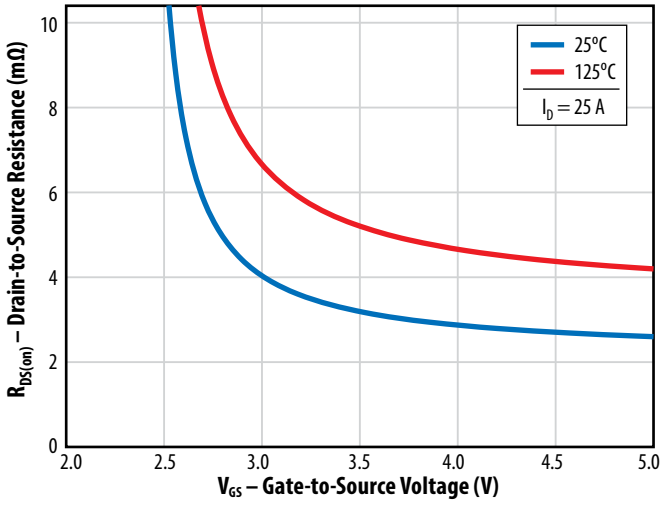


Figure 5a: Typical Capacitance (Linear Scale)

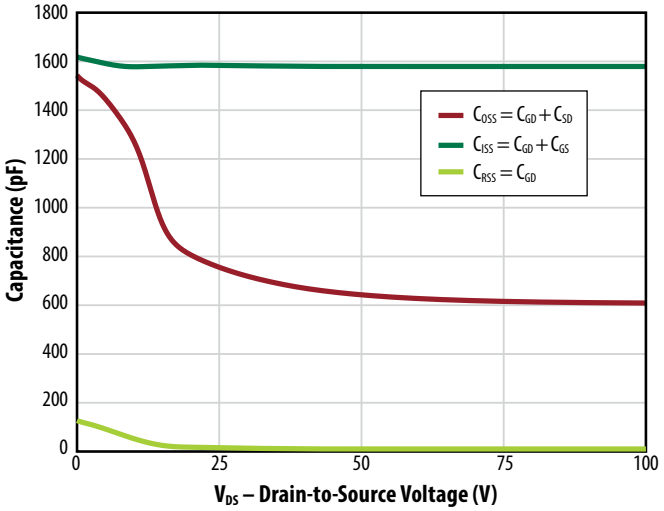


Figure 5b: Typical Capacitance (Log Scale)

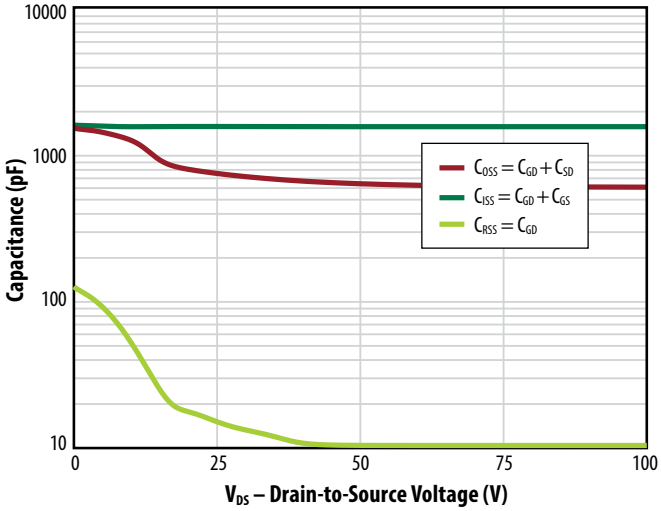


Figure 6: Typical Output Charge and C_{OSS} Stored Energy

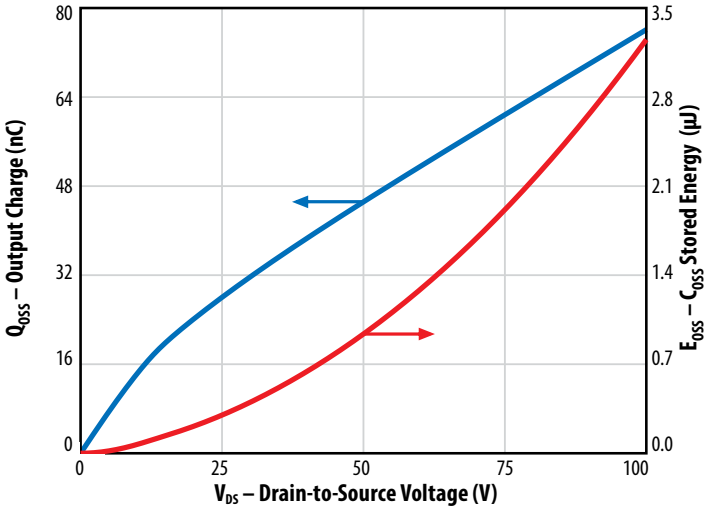


Figure 7: Typical Gate Charge

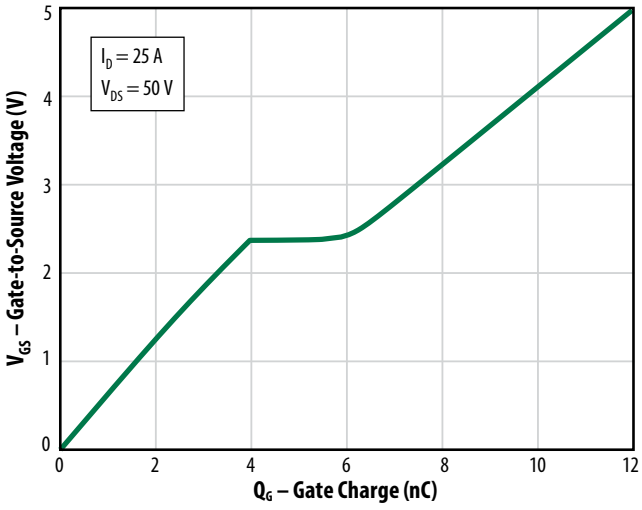


Figure 8: Typical Reverse Drain-Source Characteristics

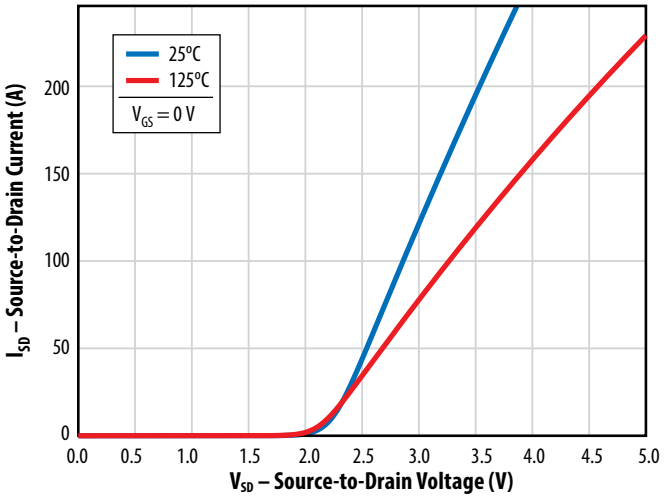
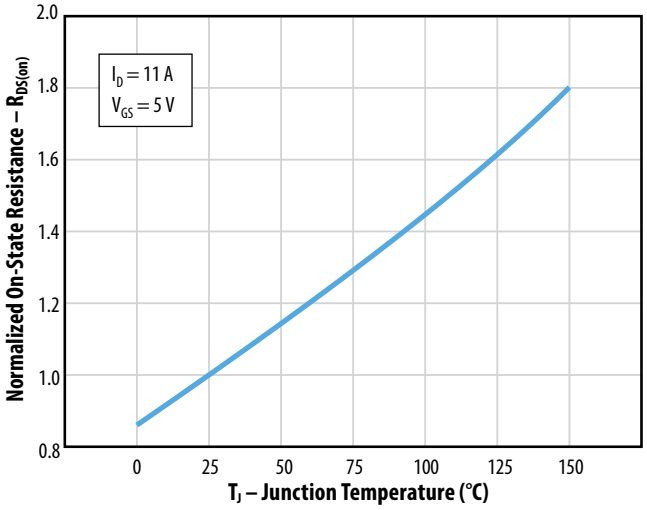


Figure 9: Typical Normalized On-State Resistance vs. Temperature



Note: Negative gate drive voltage increases the reverse drain-source voltage. EPC recommends 0 V for OFF.

Figure 10: Typical Normalized Threshold Voltage vs. Temperature

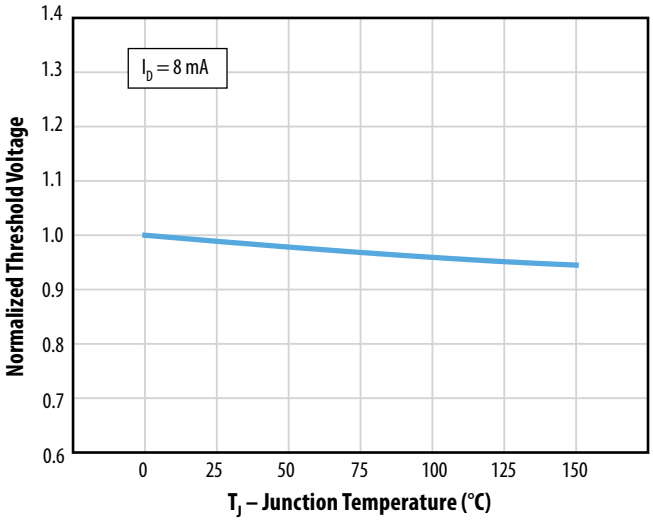
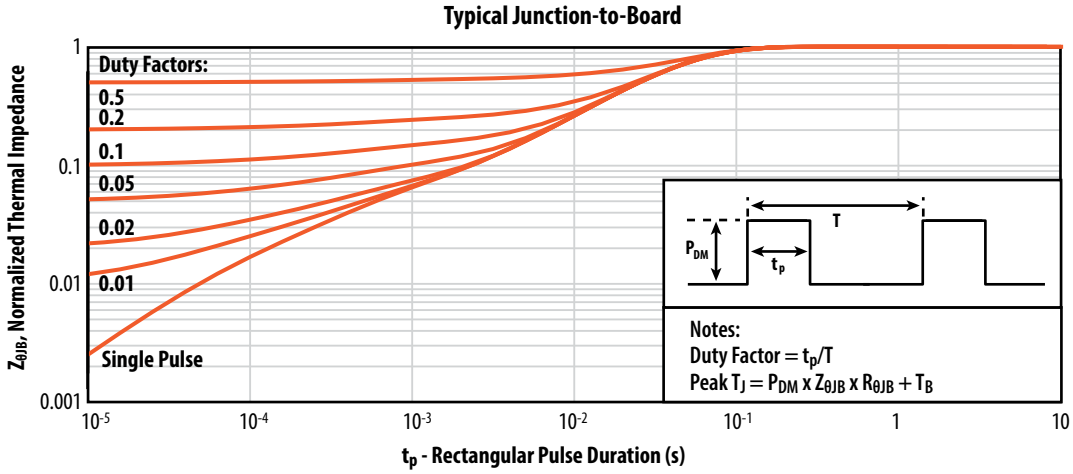


Figure 11: Typical Transient Thermal Response Curves



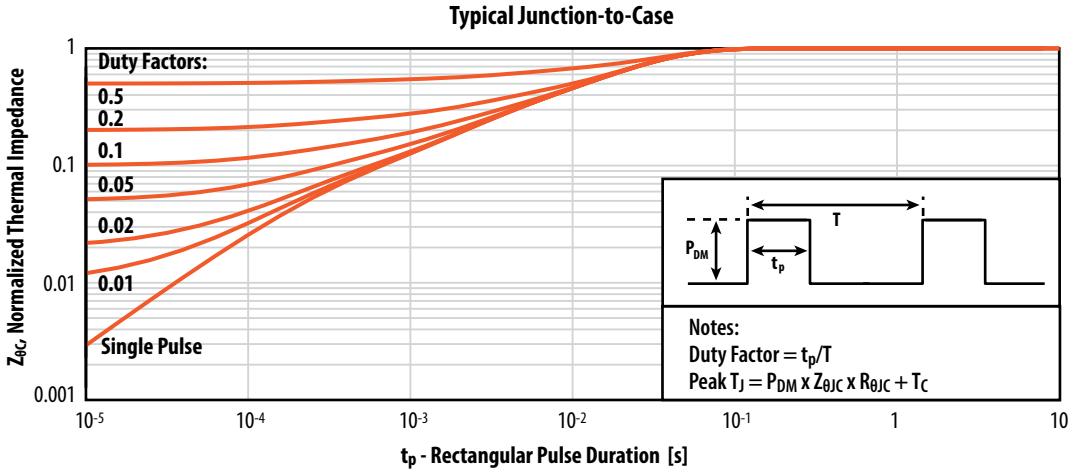
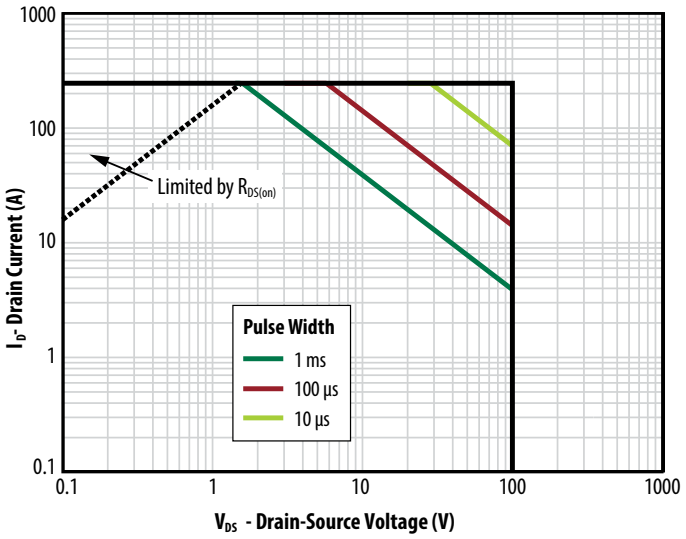


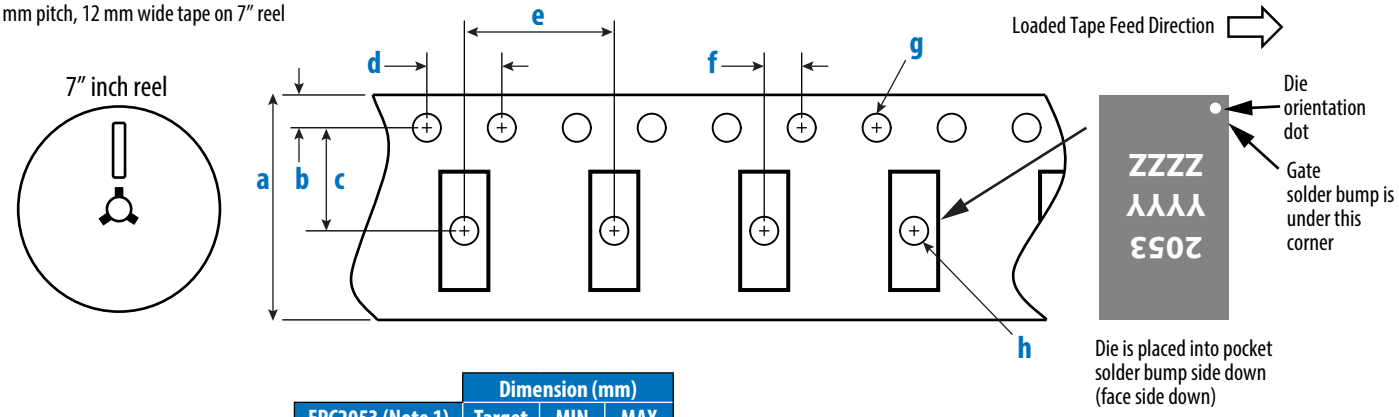
Figure 12: Safe Operating Area



T_J = Max Rated, T_C = +25°C, Single Pulse

TAPE AND REEL CONFIGURATION

8 mm pitch, 12 mm wide tape on 7" reel

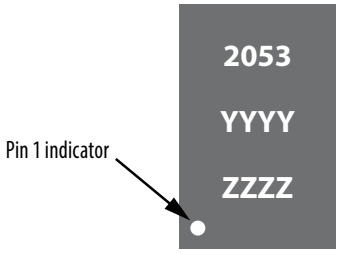


	Dimension (mm)		
EPC2053 (Note 1)	Target	MIN	MAX
a	12.00	11.90	12.30
b	1.75	1.65	1.85
c (Note 2)	5.50	5.45	5.55
d	4.00	3.90	4.10
e	8.00	7.90	8.10
f (Note 2)	2.00	1.95	2.05
g	1.50	1.50	1.60
h	1.50	1.50	1.75

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

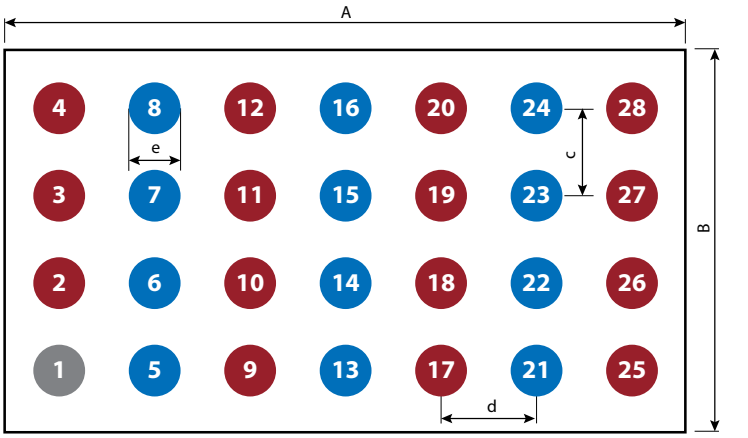
DIE MARKINGS



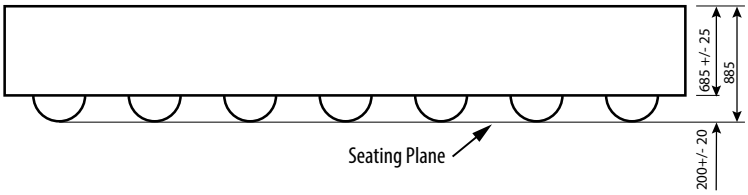
Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2053	2053	YYYY	ZZZZ

DIE OUTLINE

Solder Bump View



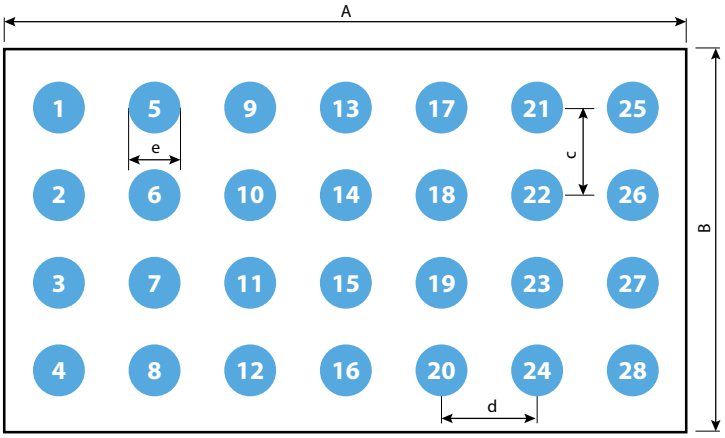
Side View



DIM	MICROMETERS		
	MIN	Nominal	MAX
A	3470	3500	3530
B	1920	1950	1980
c		450	
d		500	
e	238	264	290

Pad 1 is Gate;
Pads 2, 3, 4, 9, 10, 11, 12, 17, 18, 19, 20, 25, 26, 27, 28 are Source;
Pads 5, 6, 7, 8, 13, 14, 15, 16, 21, 22, 23, 24 are Drain.

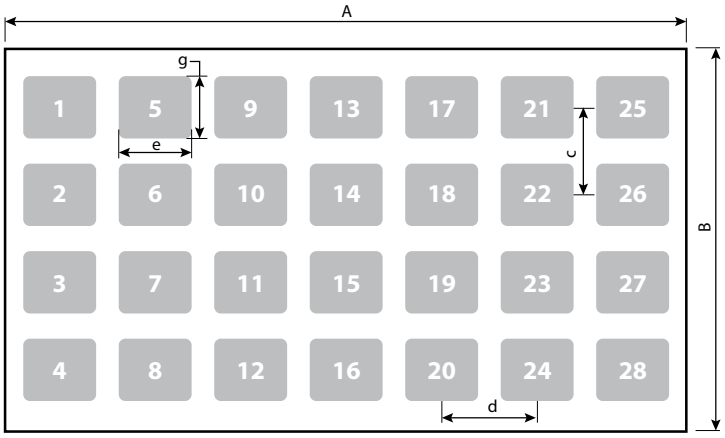
RECOMMENDED LAND PATTERN *(units in µm)*



DIM	MICROMETERS
A	3500
B	1950
c	450
d	500
e	230

Pad 1 is Gate;
Pads 2, 3, 4, 9, 10, 11, 12, 17, 18, 19, 20, 25, 26, 27, 28 are Source;
Pads 5, 6, 7, 8, 13, 14, 15, 16, 21, 22, 23, 24 are Drain.

RECOMMENDED STENCIL DRAWING *(measurements in µm)*



DIM	MICROMETERS
A	3500
B	1950
c	450
d	500
f	300
g	250

Recommended stencil should be 4 mil (100 µm) thick, must be laser cut, opening per drawing.
The corner has a radius of R60.
Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Additional assembly resources available at: https://epc-co.com/epc/design-support/assemblybasics

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