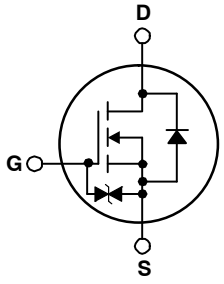
MOSFET – N-Channel, SUPERFET®

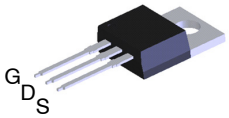
800 V, 8 A, 850 mΩ

FCP850N80Z

V_{DSS}	$R_{DS(on)}$ MAX	I_D MAX
800 V	850 mΩ @ 10 V	8 A



N-CHANNEL MOSFET



TO-220-3LD
CASE 340AT

Description

SuperFET II MOSFET is **onsemi**'s brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. In addition, internal gate−source ESD diode allows to withstand over 2 kV HBM surge stress. Consequently, SuperFET II MOSFET is very suitable for the switching power applications such as Audio, Laptop adapter, Lighting, ATX power and industrial power applications.

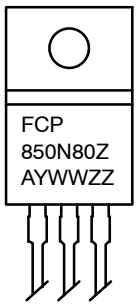
Features

- Typ. $R_{DS(on)}$ = 710 mΩ (Typ)
- Ultra Low Gate Charge (Typ. Q_g = 22 nC)
- Low E_{oss} (Typ. 2.3 μJ @ 400 V)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)}$ = 106 pF)
- 100% Avalanche Tested
- This Device is Pb-Free, Halide Free and RoHS Compliant
- ESD Improved Capability

Applications

- AC-DC Power Supply
- LED Lighting

MARKING DIAGRAM



FCP850N80Z	= Specific Device Code
A	= Assembly Location
YWW	= Date Code (Year & Week)
ZZ	= Assembly Lot

ORDERING INFORMATION

Device	Package	Shipping
FCP850N80Z	TO-220 (Pb-Free)	800 / Tube

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MOSFET MAXIMUM RATINGS (T_C = 25 °C unless otherwise noted)

Symbol	Parameter		Value	Unit
V_{DSS}	Drain to Source Voltage		800	V
V_{GSS}	Gate to Source Voltage	– DC	±20	V
		– AC (f > 1 Hz)	±30	A
I_D	Drain Current	– Continuous (T_C = 25 °C)	8.0	A
		– Continuous (T_C = 100 °C)	5.1	
I_{DM}	Drain Current	Pulsed (Note 1)	18	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		114	mJ
I_{AR}	Avalanche Current (Note 1)		1.2	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		1.36	mJ
dv/dt	MOSFET dv / dt		100	V/ns
	Peak Diode Recovery dv/dt (Note 3)		20	
P_D	Power Dissipation	(T_C = 25 °C)	136	W
		– Derate Above 25 °C	1.09	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		–55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8″ from Case for 5 Second		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. I_{AS} = 1.2 A, V_{DD} = 50 V, R_G = 25 Ω, starting T_J = 25 °C
3. $I_{SD} \le 8$ A, di/dt ≤ 200 A/μs, $V_{DD} \le BV_{DSS}$, starting T_J = 25 °C.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.92	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	°C/W

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ELECTRICAL CHARACTERISTICS (T_C = 25 °C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 1 mA, T_J = 25°C	800	–	–	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 1 mA, Referenced to 25°C	–	0.8	–	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 800 V, V_{GS} = 0 V	–	–	25	μA
		V_{DS} = 640 V, V_{GS} = 0 V, T_C = 125°C	–	–	250	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	–	–	±10	μA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 0.6 mA	2.5	–	4.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 3 A	–	710	850	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 20 V, I_D = 3 A	–	3.5	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 100 V, V_{GS} = 0 V, f = 1 MHz	–	990	1315	pF
C_{oss}	Output Capacitance		–	28	37	pF
C_{rss}	Reverse Transfer Capacitance		–	0.74	–	pF
C_{oss}	Output Capacitance	V_{DS} = 480 V, V_{GS} = 0 V, f = 1 MHz	–	15	–	pF
$C_{oss\ (eff)}$	Effective Output Capacitance	V_{DS} = 0 V to 480 V, V_{GS} = 0 V	–	106	–	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	V_{DS} = 640 V, I_D = 6 A, V_{GS} = 10 V (Note 4)	–	22	29	nC
Q_{gs}	Gate to Source Gate Charge		–	5	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	8.6	–	nC
ESR	Equivalent Series Resistance	f = 1 MHz	–	2.4	–	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 400 V, I_D = 6 A, V_{GS} = 10 V, R_g = 4.7 Ω (Note 4)	–	16	42	ns
t_r	Turn-On Rise Time		–	10	30	ns
$t_{d(off)}$	Turn-Off Delay Time		–	40	90	ns
t_f	Turn-Off Fall Time		–	4.5	19	ns
DRAIN-SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuous Drain to Source Diode Forward Current		–	–	8	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		–	–	18	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 6 A	–	–	1.2	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 6 A, dI_F/dt = 100 A/μs	–	318	–	ns
Q_{rr}	Reverse Recovery Charge		–	4.5	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially Independent of Operating Temperature Typical Characteristics

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TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

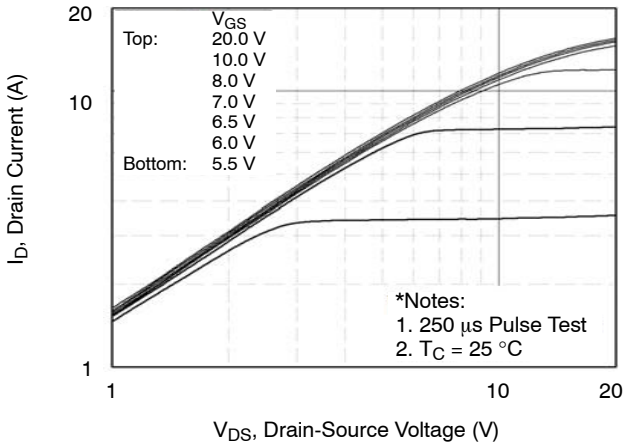


Figure 1. On-Region Characteristics

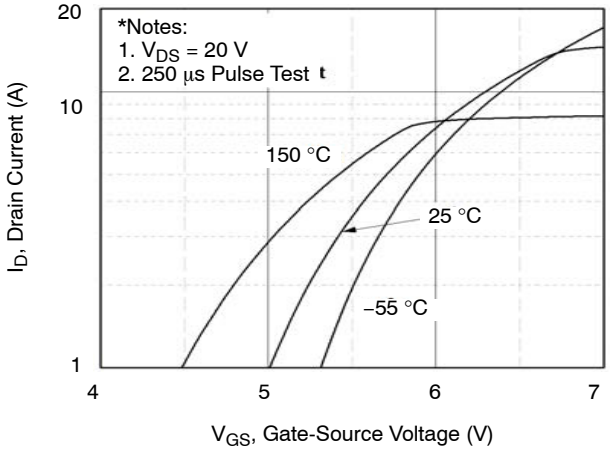


Figure 2. Transfer Characteristics

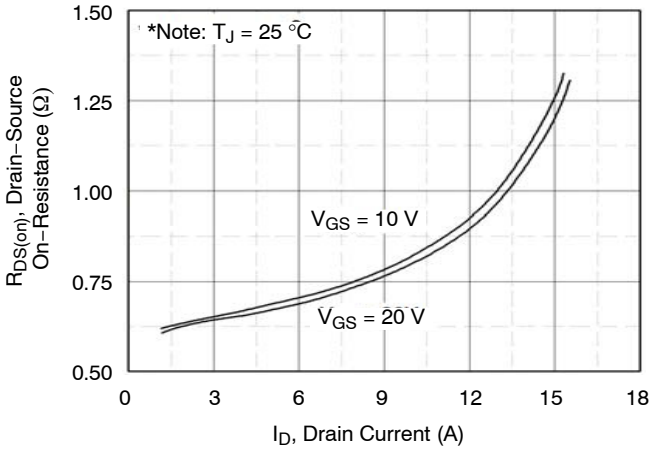


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

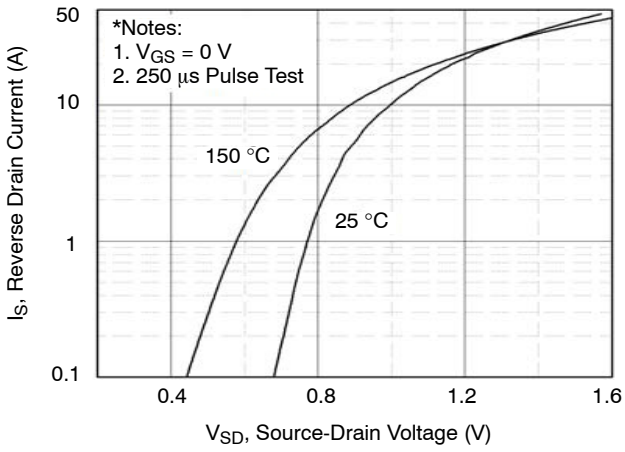


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

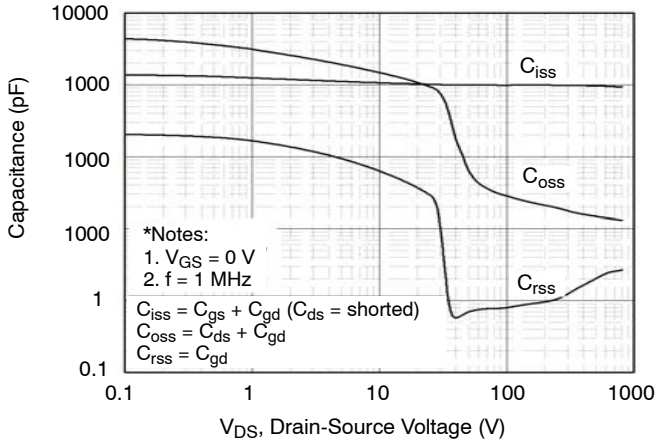


Figure 5. Capacitance Characteristics

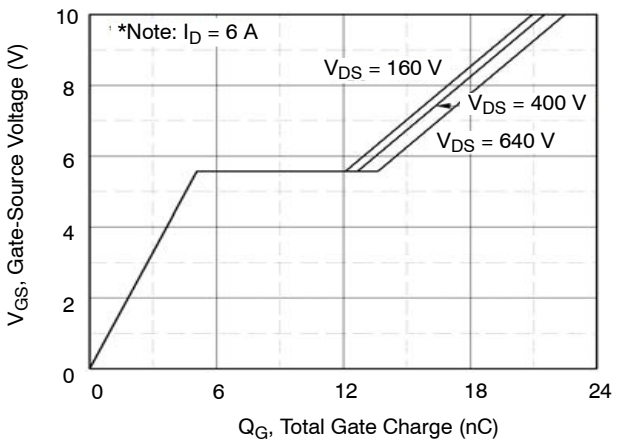


Figure 6. Gate Charge Characteristics

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TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

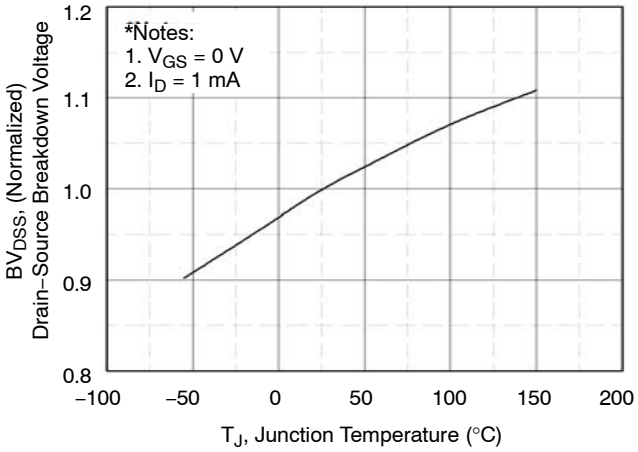


Figure 7. Breakdown Voltage Variation vs. Temperature

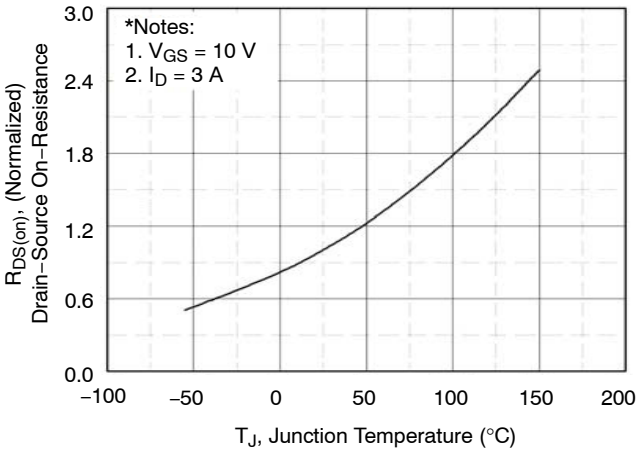


Figure 8. On-Resistance Variation vs. Temperature

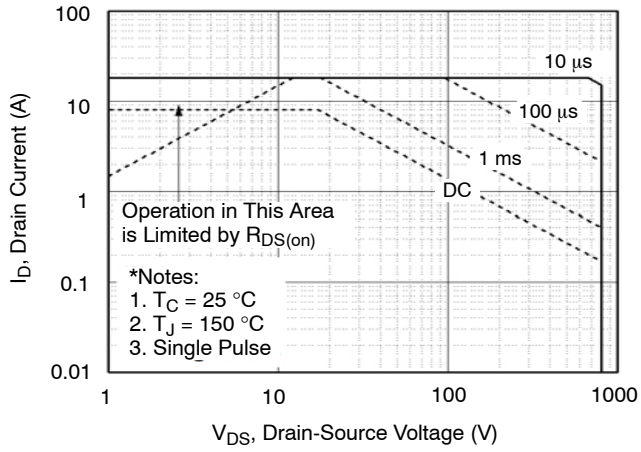


Figure 9. Maximum Safe Operating Area

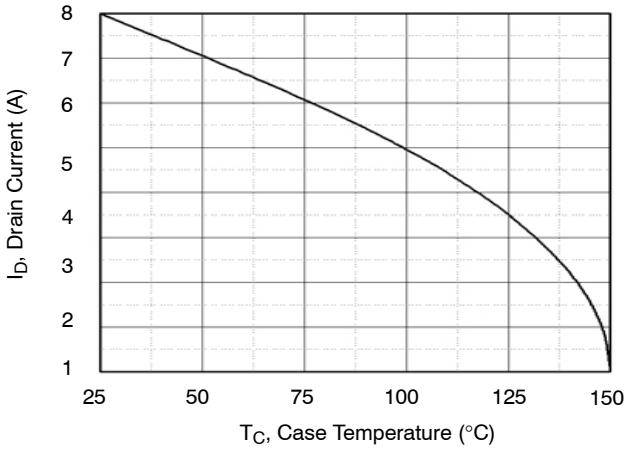


Figure 10. Maximum Drain Current vs. Case Temperature

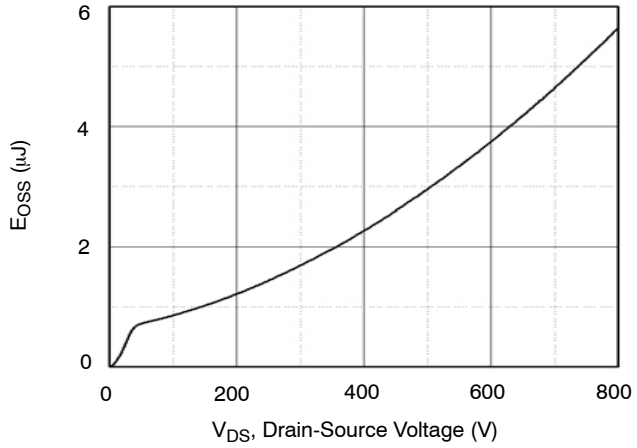


Figure 11. E_{OSS} vs. Drain to Source Voltage

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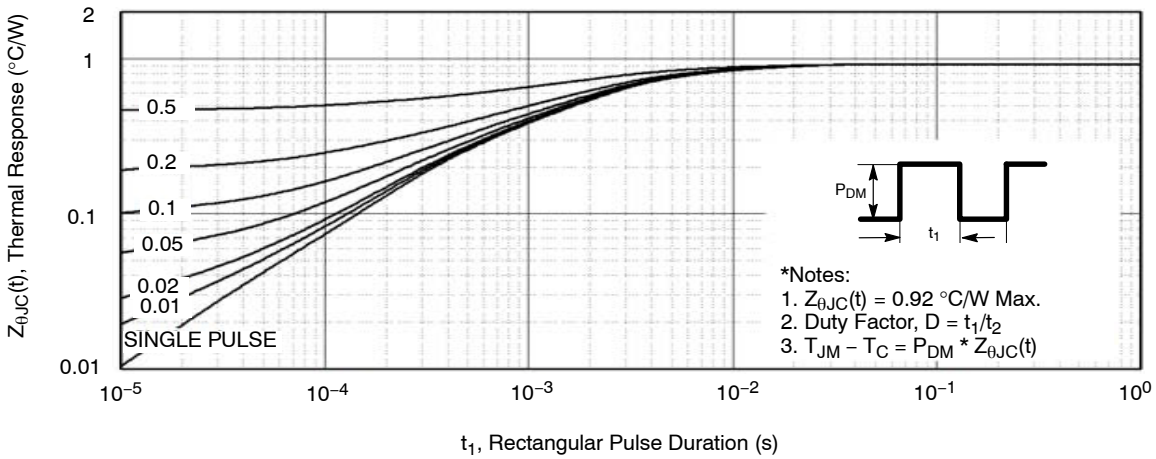


Figure 12. Transient Thermal Response Curve

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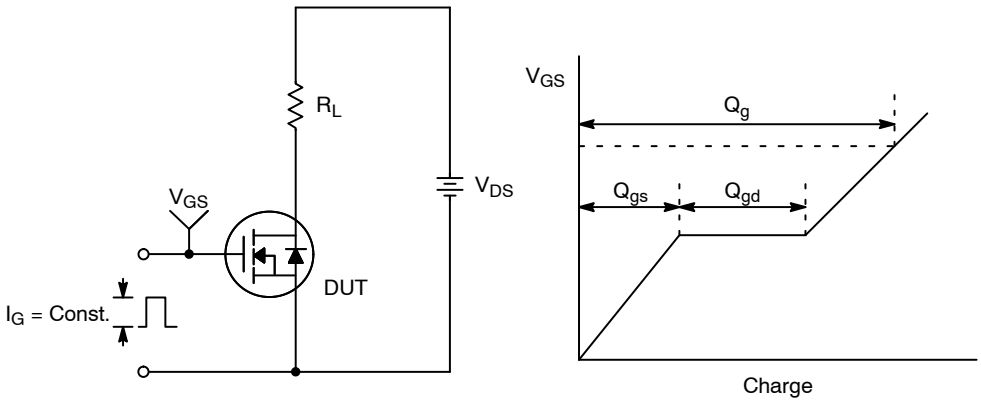


Figure 13. Gate Charge Test Circuit & Waveform

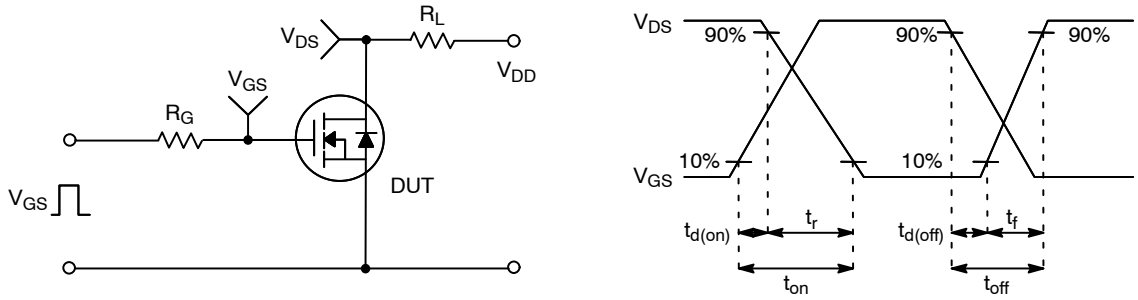


Figure 14. Resistive Switching Test Circuit & Waveforms

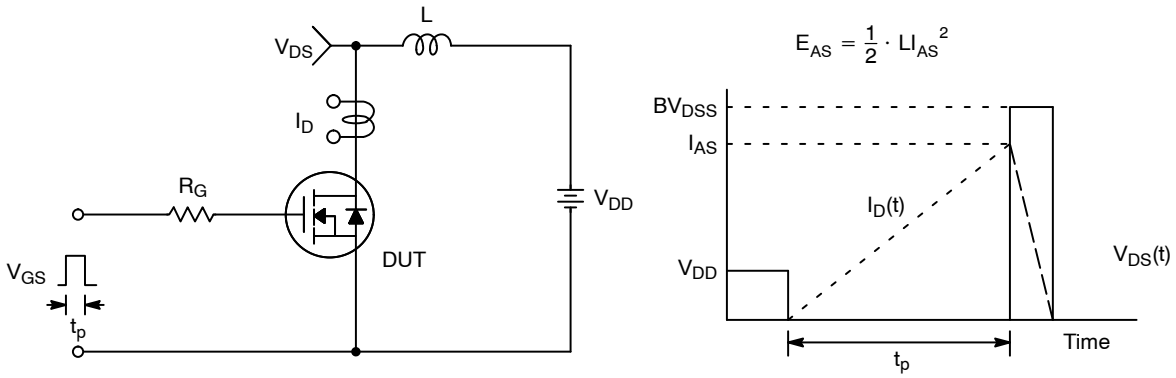


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

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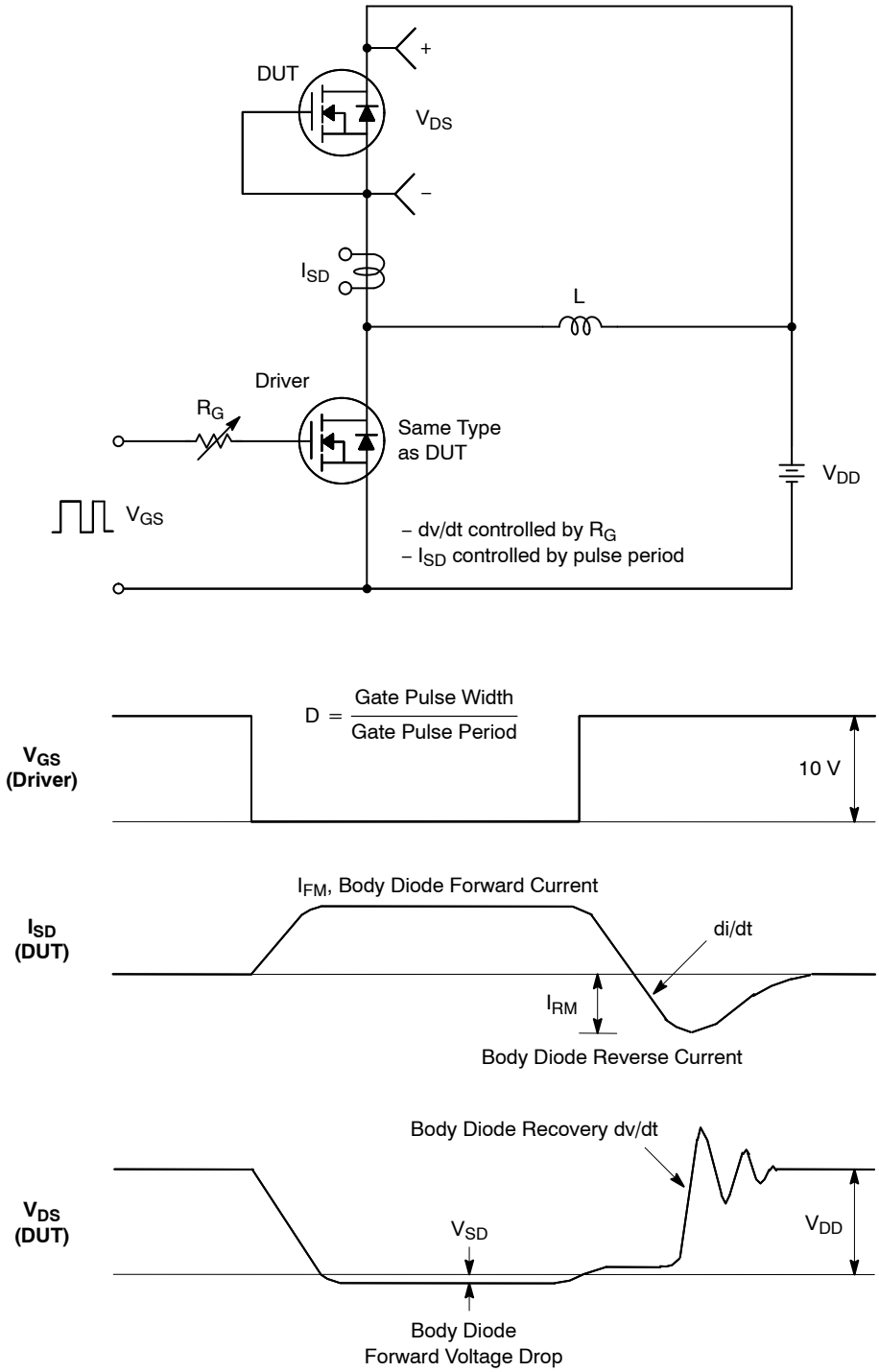


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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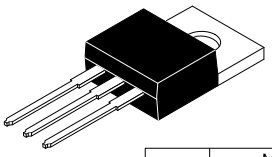
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REVISION HISTORY

Revision	Description of Changes	Date
2	Converted the Data Sheet to **onsemi** format.	12/10/2025

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

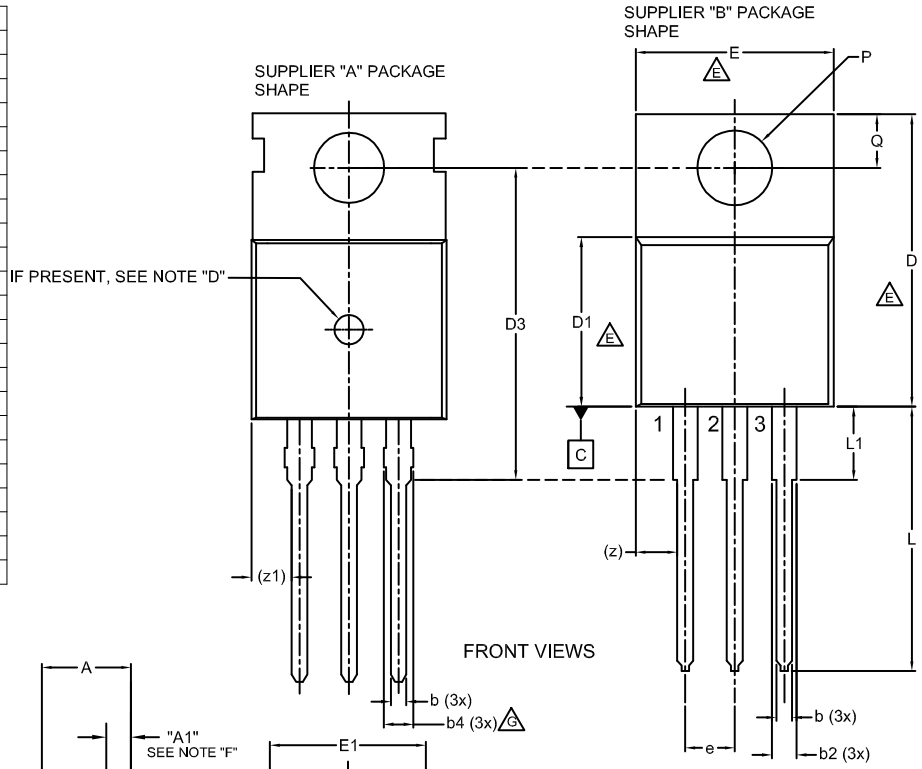
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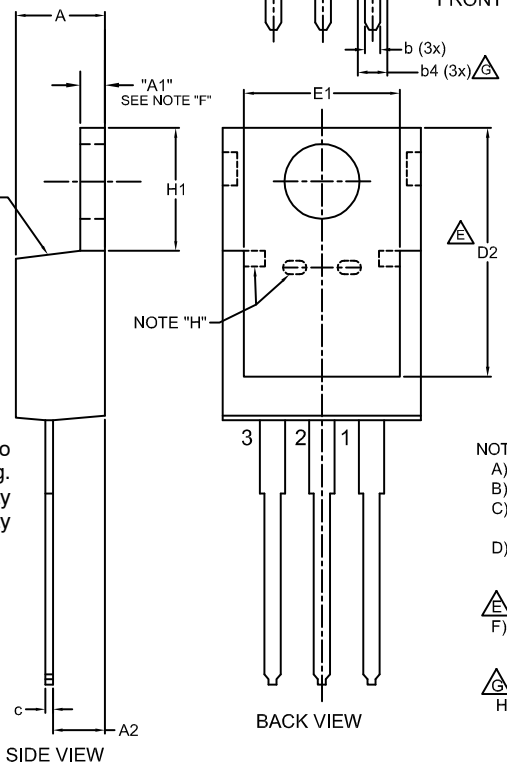


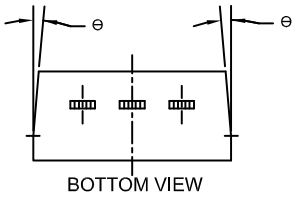
TO−220−3LD
CASE 340AT
ISSUE B

DATE 08 AUG 2022

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	4.00	--	4.70
A1	SEE NOTE "F"		
A2	2.10	--	2.85
b	0.55	--	1.00
b2	1.10	--	1.62
b4	1.42	--	1.62
c	0.36	--	0.60
D	13.90	--	16.30
D1	8.13	--	9.40
D2	11.50	--	14.30
D3	15.42	--	16.51
E	9.65	--	10.67
E1	7.59	--	8.65
e	2.40	--	2.67
H1	6.06	--	6.69
L	12.70	--	14.04
L1	2.70	--	4.10
P	3.50	--	4.00
Q	2.50	--	3.40
z	2.13 REF		
z1	2.06 REF		
Θ	3°	–	5°







GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

NOTES:
A) REFERENCE JEDEC, TO-220, VARIATION AB
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS COMMON TO ALL PACKAGE SUPPLIERS EXCEPT WHERE NOTED [ ].
D) LOCATION OF MOLDED FEATURE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
E) DOES NOT COMPLY JEDEC STANDARD VALUE.
F) "A1" DIMENSIONS AS BELOW:
SINGLE GAUGE = 0.51 - 0.61
DUAL GAUGE = 1.10 - 1.45
G) PRESENCE IS SUPPLIER DEPENDENT
H) SUPPLIER DEPENDENT MOLD LOCKING HOLES IN HEATSINK.

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DESCRIPTION:	**TO−220−3LD**	**PAGE 1 OF 1**

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