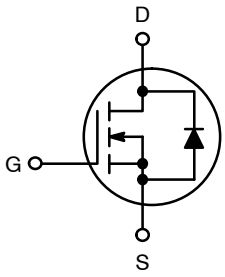
MOSFET – N-Channel, SUPERFET®, FRFET®

600 V, 11 A, 380 mΩ

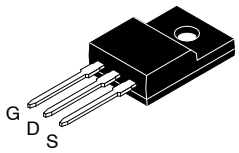
FCPF11N60F

V_{DS}	$R_{DS(on)}$ MAX	I_D MAX
600 V	380 mΩ @ 10 V	11 A*

*Drain current limited by maximum junction temperature.



N−Channel



TO−220 FULLPAK, 3−Lead
/ TO−220F−3SG
CASE 221AT

Description

SUPERFET MOSFET is **onsemi**'s first generation of high voltage super−junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on−resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SUPERFET MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications. SUPERFET FRFET MOSFET's optimized body diode reverse recovery performance can remove additional component and improve system reliability.

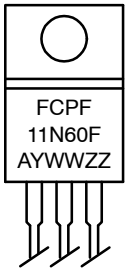
Features

- 600 V @ T_J = 150°C
- $R_{DS(on)}$ = 320 mΩ (Typ.)
- Fast Recovery Type (t_{rr} = 120 ns)
- Ultra Low Gate Charge (Typ. Q_g = 40 nC)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)}$ = 95 pF)
- 100% Avalanche Tested
- These Devices are Pb−Free and are RoHS Compliant

Applications

- LCD/LED/PDP TV
- Lighting
- Solar Inverter
- AC−DC Power Supply

MARKING DIAGRAM



FCPF11N60F	= Specific Device Code
A	= Assembly Location
YWW	= Date Code (Year & Week)
ZZ	= Assembly Lot

ORDERING INFORMATION

Device	Package	Shipping
FCPF11N60F	TO−220−3 FULLPAK	1000 Units / Tube

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MOSFET MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Parameter		FCPF11N60F	Unit
V_{DSS}	Drain to Source Voltage		600	V
I_D	Drain Current	– Continuous (T_C = 25°C)	11*	A
		– Continuous (T_C = 100°C)	7*	
I_{DM}	Drain Current	– Pulsed (Note 1)	33*	A
V_{GSS}	Gate to Source Voltage		±30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		340	mJ
I_{AR}	Avalanche Current (Note 1)		11	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		12.5	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		4.5	V/ns
P_D	Power Dissipation	(T_C = 25°C)	36	W
		– Derate Above 25°C	0.29	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		–55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
*Drain current limited by maximum junction temperature.
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. I_{AS} = 5.5 A, V_{DD} = 50 V, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 11 A, di/dt ≤ 200 A/μs, V_{DD} ≤ BV_{DSS}, starting T_J = 25°C.

THERMAL CHARACTERISTICS

Symbol	Parameter	FCPF11N60F	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	3.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	°C/W

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA, T_C = 25°C	600	–	–	V
		V_{GS} = 0 V, I_D = 250 μA, T_C = 150°C	–	650	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	–	0.6	–	V/°C
BV_{DS}	Drain−Source Avalanche Breakdown Voltage	V_{GS} = 0 V, I_D = 11 A	–	700	–	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 600 V, V_{GS} = 0 V	–	–	1	μA
		V_{DS} = 480 V, T_C = 125°C	–	–	10	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±30 V, V_{DS} = 0 V	–	–	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	3.0	–	5.0	V
$R_{DS(on)}$	Static Drain to Source On−Resistance	V_{GS} = 10 V, I_D = 5.5 A	–	0.32	0.38	Ω
g_{FS}	Forward Transconductance	V_{DS} = 40 V, I_D = 5.5 A	–	6	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	–	1148	1490	pF
C_{oss}	Output Capacitance		–	671	870	pF
C_{rss}	Reverse Transfer Capacitance		–	63	82	pF
C_{oss}	Output Capacitance	V_{DS} = 480 V, V_{GS} = 0 V, f = 1 MHz	–	35	–	pF
$C_{oss(eff.)}$	Effective Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	–	95	–	pF
$Q_{g(tot)}$	Total Gate Charge at 10 V	V_{DS} = 480 V, I_D = 11 A, V_{GS} = 10 V (Note 4)	–	40	52	nC
Q_{gs}	Gate to Source Gate Charge		–	7.2	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	21	–	nC
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 300 V, I_D = 11 A, R_G = 25 Ω (Note 4)	–	34	80	ns
t_r	Turn−On Rise Time		–	98	205	ns
$t_{d(off)}$	Turn−Off Delay Time		–	119	250	ns
t_f	Turn−Off Fall Time		–	56	120	ns
DRAIN−SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuous Drain to Source Diode Forward Current		–	–	11	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		–	–	33	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 11 A	–	–	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 11 A, dI_F/dt = 100 A/μs	–	120	–	ns
Q_{rr}	Reverse Recovery Charge		–	0.8	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature

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TYPICAL PERFORMANCE CHARACTERISTICS

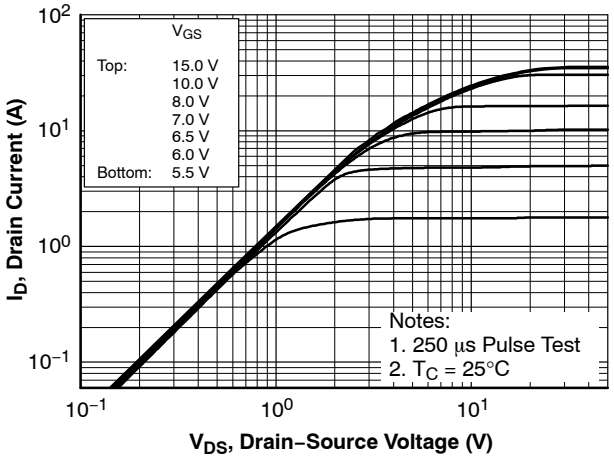


Figure 1. On−Region Characteristics

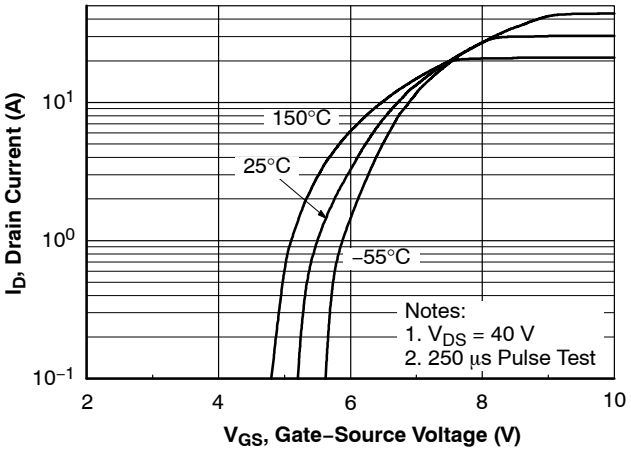


Figure 2. Transfer Characteristics

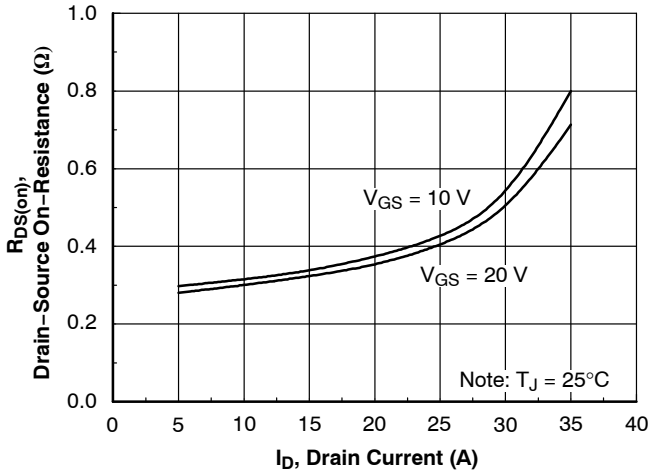


Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage

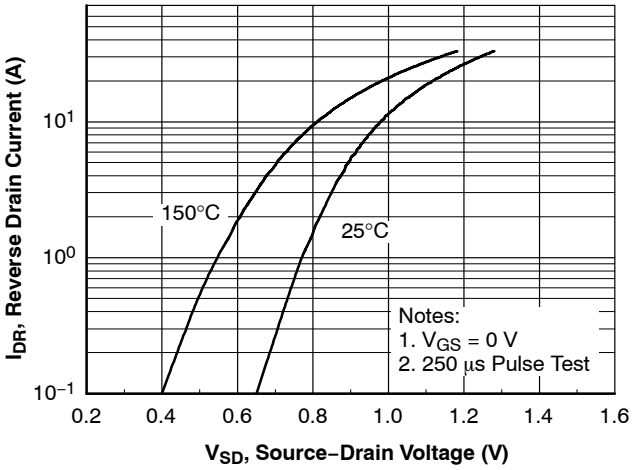


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

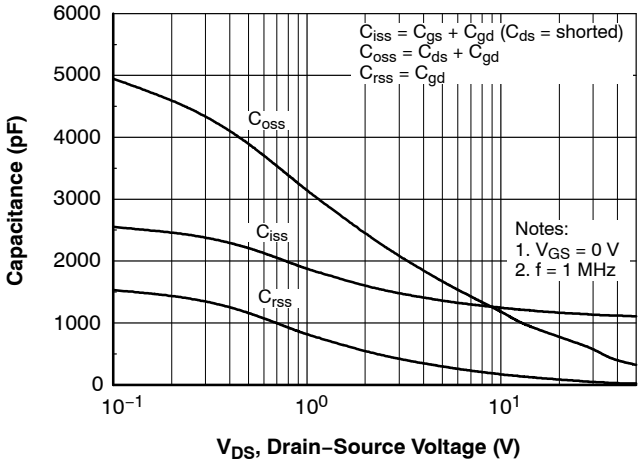


Figure 5. Capacitance Characteristics

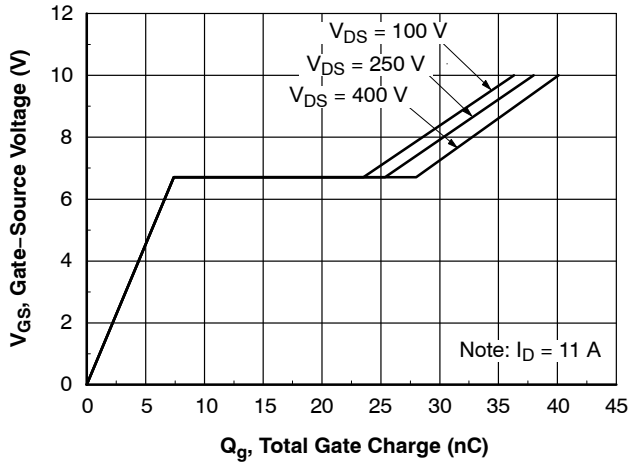


Figure 6. Gate Charge Characteristics

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TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

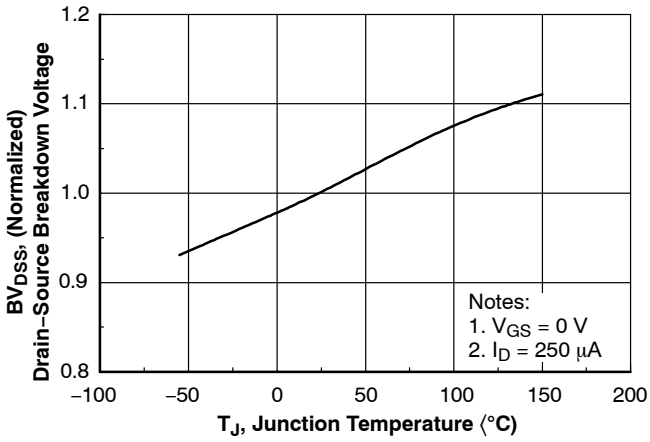


Figure 7. Breakdown Voltage Variation vs. Temperature

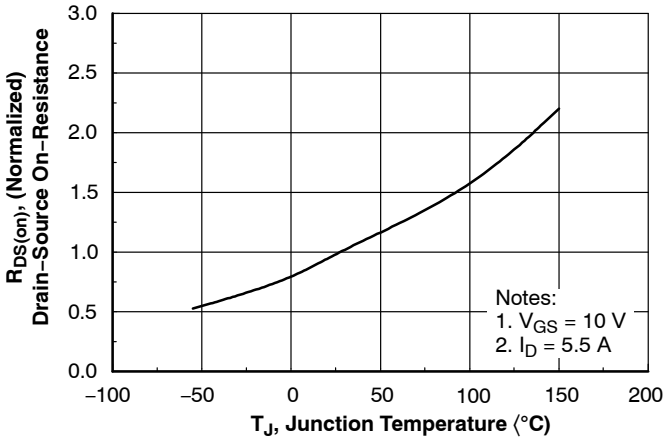


Figure 8. On−Resistance Variation vs. Temperature

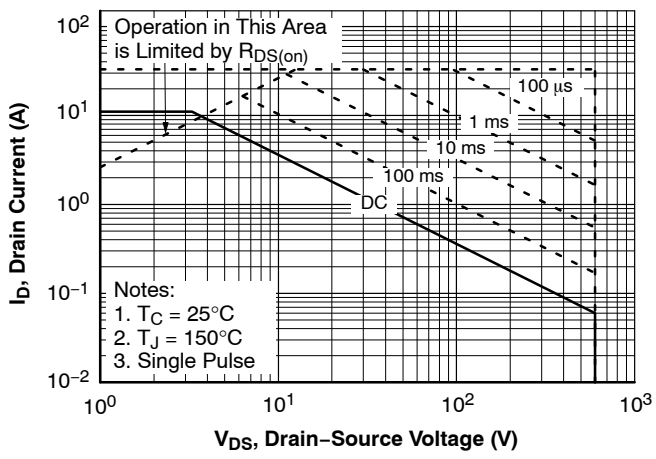


Figure 9. Safe Operating Area

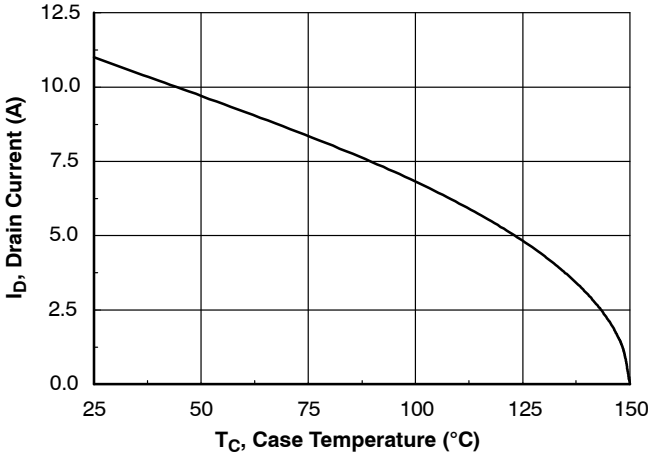


Figure 10. Maximum Drain Current vs. Case Temperature

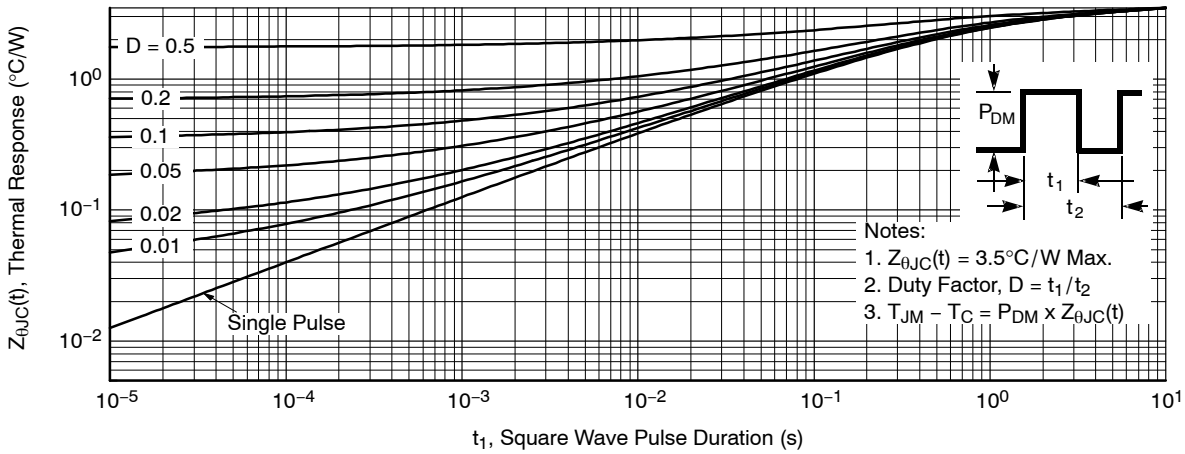


Figure 11. Transient Thermal Response Curve

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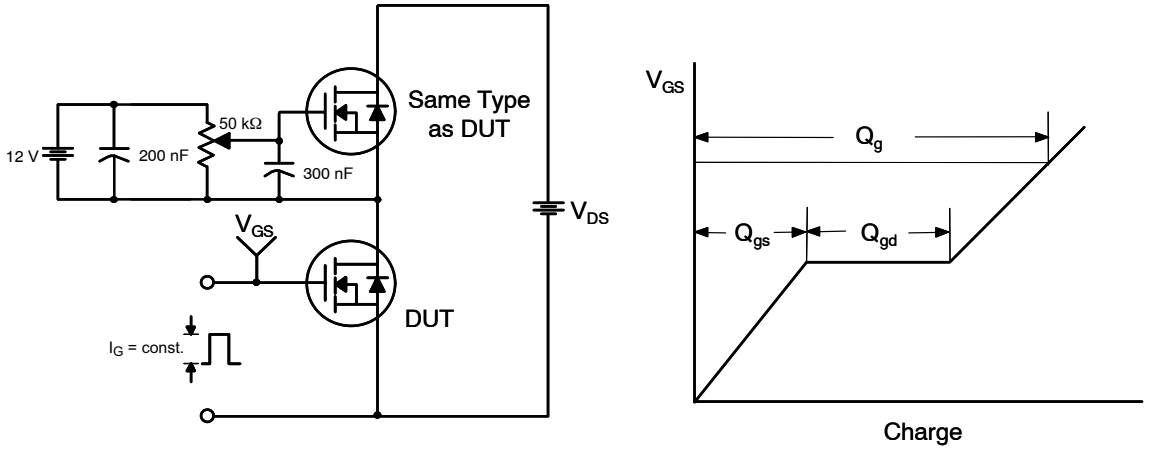


Figure 12. Gate Charge Test Circuit & Waveform

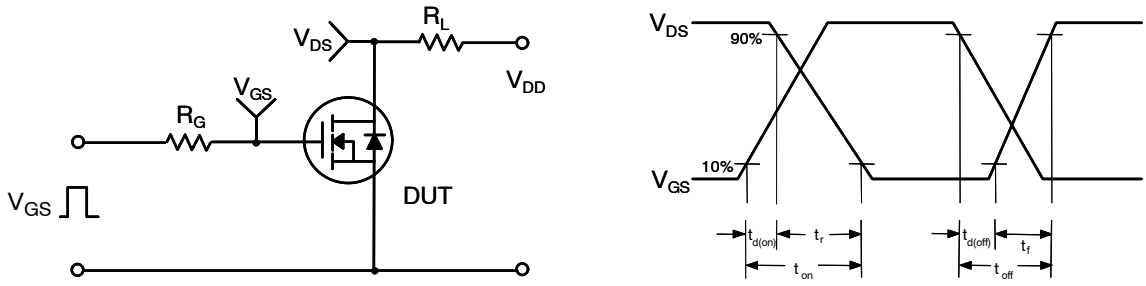


Figure 13. Resistive Switching Test Circuit & Waveforms

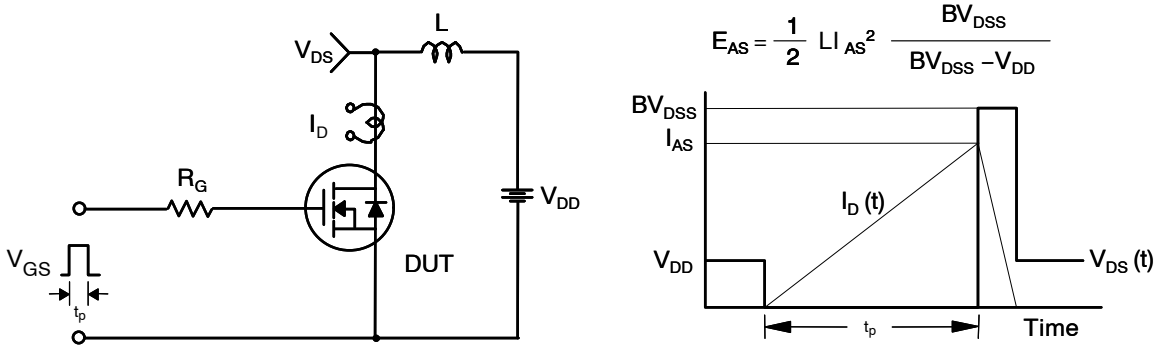


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

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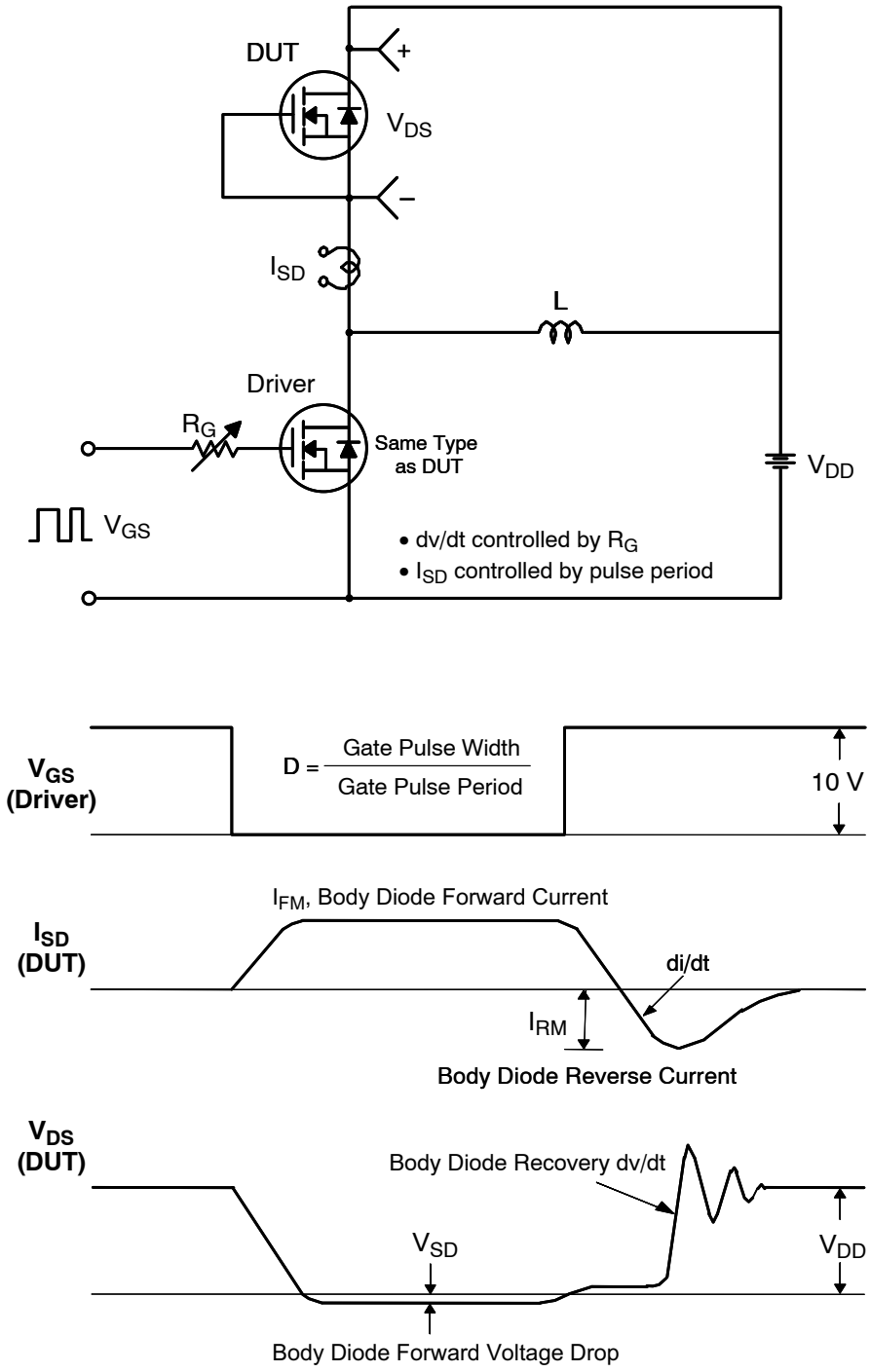


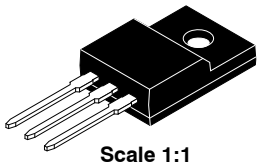
Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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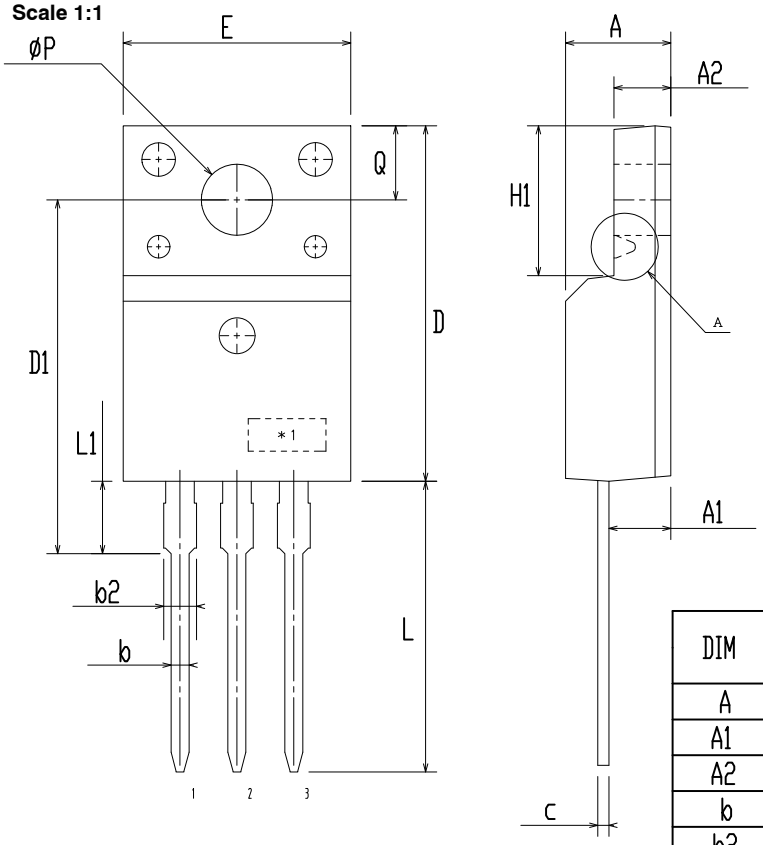
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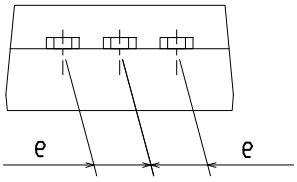
TO−220 Fullpack, 3−Lead / TO−220F−3SG
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ISSUE B

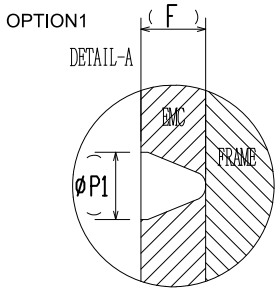
DATE 19 JAN 2021



Scale 1:1







DIM	MILLIMITERS		
	MIN	NOM	MAX
A	4.50	4.70	4.90
A1	2.56	2.76	2.96
A2	2.34	2.54	2.74
b	0.70	0.80	0.90
b2	~	~	1.47
c	0.45	0.50	0.60
D	15.67	15.87	16.07
D1	15.60	15.80	16.00
E	9.96	10.16	10.36
e	2.34	2.54	2.74
F	~	0.84	~
H1	6.48	6.68	6.88
L	12.78	12.98	13.18
L1	3.03	3.23	3.43
ø P	2.98	3.18	3.38
ø P1	~	1.00	~
Q	3.20	3.30	3.40

NOTES:
A. DIMENSION AND TOLERANCE AS ASME Y14.5-2009
B. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUCSIONS.
C. OPTION 1 - WITH SUPPORT PIN HOLE
OPTION 2 - NO SUPPORT PIN HOLE

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DESCRIPTION:	**TO−220 FULLPACK, 3−LEAD / TO−220F−3SG**		**PAGE 1 OF 1**

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