MOSFET – Power, N-Channel, SUPERFET III, Easy Drive
650 V, 17 A, 190 mΩ

FCPF190N65S3R0L

Description

SUPERFET III MOSFET is ON Semiconductor's brand−new high voltage super−junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on−resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate. Consequently, SUPERFET III MOSFET Easy drive series helps manage EMI issues and allows for easier design implementation.

Features

- 700 V @ T_J = 150°C
- Typ. $R_{DS(on)}$ = 159 mΩ
- Ultra Low Gate Charge (Typ. Q_g = 33 nC)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)}$ = 300 pF)
- 100% Avalanche Tested
- This Device is Pb−Free and is RoHS Compliant

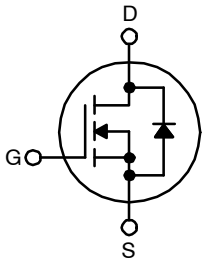
Applications

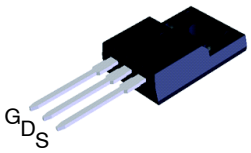
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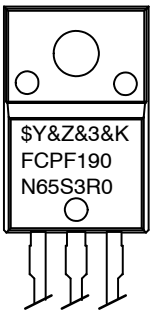
V_{DSS}	$R_{DS(on)}$ MAX	I_D MAX
650 V	190 mΩ @ 10 V	17 A





TO−220
CASE 340BF

MARKING DIAGRAM



$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FCPF190N65S3R0	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

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ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Parameter		Value	Unit
V_{DSS}	Drain to Source Voltage		650	V
V_{GSS}	Gate to Source Voltage	DC	±30	V
		AC (f > 1 Hz)	±30	V
I_D	Drain Current	Continuous (T_C = 25°C)	17*	A
		Continuous (T_C = 100°C)	11*	
I_{DM}	Drain Current	Pulsed (Note 1)	42.5*	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		76	mJ
I_{AS}	Avalanche Current (Note 2)		2.5	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		1.44	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt (Note 3)		20	
P_D	Power Dissipation	T_C = 25°C	33	W
		Derate Above 25°C	1.15	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		−55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8” from Case for 5 Seconds		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
*Drain current limited by maximum junction temperature.
1. Repetitive rating: pulse−width limited by maximum junction temperature.
2. I_{AS} = 2.5 A, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 8.5 A, di/dt ≤ 200 A/ms, V_{DD} ≤ 400 V, starting T_J = 25°C.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	3.76	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCPF190N65S3R0L	FCPF190N65S3R0	TO−220F	Tube	N/A	N/A	50 Units

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 1 mA, T_J = 25°C	650			V
		V_{GS} = 0 V, I_D = 1 mA, T_J = 150°C	700			V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 1 mA, Referenced to 25ºC		0.6		V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 650 V, V_{GS} = 0 V			1	μA
		V_{DS} = 520 V, T_C = 125ºC		0.89		
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±30 V, V_{DS} = 0 V			±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 0.39 mA	2.5		4.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 8.5 A		159	190	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 20 V, I_D = 8.5 A		10		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 400 V, V_{GS} = 0 V, f = 1 MHz		1350		pF
C_{oss}	Output Capacitance			30		pF
$C_{oss(eff.)}$	Effective Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V		300		pF
$C_{oss(er.)}$	Energy Related Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V		43		pF
$Q_{g(tot)}$	Total Gate Charge at 10V	V_{DS} = 400 V, I_D = 8.5 A, V_{GS} = 10 V (Note 4)		33		nC
Q_{gs}	Gate to Source Gate Charge			7.9		nC
Q_{gd}	Gate to Drain “Miller” Charge			14		nC
ESR	Equivalent Series Resistance	f = 1 MHz		0.5		Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 400 V, I_D = 8.5 A, V_{GS} = 10 V, R_g = 4.7 Ω (Note 4)		17		ns
t_r	Turn−On Rise Time			16		ns
$t_{d(off)}$	Turn−Off Delay Time			42		ns
t_f	Turn−Off Fall Time			6		ns
SOURCE−DRAIN DIODE CHARACTERISTICS						
I_S	Maximum Continuous Source to Drain Diode Forward Current				17	A
I_{SM}	Maximum Pulsed Source to Drain Diode Forward Current				42.5	A
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 8.5 A			1.2	V
t_{rr}	Reverse Recovery Time	V_{DD} = 400 V, I_{SD} = 8.5 A, dI_F/dt = 100 A/ms		313		ns
Q_{rr}	Reverse Recovery Charge			4.9		μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

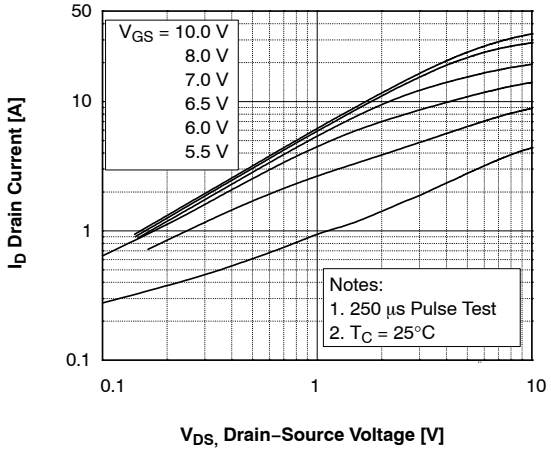


Figure 1. On−Region Characteristics

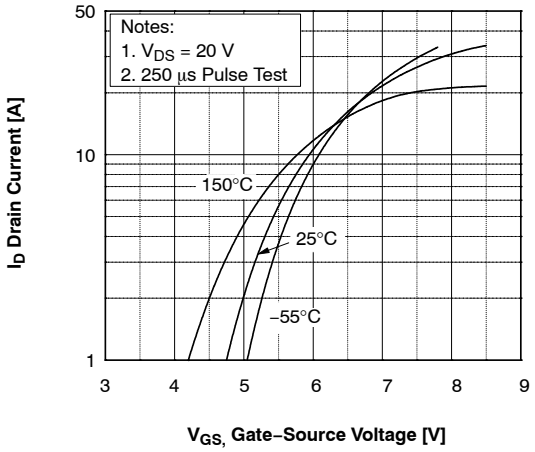


Figure 2. Transfer Characteristics

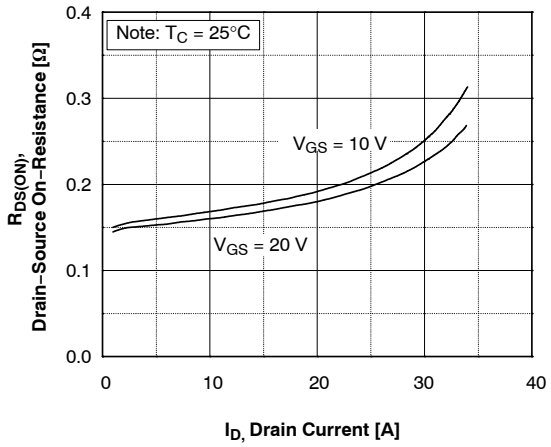


Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage

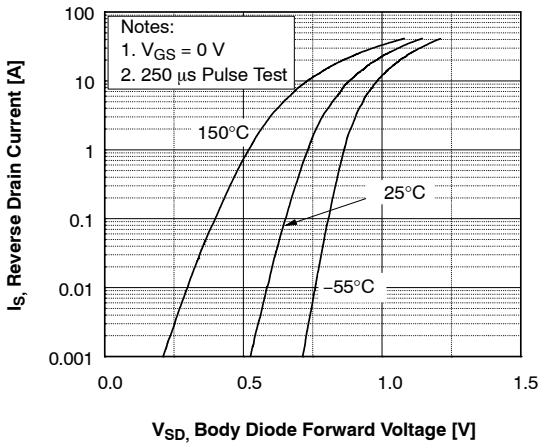


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

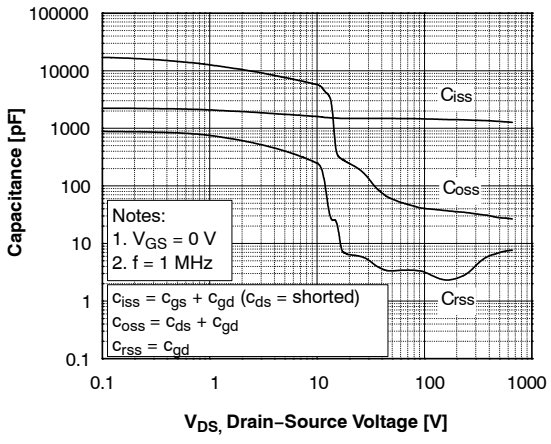


Figure 5. Capacitance Characteristics

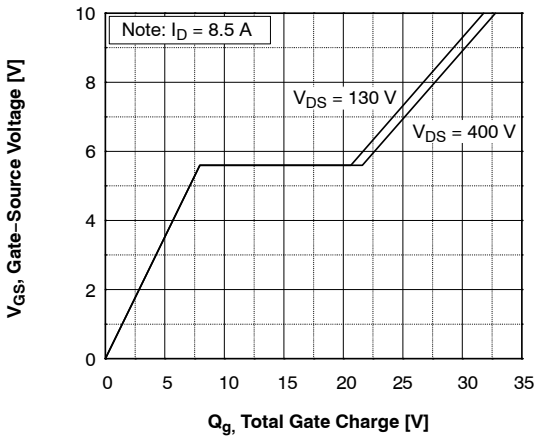


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

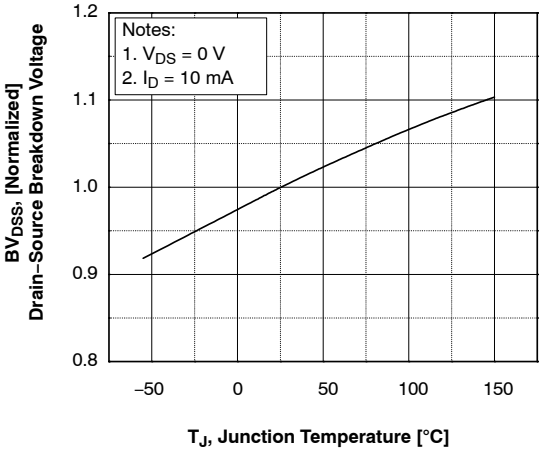


Figure 7. Breakdown Voltage Variation vs. Temperature

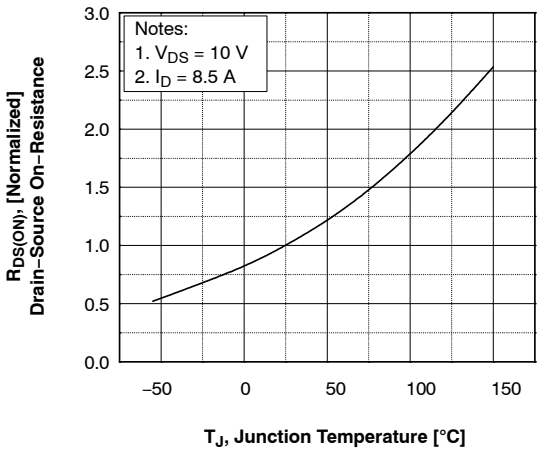


Figure 8. On−Resistance Variation vs. Temperature

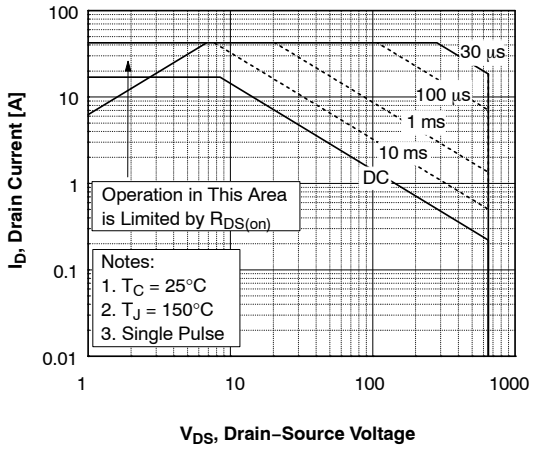


Figure 9. Maximum Safe Operating Area

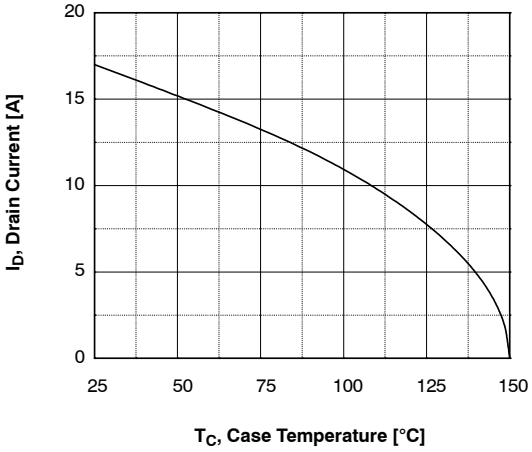


Figure 10. Maximum Drain Current vs. Case Temperature

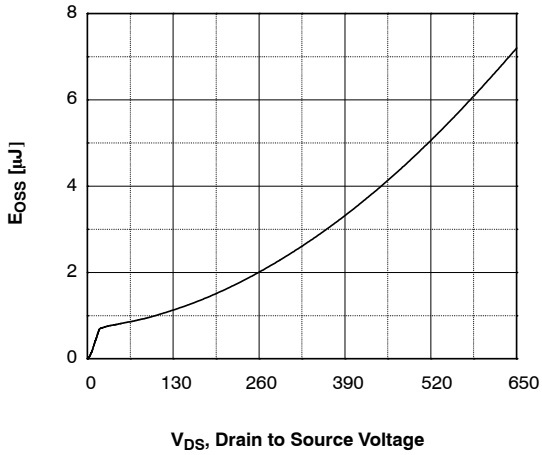


Figure 11. E_{oss} vs. Drain to Source Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

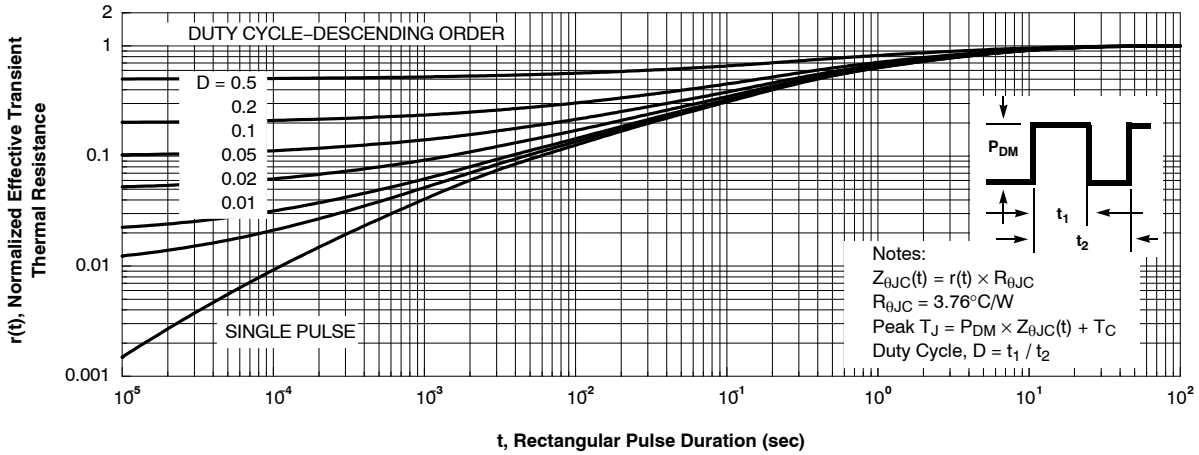


Figure 12. Transient Thermal Response Curve

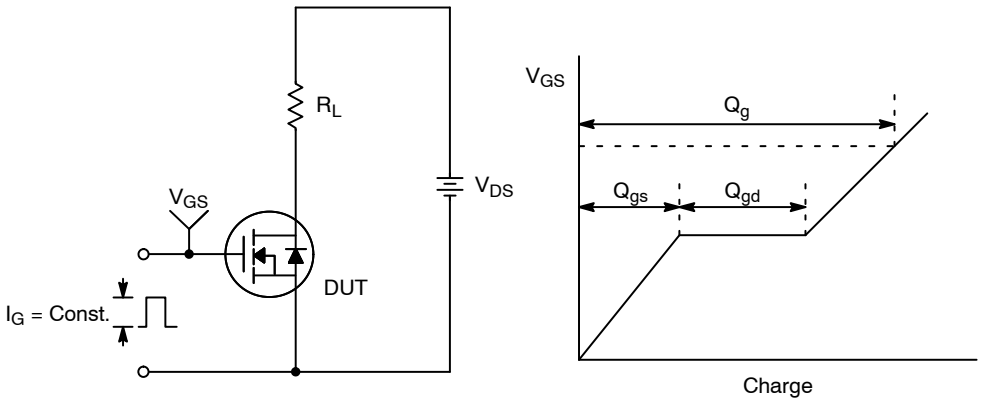


Figure 13. Gate Charge Test Circuit & Waveform

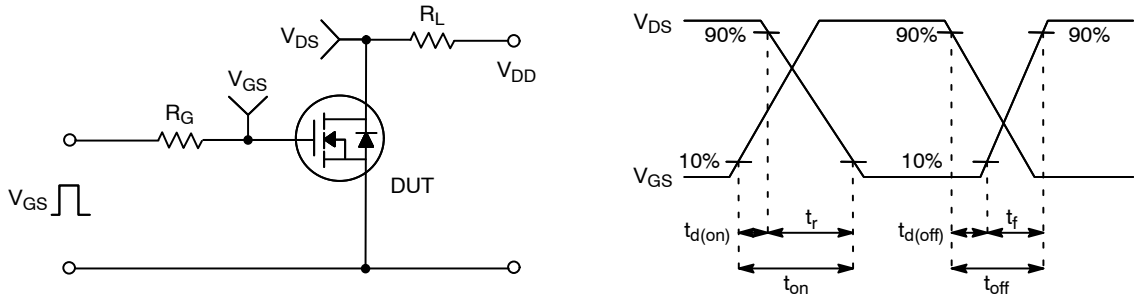


Figure 14. Resistive Switching Test Circuit & Waveforms

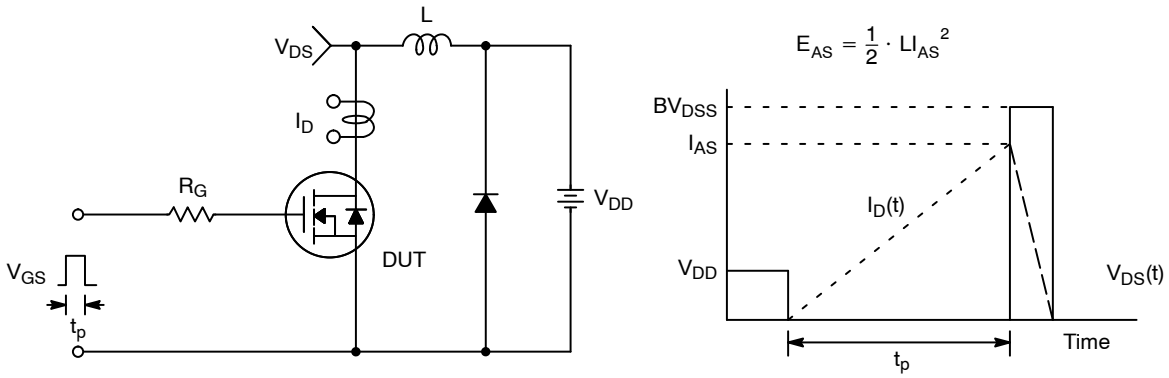


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

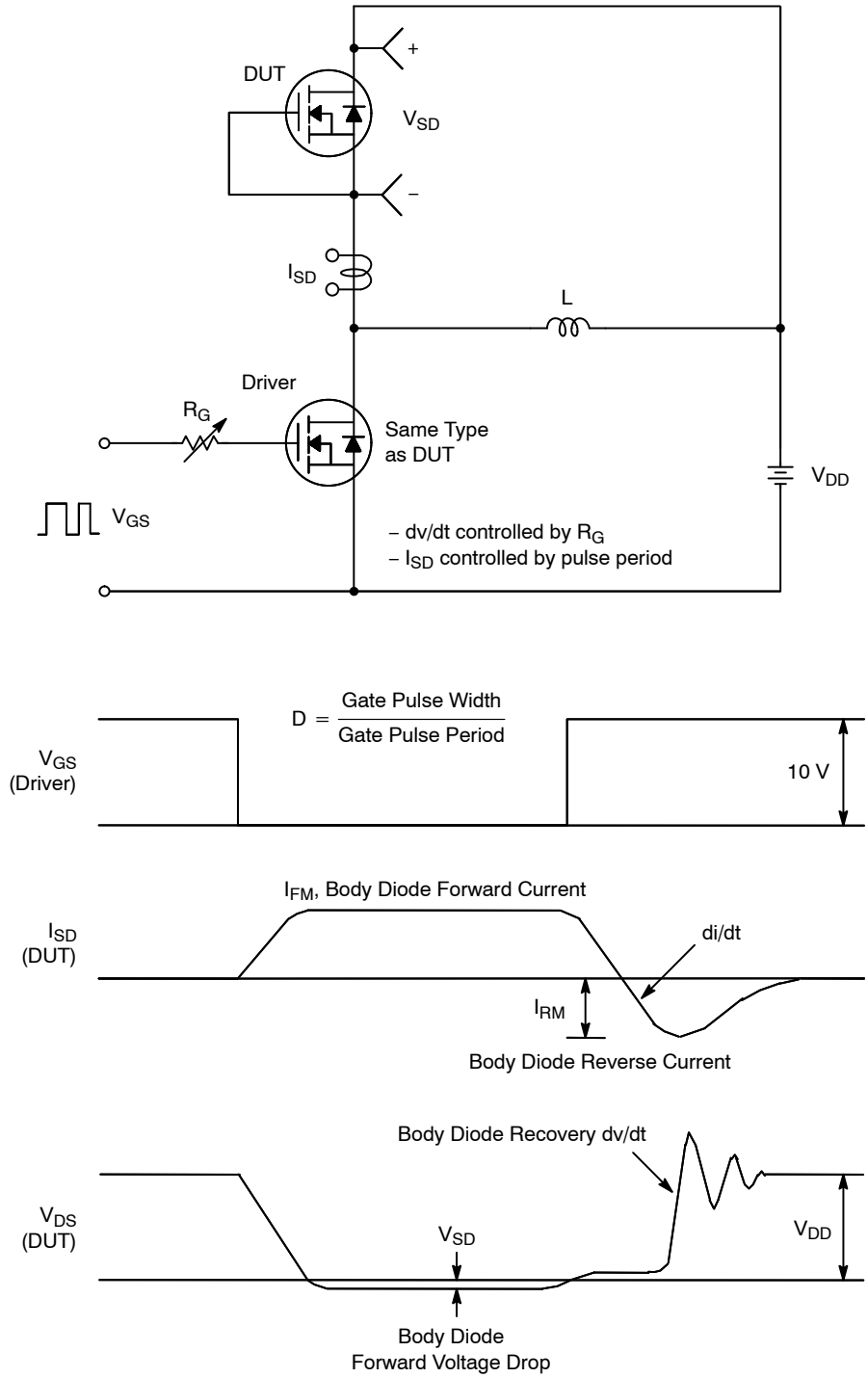
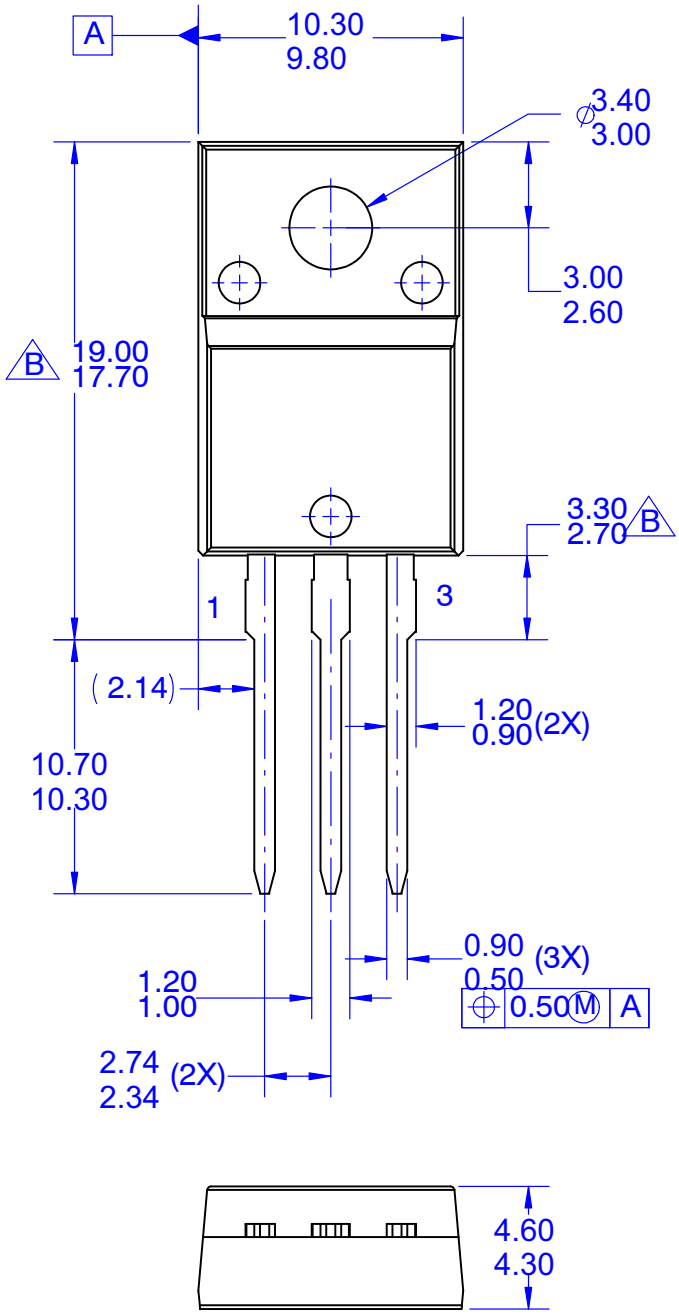


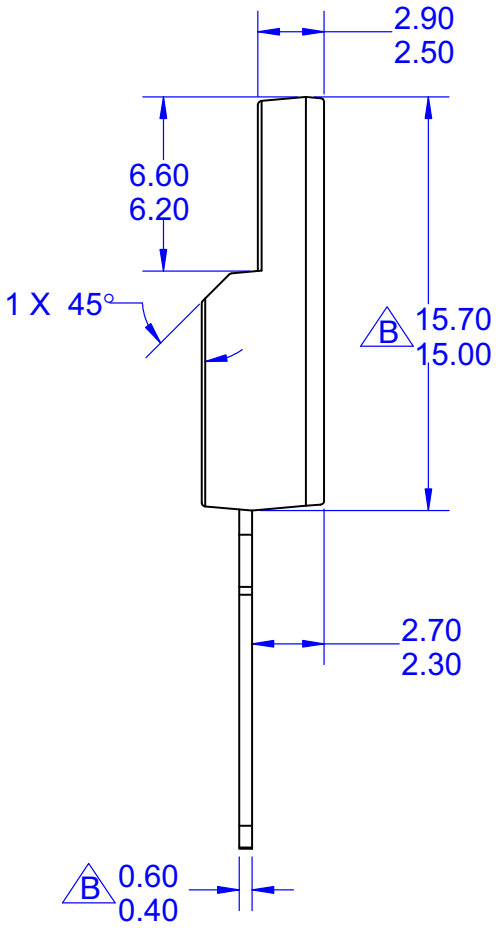
Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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TO−220 FULLPAK 3LD
CASE 340BF
ISSUE O

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NOTES:

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B. DOES NOT COMPLY EIAJ STD. VALUE.
C. ALL DIMENSIONS ARE IN MILLIMETERS.
D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
E. DIMENSION AND TOLERANCE AS PER ASME Y14.5−2009.

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