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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

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October 2024

FDB0105N407L

N-Channel PowerTrench® MOSFET

40 V, 460 A, 0.8 mΩ

Features

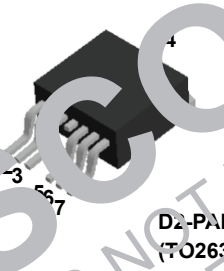
- Max $r_{DS(on)}$ = 0.8 mΩ at V_{GS} = 10 V, I_D = 50 A
- Max $r_{DS(on)}$ = 1.1 mΩ at V_{GS} = 6 V, I_D = 42 A
- Fast Switching Speed
- Low Gate Charge
- High Performance Trench Technology for Extremely Low $R_{DS(on)}$
- High Power and Current Handling Capability
- RoHS Compliant

General Description

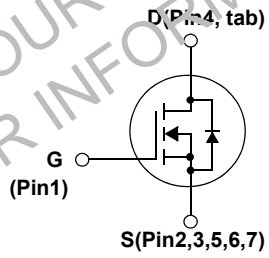
This N-Channel MOSFET is produced using Fairchild Semiconductor's advance PowerTrench® process that has been especially tailored to minimize the on-state resistance while maintaining superior ruggedness and switching performance for industrial applications.

Applications

- Industrial Motor Drive
- Industrial Power Supply
- Industrial Automation
- Battery Operated tools
- Battery Protection
- Solar Inverters
- UPS and Energy Inverters
- Energy Storage
- Load Switch



D2-PAK
(TO263)



MOSFET Maximum Ratings T_C = 25 °C unless otherwise noted.

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			40	V
V_{GS}	Gate to Source Voltage			±20	V
I_D	Drain Current -Continuous	T_C = 25°C	(Note 5)	460	A
	-Continuous	T_C = 100°C	(Note 5)	330	
	-Pulsed		(Note 4)	2540	
E_{AS}	Single Pulse Avalanche Energy		(Note 3)	1109	mJ
P_D	Power Dissipation	T_C = 25°C		300	W
	Power Dissipation	T_A = 25°C	(Note 1a)	3.8	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +175	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Note 1)	0.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	40	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB0105N407L	FDB0105N407L	D2-PAK-7L	330mm	24mm	800 units

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Electrical Characteristics T_J = 25 °C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	40			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		13		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 32 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2	2.8	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C				mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 50 A		1.6	1.8	mΩ
		V_{GS} = 6 V, I_D = 42 A		0.[illegible]	1.1	
		V_{GS} = 10 V, I_D = 50 A, T_J = 15[illegible] °C		1	1.8	
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 50 A		286		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 20[illegible] V, V_{G} = [illegible] V, f = 1[illegible] MHz		16500	23100	pF
C_{oss}	Output Capacitance			5335	7470	pF
C_{rss}	Reverse Transfer Capacitance			473	1065	pF
R_g	Gate Resistance			2.6		Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 20[illegible] V, I_D = 50 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		45	73	ns
t_r	Rise Time			69	110	ns
$t_{d(off)}$	Turn-Off Delay Time			117	186	ns
t_f	Fall Time			61	97	ns
Q_g	Total Gate Charge	V_{DD} = 20[illegible] V, I_D = 50 A, V_{GS} = 10 V		208	291	nC
Q_{gs}	Gate to Source Gate Charge			64		nC
Q_{gd}	Gate to Drain “Miller” Charge			29		nC
Drain-Source Diode Characteristics						
	Maximum Continuous Drain to Source Diode Forward Current		-	-	460	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	2540	A
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 50 A (Note 2)		0.8	1.2	V
t_{rr}	Reverse Recovery Time	I_F = 50 A, di/dt = 100 A/μs		107	171	ns
Q_{rr}	Reverse Recovery Charge			119	191	nC

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

   a) 40 °C/W when mounted on a 1 in^2 pad of 2 oz copper.
   b) 62.5 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0 %.

3. E_{AS} of 1109 mJ is based on starting T_J = 25 °C, L = 0.3 mH, I_{AS} = 86 A, V_{DD} = 10 V, V_{GS} = 36 V. 100% test at L = 0.1 mH, I_{AS} = 125 A.

4. Pulsed Id please refer to Figure “Forward Bias Safe Operating Area” for more details.

5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

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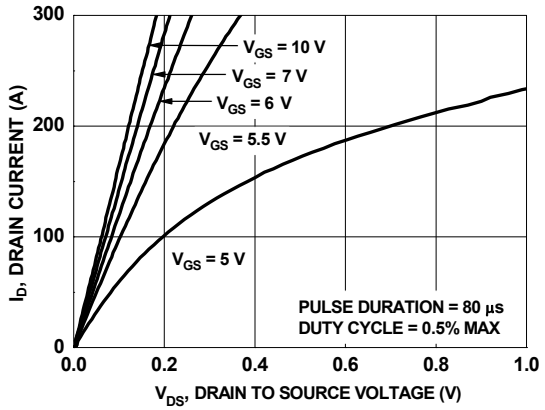


Figure 1. On Region Characteristics

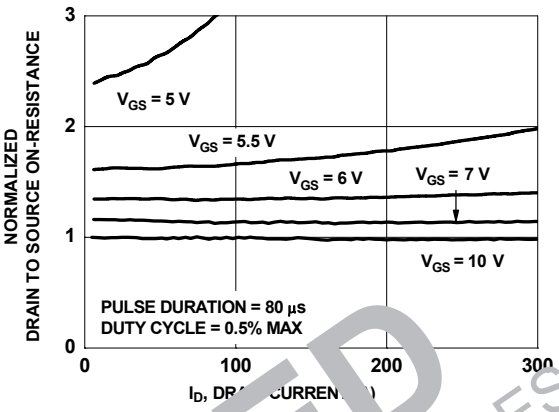


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

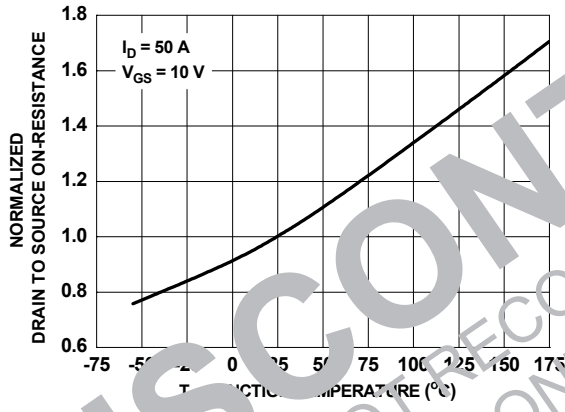


Figure 3. Normalized On Resistance vs. Junction Temperature

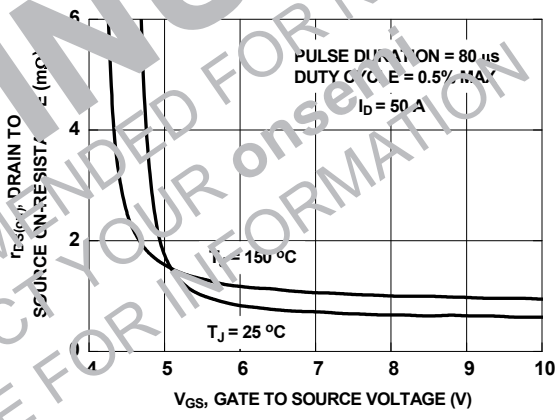


Figure 4. On-Resistance vs. Gate to Source Voltage

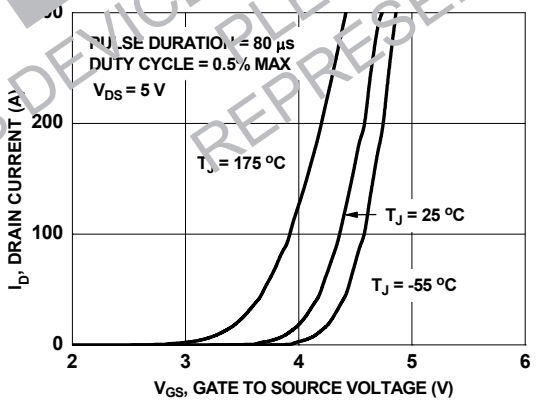


Figure 5. Transfer Characteristics

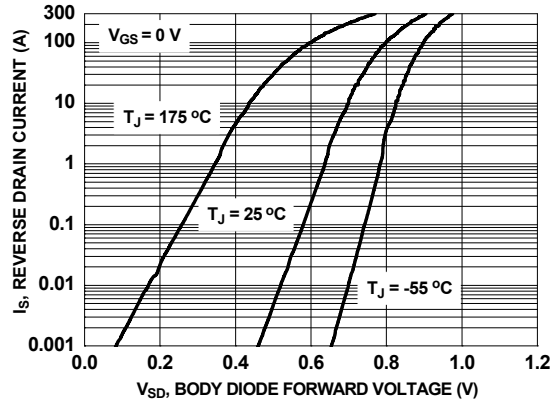


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

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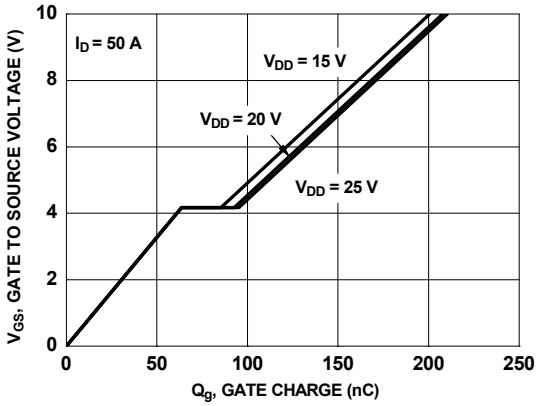


Figure 7. Gate Charge Characteristics

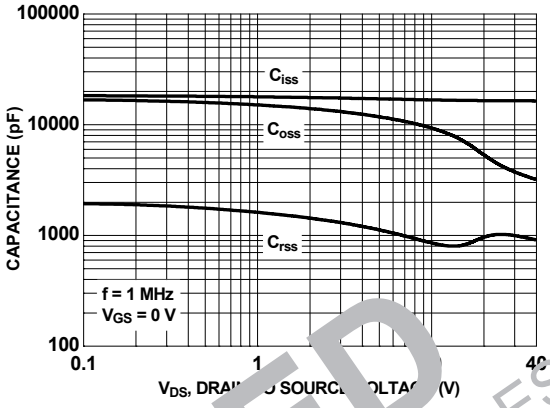


Figure 8. Capacitance vs. Drain to Source Voltage

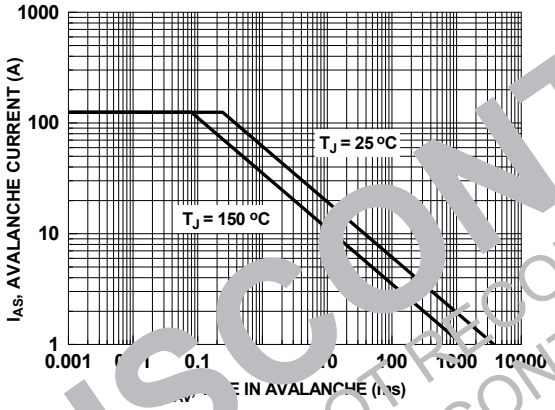


Figure 9. Unclamped Inductive Switching Capability

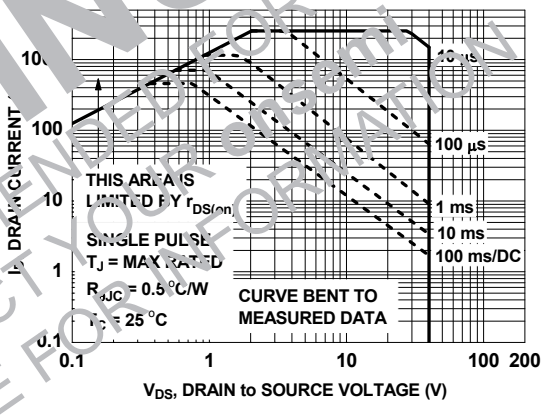


Figure 10. Forward Bias Safe Operating Area

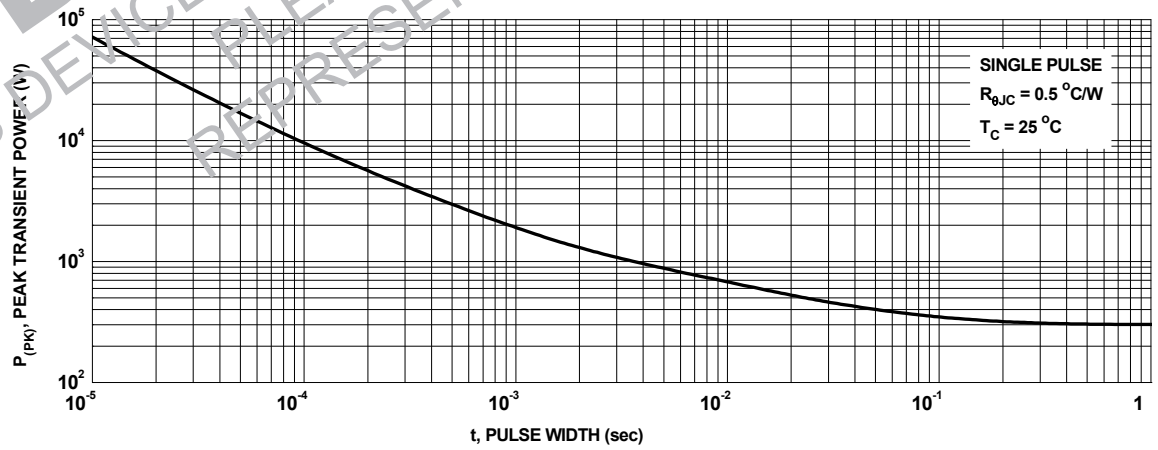


Figure 11. Single Pulse Maximum Power Dissipation

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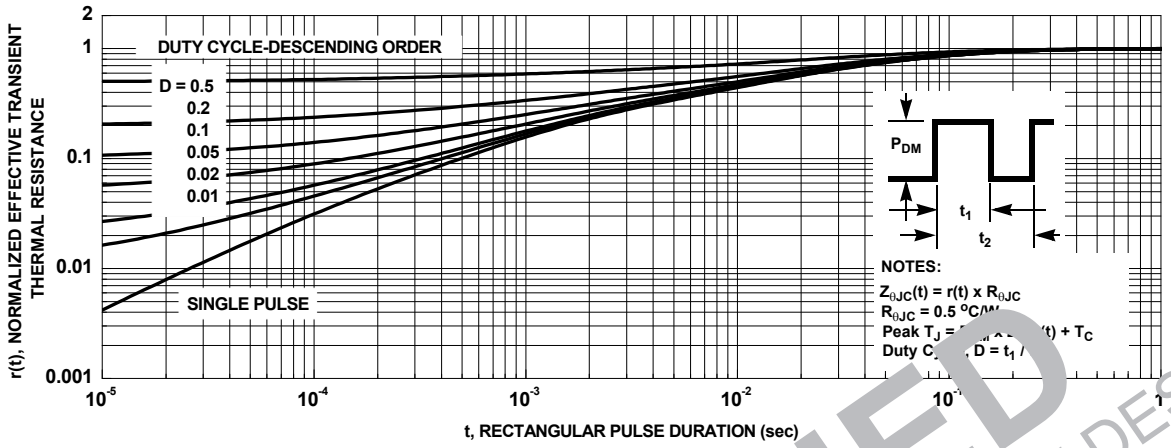
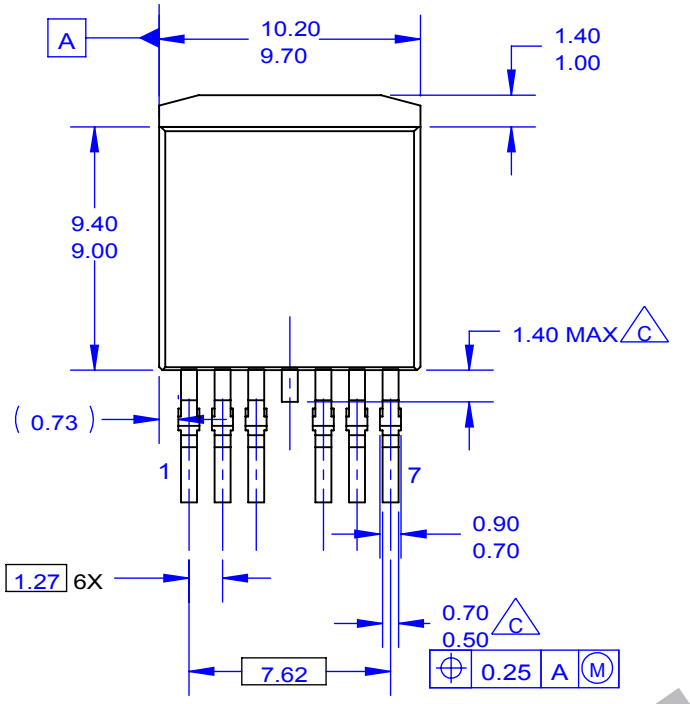
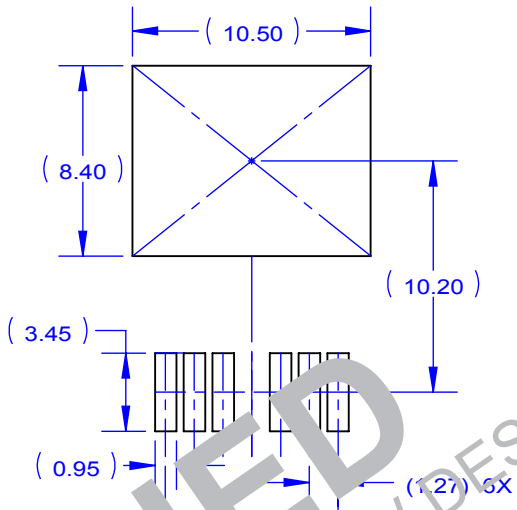


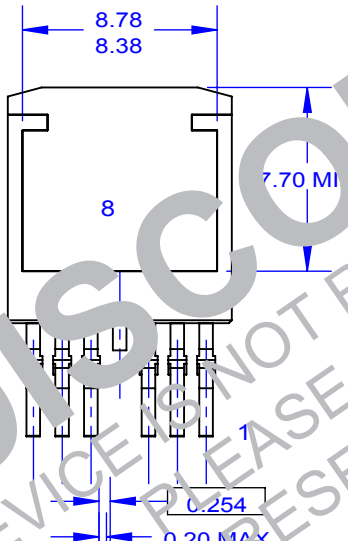
Figure 12. Junction-to-Case Transient Thermal Response Curve

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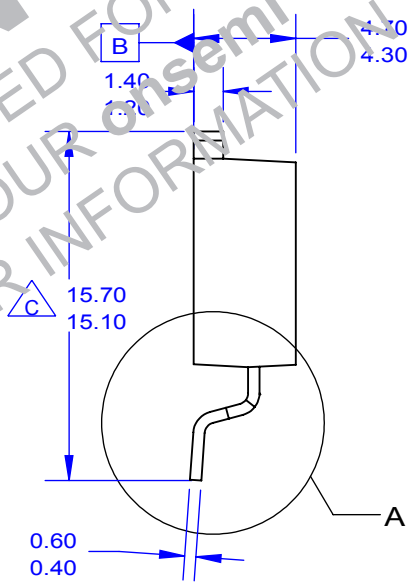




LAND PATTERN RECOMMENDATION



DETAIL A
SCALE 2:1



NOTES:

A. PACKAGE CONFORMS TO JEDEC TO-263 VARIATION CB EXCEPT WHERE NOTED.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C OUT OF JEDEC STANDARD VALUE.
D. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
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F. LAND PATTERN RECOMMENDATION PER IPC. TO127P1524X465-8N.
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