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FDD86250_F085 (Note1)

N-Channel Sheilded Gate PowerTrench® MOSFET

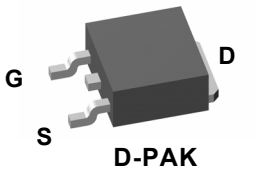
150 V, 50 A, 22 mΩ

Features

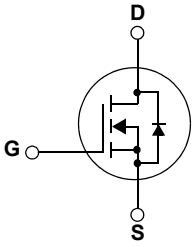
- Typical $R_{DS(on)}$ = 19.4 mΩ at V_{GS} = 10V, I_D = 20 A
- Typical $Q_{g(tot)}$ = 28 nC at V_{GS} = 10V, I_D = 40 A
- UIS Capability
- RoHS Compliant
- Qualified to AEC Q101

Applications

- Automotive Engine Control
- PowerTrain Management
- Solenoid and Motor Drivers
- Integrated Starter/Alternator
- Distributed Power Architectures and VRM
- Primary Switch for 12V Systems



D-PAK
(TO-252)



MOSFET Maximum Ratings T_J = 25°C unless otherwise noted.

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-to-Source Voltage		150	V
V_{GS}	Gate-to-Source Voltage		±20	V
I_D	Drain Current - Continuous (V_{GS}=10V) (Note 2)	T_C = 25°C	50	A
	Pulsed Drain Current	T_C = 25°C	See Figure 4	
E_{AS}	Single Pulse Avalanche Energy	(Note 3)	80	mJ
P_D	Power Dissipation		160	W
	Derate Above 25°C		1.06	W/°C
T_J, T_{STG}	Operating and Storage Temperature		-55 to + 175	°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case		0.94	°C/W
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient	(Note 4)	40	°C/W

Notes:

1: Due to system integration constraints between Fairchild and ON semiconductor, as of November 1, 2017 any product part number with a underscore will be replaced with a dash. This is a notification.
2: Current is limited by bondwire configuration.
3: Starting T_J = 25°C, L = 0.1mH, I_{AS} = 40A, V_{DD} = 135V during inductor charging and V_{DD} = 0V during time in avalanche.
4: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$is determined by the board design. The maximum rating presented here is based on mounting on a 1 in^2 pad of 2oz copper.

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD86250	FDD86250_F085	D-PAK(TO-252)	13”	16mm	2500units

Electrical Characteristics T_J = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Off Characteristics						
B_{VDSS}	Drain-to-Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V	150	-	-	V
I_{DSS}	Drain-to-Source Leakage Current	V_{DS} = 150V, V_{GS} = 0V, T_J = 25°C	-	-	1	μA
		V_{DS} = 150V, V_{GS} = 0V, T_J = 175°C (Note 5)	-	-	1	mA
I_{GSS}	Gate-to-Source Leakage Current	V_{GS} = ±20V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	2	3	4	V
$R_{DS(on)}$	Drain to Source On Resistance	I_D = 20A, V_{GS}= 10V, T_J = 25°C	-	19.4	22	mΩ
		I_D = 20A, V_{GS}= 10V, T_J = 175°C (Note 5)	-	56	62	mΩ
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 75V, V_{GS} = 0V, f = 1MHz	-	1900	-	pF
C_{oss}	Output Capacitance		-	169	-	pF
C_{rss}	Reverse Transfer Capacitance		-	10	-	pF
R_g	Gate Resistance	f = 1MHz	-	0.5	-	Ω
$Q_{g(ToT)}$	Total Gate Charge	V_{GS} = 0 to 10V, V_{DD} = 120V, I_D = 40A	-	28	37	nC
$Q_{g(th)}$	Threshold Gate Charge	V_{GS} = 0 to 2V, V_{DD} = 120V, I_D = 40A	-	4	-	nC
Q_{gs}	Gate-to-Source Gate Charge	V_{DD} = 120V, I_D = 40A	-	11	-	nC
Q_{gd}	Gate-to-Drain “Miller“ Charge	V_{DD} = 120V, I_D = 40A	-	7	-	nC
Switching Characteristics						
t_{on}	Turn-On Time	V_{DD} = 75V, I_D = 40A, V_{GS} = 10V, R_{GEN} = 6Ω	-		64	ns
$t_{d(on)}$	Turn-On Delay		-	14	-	ns
t_r	Rise Time		-	34	-	ns
$t_{d(off)}$	Turn-Off Delay		-	23	-	ns
t_f	Fall Time		-	5	-	ns
t_{off}	Turn-Off Time		-	-	37	ns
Drain-Source Diode Characteristics						
V_{SD}	Source-to-Drain Diode Voltage	I_{SD} = 40A, V_{GS} = 0V	-	0.9	1.25	V
		I_{SD} = 20A, V_{GS} = 0V	-	0.8	1.2	V
t_{rr}	Reverse-Recovery Time	V_{DD} = 120V, I_F = 40A, dI_{SD}/dt = 100A/μs	-	91	137	ns
Q_{rr}	Reverse-Recovery Charge		-	237	355	nC

Note:

5: The maximum value is specified by design at T_J = 175°C. Product is not tested to this condition in production.

Typical Characteristics

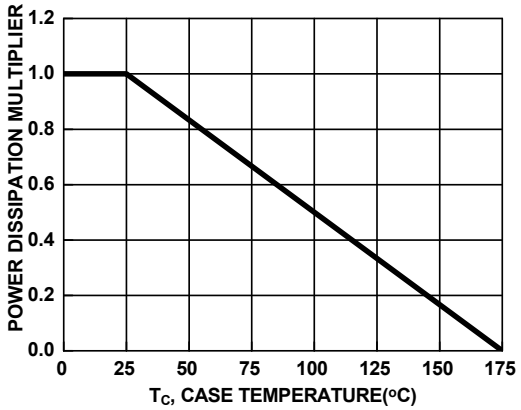


Figure 1. Normalized Power Dissipation vs. Case Temperature

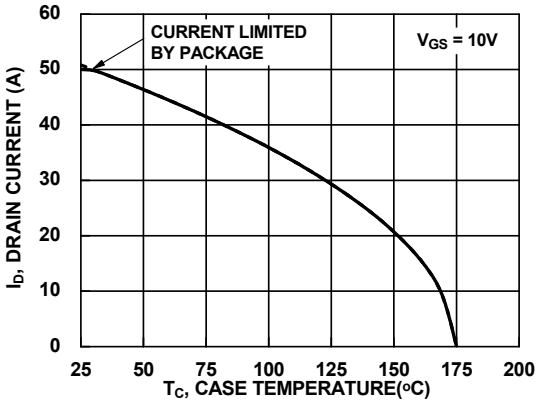


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

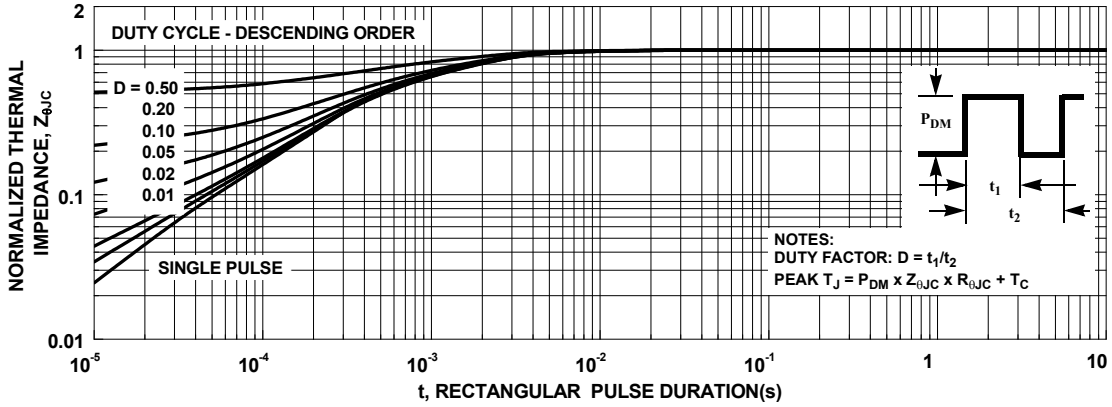


Figure 3. Normalized Maximum Transient Thermal Impedance

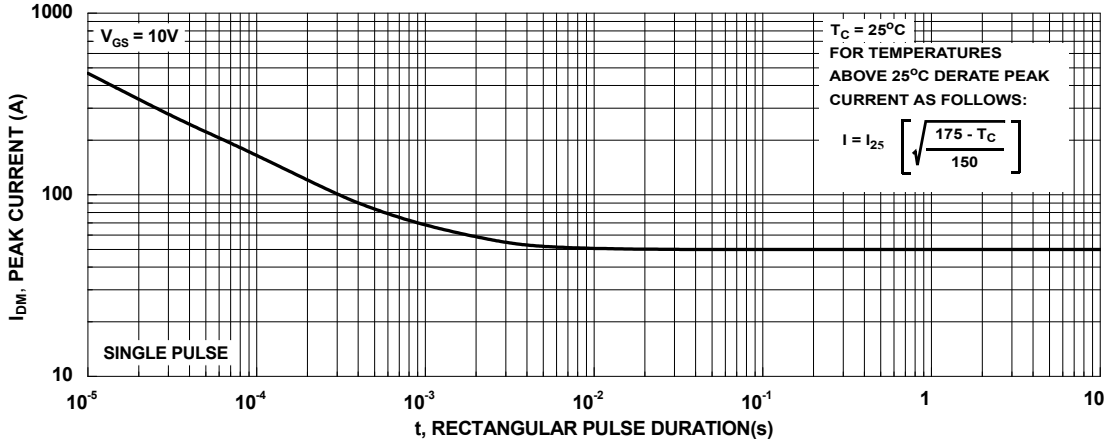


Figure 4. Peak Current Capability

Typical Characteristics

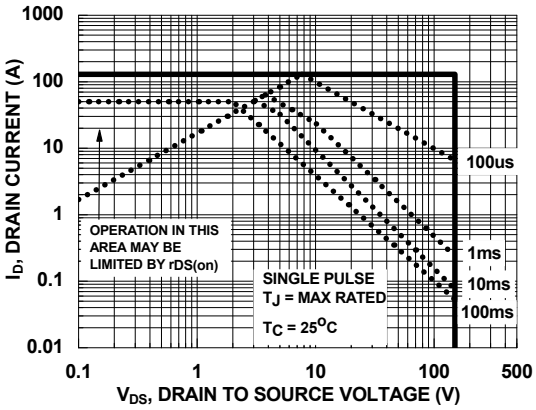
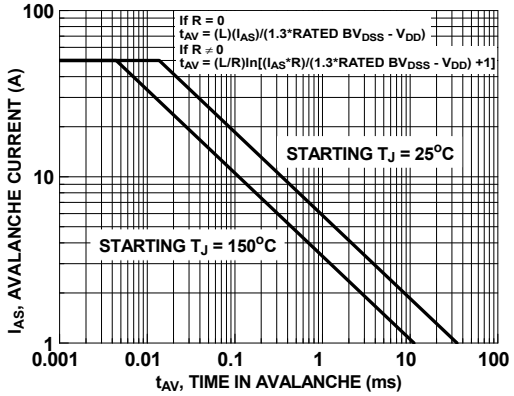


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

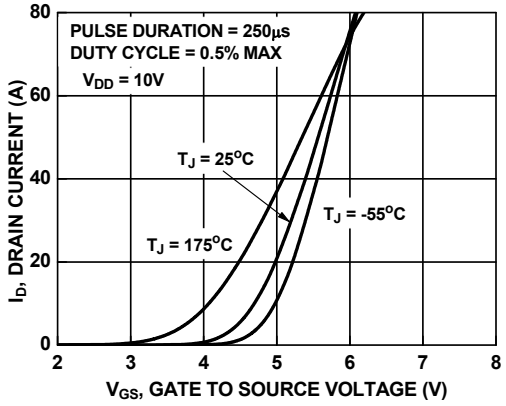


Figure 7. Transfer Characteristics

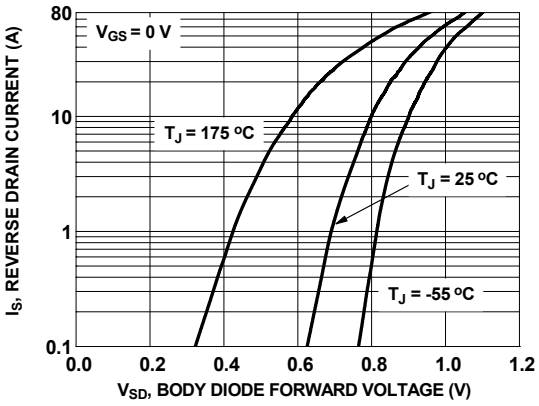


Figure 8. Forward Diode Characteristics

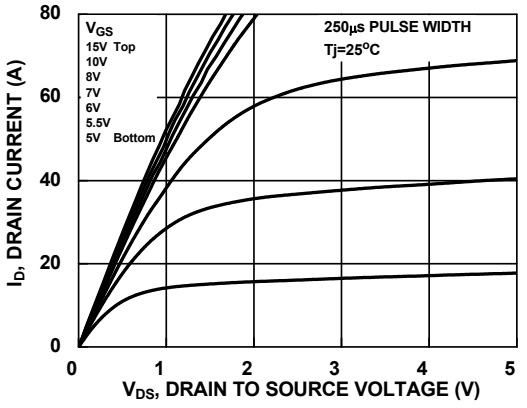


Figure 9. Saturation Characteristics

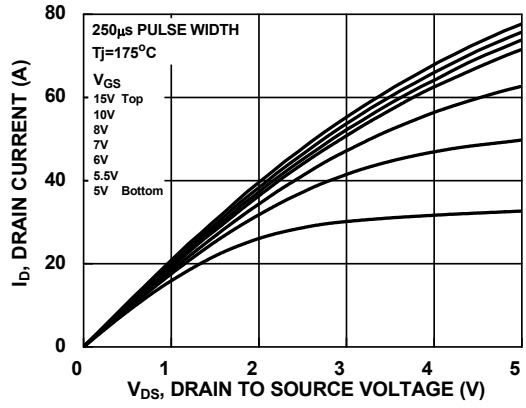


Figure 10. Saturation Characteristics

Typical Characteristics

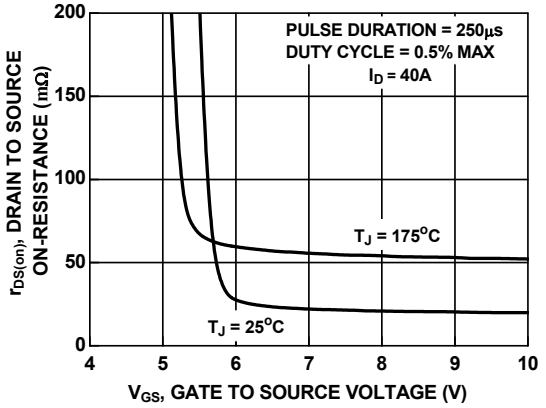


Figure 11. R_{DSON} vs. Gate Voltage

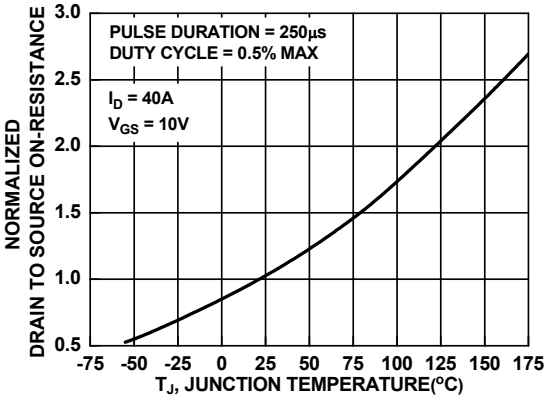


Figure 12. Normalized R_{DSON} vs. Junction Temperature

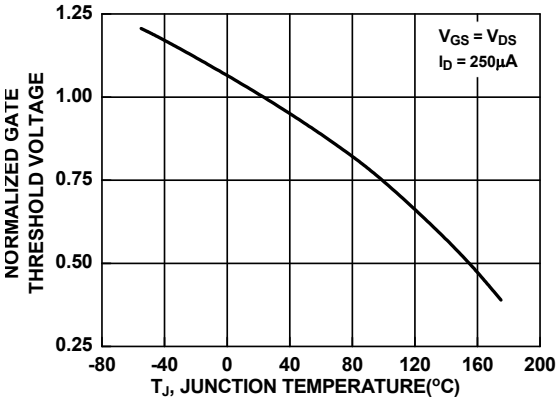


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

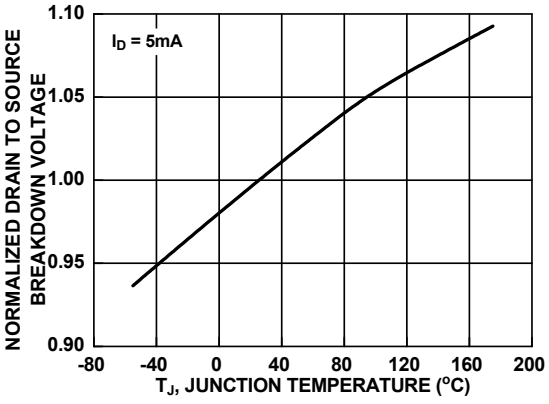


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

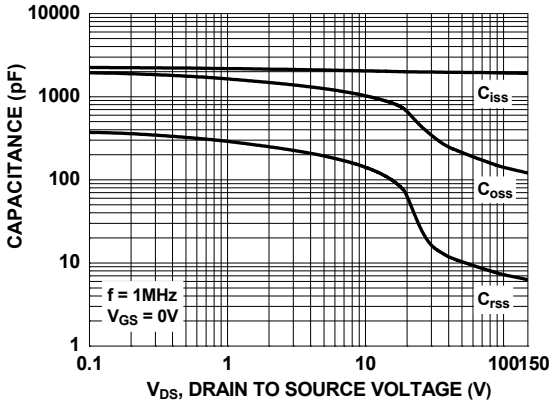


Figure 15. Capacitance vs. Drain to Source Voltage

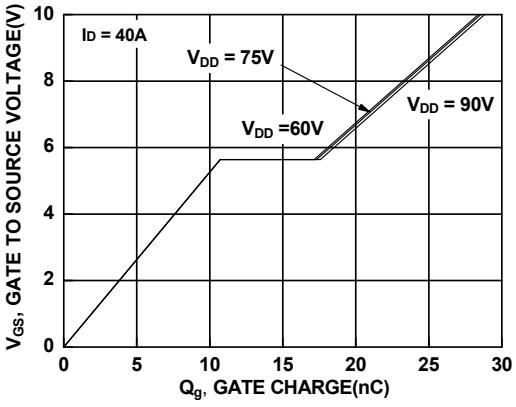
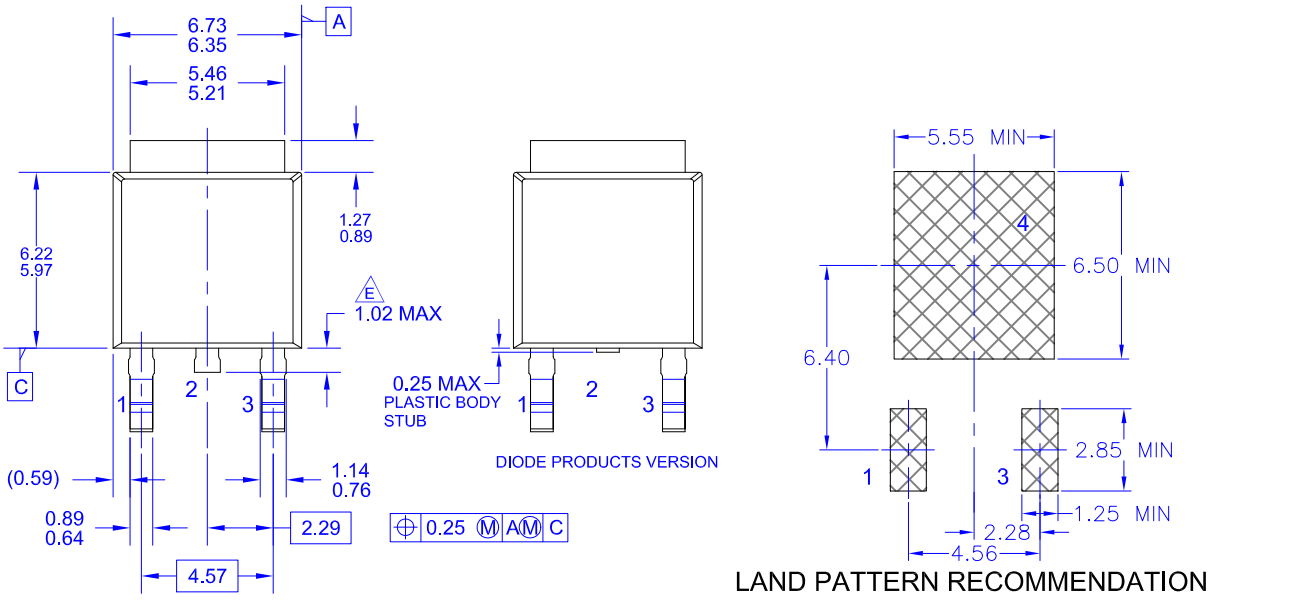
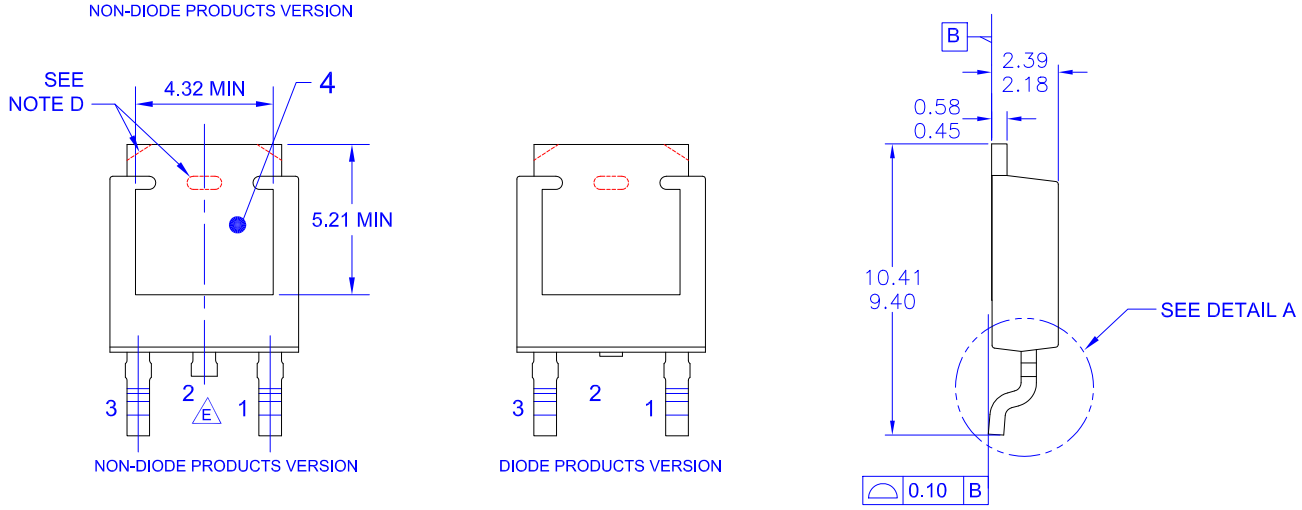


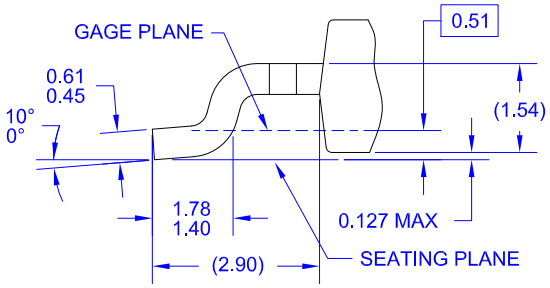
Figure 16. Gate Charge vs. Gate to Source Voltage

DPAK3 (TO−252 3 LD)
CASE 369AS
ISSUE O





NOTES: UNLESS OTHERWISE SPECIFIED
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B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
E) TRIMMED CENTER LEAD IS PRESENT ONLY FOR DIODE PRODUCTS
F) DIMENSIONS ARE EXCLUSSIVE OF BURSS, MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.



DETAIL A
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