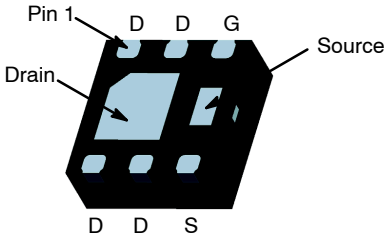
MOSFET – Single, N-Channel, POWERTRENCH®, 1.5 V Specified

20 V, 9.5 A, 23 mΩ

FDMA410NZ

V_{DS}	$R_{DS(on)}$ MAX	I_D MAX
20 V	23 mΩ @ 4.5 V	9.5 A
	29 mΩ @ 2.5 V	
	36 mΩ @ 1.8 V	
	50 mΩ @ 1.5 V	



Bottom

WDFN6 2x2, 0.65P
(MicroFET 2x2)
CASE 511CZ

General Description

This Single N-Channel MOSFET has been designed using **onsemi**'s advanced POWERTRENCH process to optimize the $R_{DS(on)}$ @ V_{GS} = 1.5 V on special MicroFET™ leadframe.

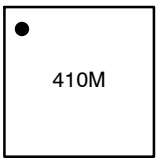
Features

- Max $R_{DS(on)}$ = 23 mΩ at V_{GS} = 4.5 V, I_D = 9.5 A
- Max $R_{DS(on)}$ = 29 mΩ at V_{GS} = 2.5 V, I_D = 8.0 A
- Max $R_{DS(on)}$ = 36 mΩ at V_{GS} = 1.8 V, I_D = 4.0 A
- Max $R_{DS(on)}$ = 50 mΩ at V_{GS} = 1.5 V, I_D = 2.0 A
- HBM ESD Protection Level > 2.5 kV (Note 3)
- Low Profile – 0.8 mm Maximum in the New Package MicroFET 2x2 mm
- Free from Halogenated Compounds and Antimony Oxides
- This Device is Pb-Free, Halide Free and is RoHS Compliant

Applications

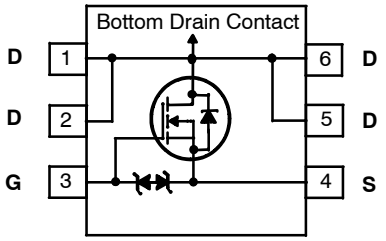
- Li-Ion Battery Pack
- Baseband Switch
- Load Switch
- DC-DC Conversion

MARKING DIAGRAM



410 = Specific Device Code
M = Month Code

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DS}	Drain to Source Voltage	20	V
V_{GS}	Gate to Source Voltage	±8	V
I_D	Drain Current – Continuous (Note 1a) – Pulsed	 9.5 24	A
P_D	Power Dissipation – (Note 1a) – (Note 1b)	 2.4 0.9	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ORDERING INFORMATION

Device	Package	Shipping†
FDMA410NZ	WDFN6 (Pb-Free, Halide Free)	3000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	52	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	145	

ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise noted)

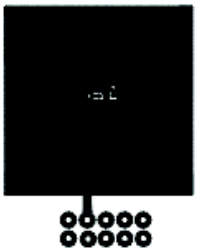
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		17		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±8 V, V_{DS} = 0 V			±10	μA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	0.4	0.7	1.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		–3		mV/°C
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 4.5 V, I_D = 9.5 A		17	23	mΩ
		V_{GS} = 2.5 V, I_D = 8.0 A		20	29	
		V_{GS} = 1.8 V, I_D = 4.0 A		24	36	
		V_{GS} = 1.5 V, I_D = 2.0 A		29	50	
		V_{GS} = 4.5 V, I_D = 9.5 A, T_J = 125 °C		23	32	
g_{FS}	Forward Transconductance	V_{DD} = 5 V, I_D = 9.5 A		35		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz		815	1080	pF
C_{oss}	Output Capacitance			130	175	pF
C_{rss}	Reverse Transfer Capacitance			85	130	pF
R_g	Gate Resistance	f = 1 MHz		2.1		Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 10 V, I_D = 9.5 A, V_{GS} = 4.5 V, R_{GEN} = 6 Ω		7.5	15	ns
t_r	Rise Times			3.9	10	ns
$t_{d(off)}$	Turn-Off Delay Time			27	44	ns
t_f	Fall Time			3.7	10	ns
Q_g	Total Gate Charge	V_{DD} = 10 V, I_D = 9.5 A, V_{GS} = 4.5 V		10	14	nC
Q_{gs}	Gate to Source Charge			1.2		nC
Q_{gd}	Gate to Drain “Miller” Charge			2.0		nC
DRAIN-SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuous Drain–Source Diode Forward Current				2.0	A
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.0 A (Note 2)		0.7	1.2	V
t_{rr}	Reverse Recovery Time	I_F = 9.5 A, di/dt = 100 A/μs		12	22	ns
Q_{rr}	Reverse Recovery Charge			2.6	10	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

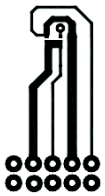
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NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a.) 52 °C/W when mounted
on a 1 in^2 pad of 2 oz copper



b.) 145 °C/W when mounted
on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

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TYPICAL CHARACTERISTICS

(T_J = 25 °C unless otherwise noted)

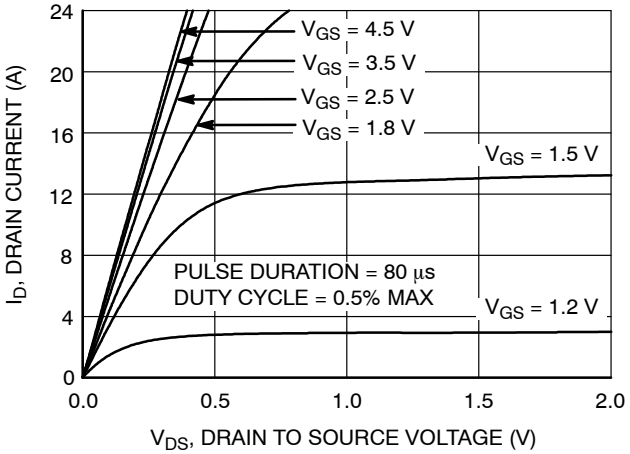


Figure 1. On-Region Characteristics

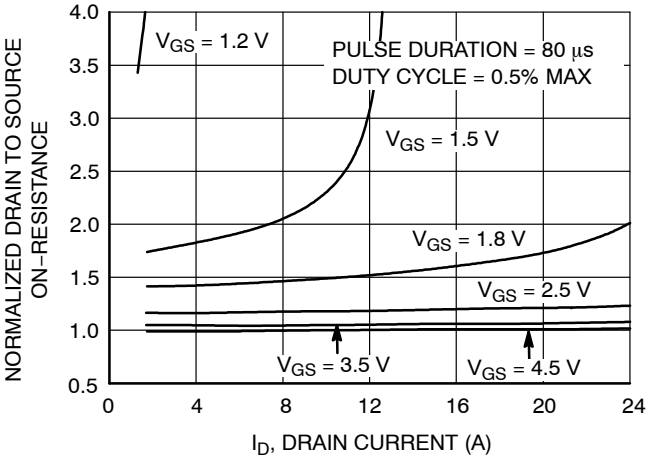


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

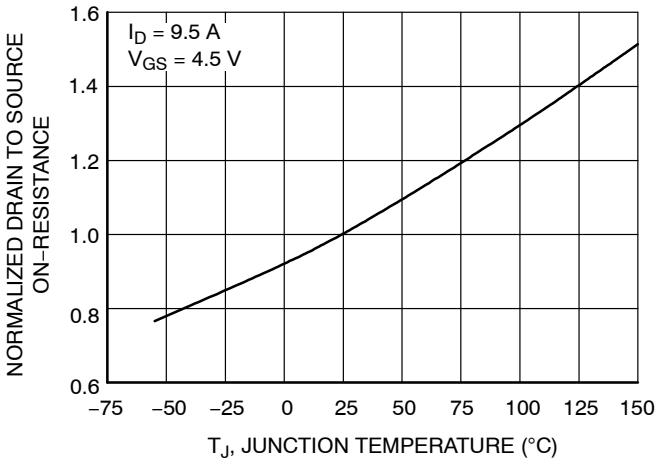


Figure 3. Normalized On-Resistance vs. Junction Temperature

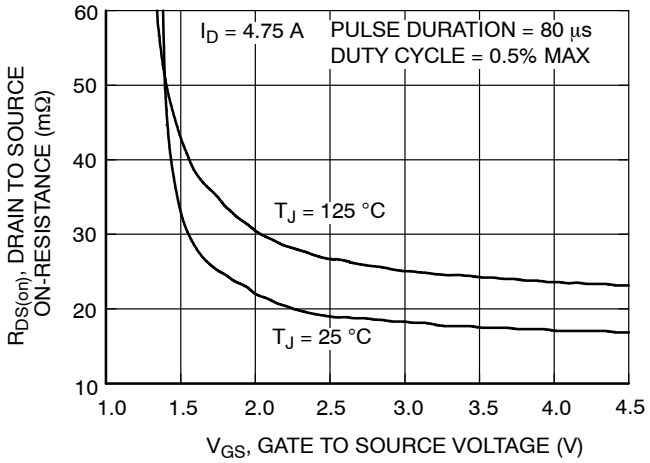


Figure 4. On-Resistance vs. Gate to Source Voltage

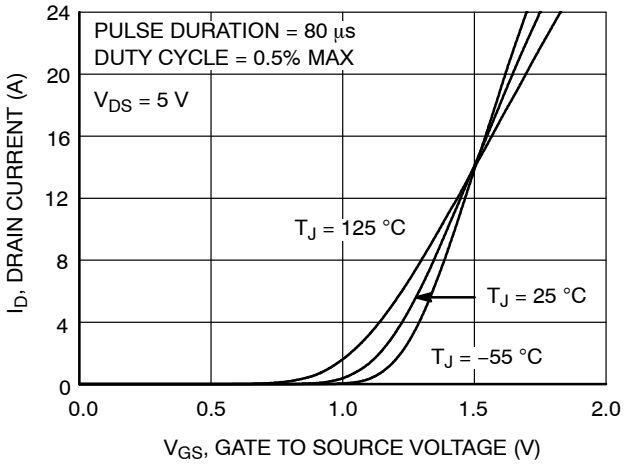


Figure 5. Transfer Characteristics

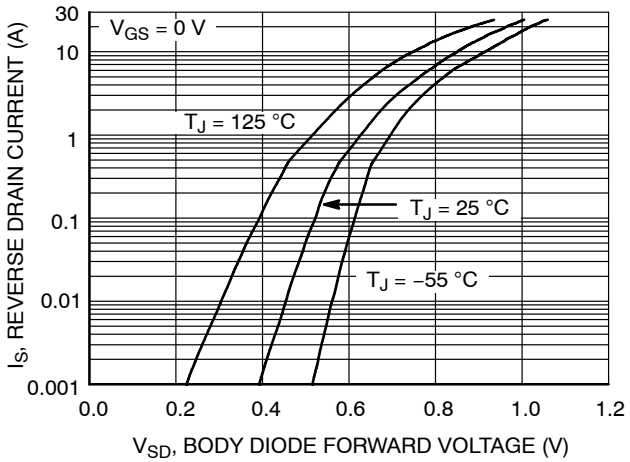


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

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TYPICAL CHARACTERISTICS (continued)

(T_J = 25 °C unless otherwise noted)

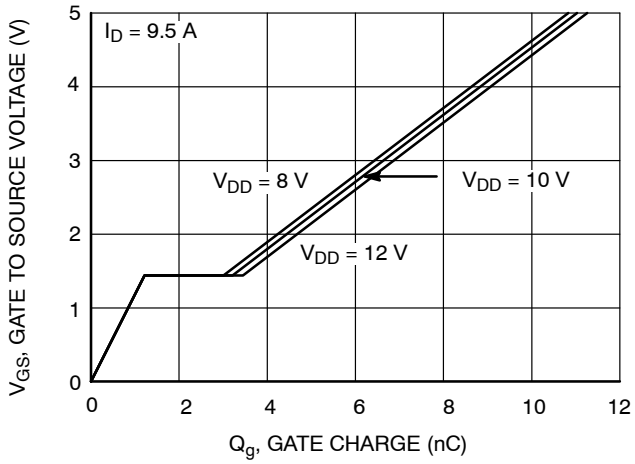


Figure 7. Gate Charge Characteristics

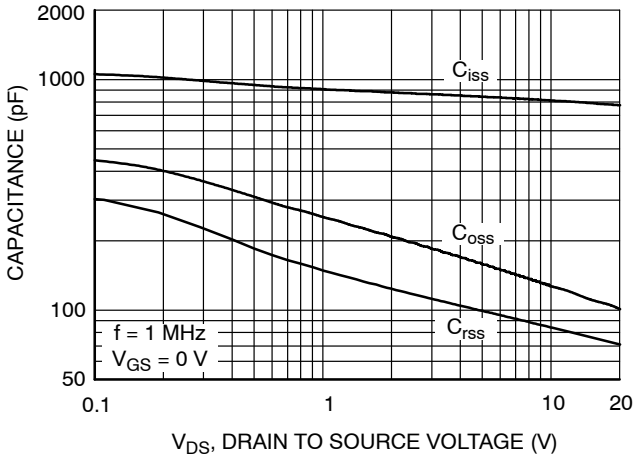


Figure 8. Capacitance vs. Drain to Source Voltage

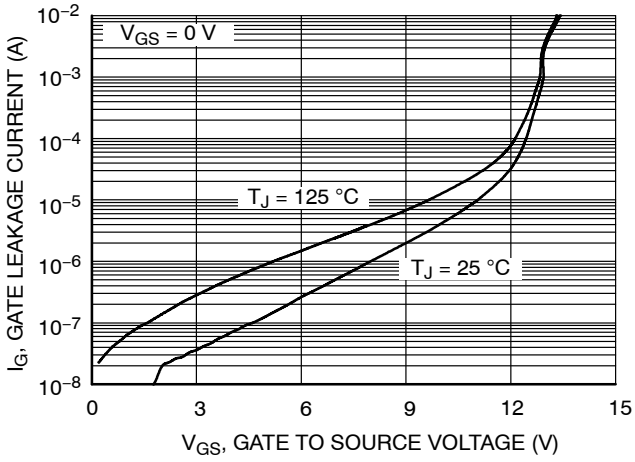


Figure 9. Gate Leakage Current vs. Gate to Source Voltage

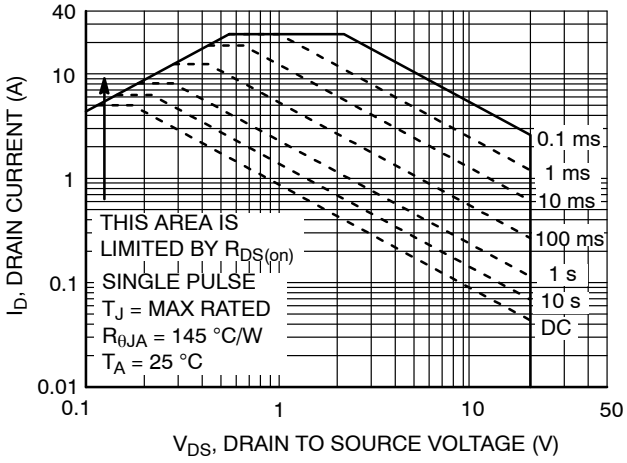


Figure 10. Forward Bias Safe Operating Area

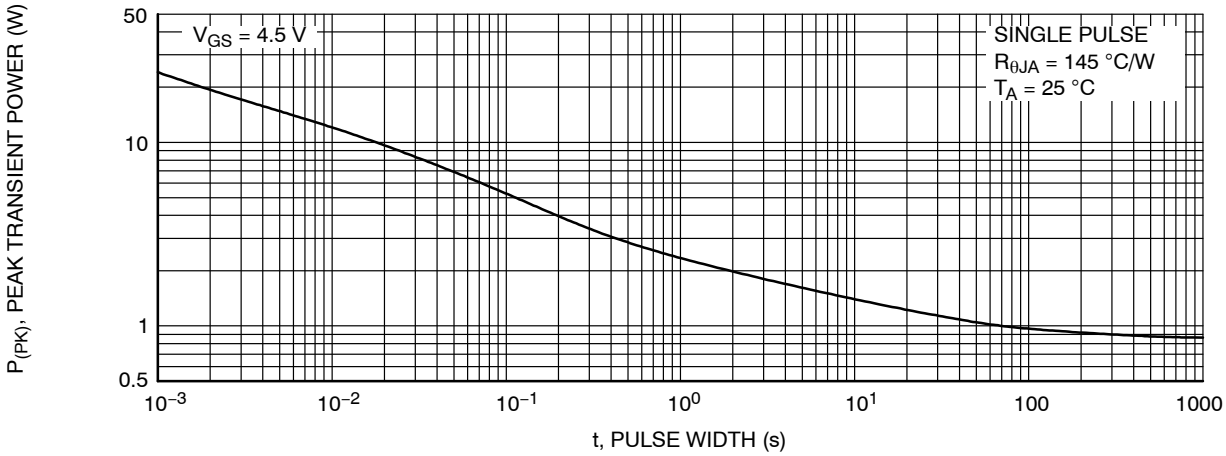


Figure 11. Single Pulse Maximum Power Dissipation

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TYPICAL CHARACTERISTICS (continued)

(T_J = 25°C unless otherwise noted)

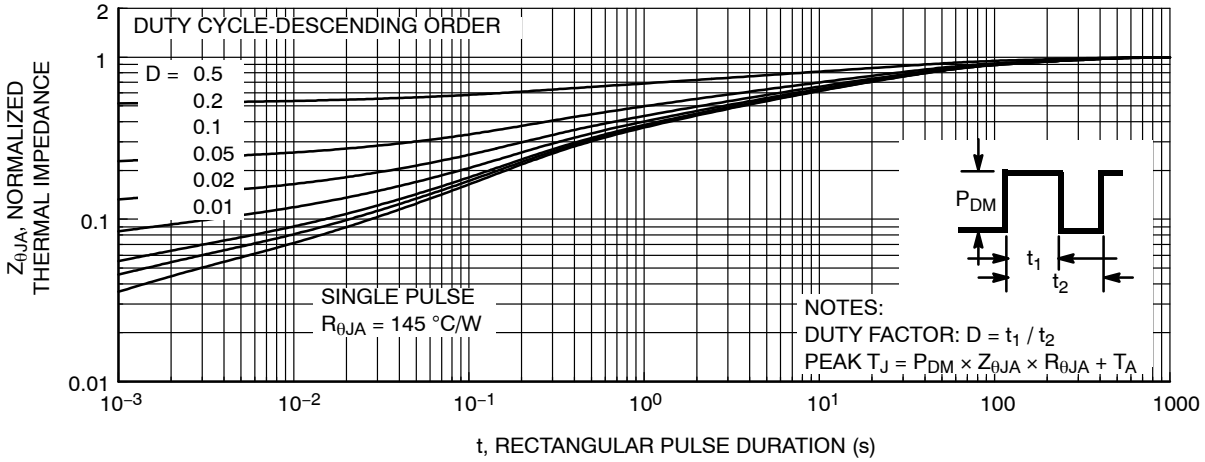


Figure 12. Junction-to-Ambient Transient Thermal Response Curve

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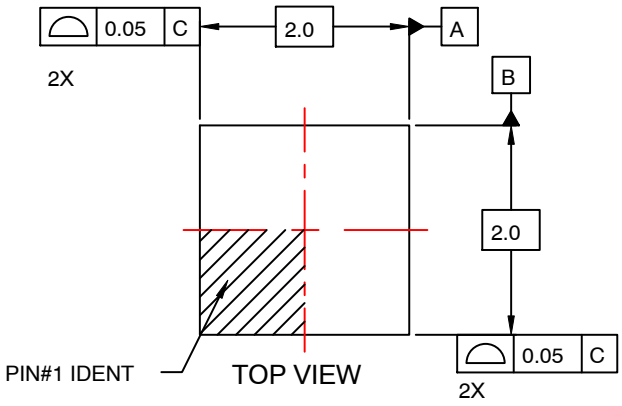
Revision	Description of Changes	Date
3	Marking Diagram update.	11/5/2026

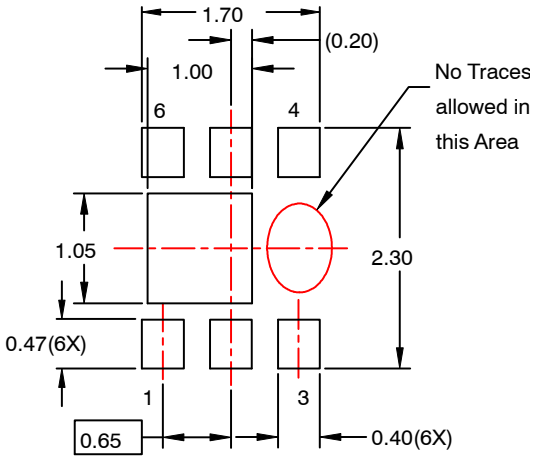
This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

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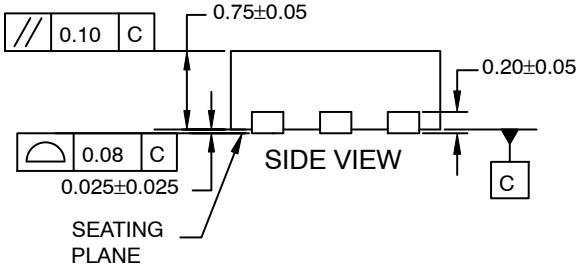
WDFN6 2x2, 0.65P
CASE 511CZ
ISSUE O

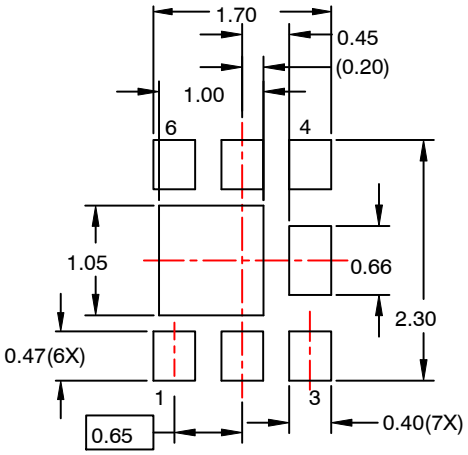
DATE 31 JUL 2016



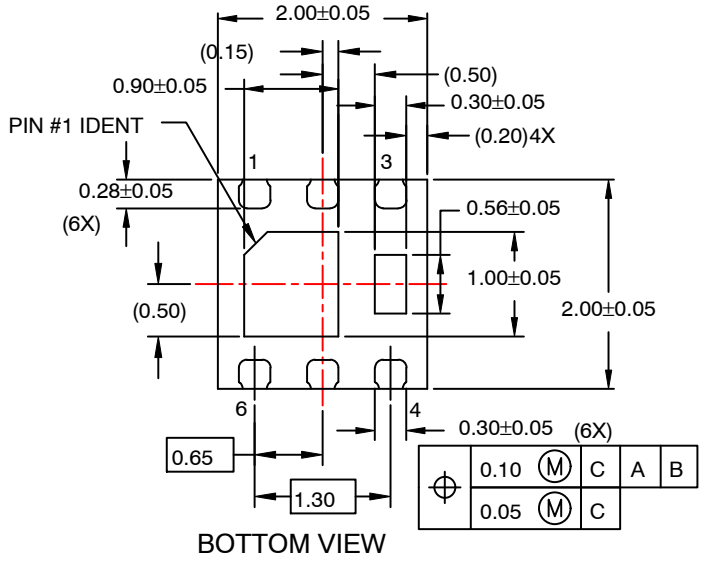


RECOMMENDED
LAND PATTERN OPT 1





RECOMMENDED
LAND PATTERN OPT 2



NOTES:

A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC MO−229 REGISTRATION

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

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DESCRIPTION:	**WDFN6 2X2, 0.65P**		**PAGE 1 OF 1**

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