MOSFET – Single, P-Channel, POWERTRENCH®

-20 V, -7.8 A, 24 mΩ

FDMA507PZ

V_{S1S2}	$r_{S1S2(on)}$ MAX	I_{S1S2} MAX
−20 V	24 mΩ @ −5 V	−7.8 A
	25 mΩ @ −4.5 V	
	35 mΩ @ −2.5 V	
	45 mΩ @ −1.8 V	

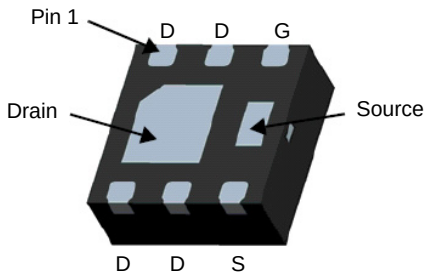
General Description

This device is designed specifically for battery charge or load switching in cellular handset and other ultraportable applications. It features a MOSFET with low on−stade resistance.

The MicroFET ™ 2x2 package offers exceptional thermal perfomance for its physical size and is well suited to linear mode applications.

Features

- Max $r_{DS(on)}$ = 24 mΩ at V_{GS} = −5 V, I_D = −7.8 A
- Max $r_{DS(on)}$ = 25 mΩ at V_{GS} = −4.5 V, I_D = −7 A
- Max $r_{DS(on)}$ = 35 mΩ at V_{GS} = −2.5 V, I_D = −5.5 A
- Max $r_{DS(on)}$ = 45 mΩ at V_{GS} = −1.8 V, I_D = −4 A
- Low Profile − 0.8 mm Maximum − in the Package MicroFET ™ 2x2 mm
- HBM ESD Protection Level > 3.2 kV Typical (Note 3)
- Free from Halogenated Compounds and Antimony Oxides
- This Device is Pb−Free, Halide Free and is RoHS Compliant



Bottom View

WDFN6 2x2, 0.65P
(MicroFET 2x2)
CASE 511DB

MOSFET MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

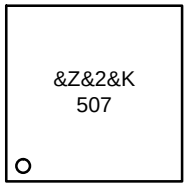
Symbol	Parameter	Ratings	Unit
V_{DS}	Drain to Source Voltage	−20	V
V_{GS}	Gate to Source Voltage	±8	V
I_D	Drain Current −Continuous T_A = 25°C (Note 1a) −Pulsed	 −7.8 −24	A
P_D	Power Dissipation T_A = 25°C (Note 1a) T_A = 25°C (Note 1b)	 2.4 0.9	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted)

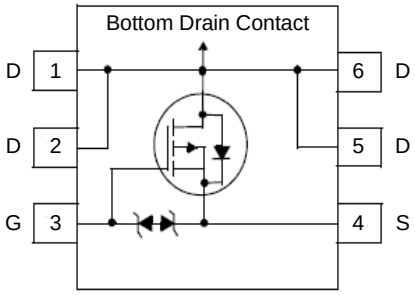
Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	52	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	145	

MARKING DIAGRAM



&Z = Assembly Plant Code
&2 = 2−Digit Date Code
&K = 2−Digits Lot Run Traceability Code
507 = Specific Device Code

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

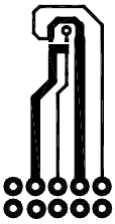
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = −250 μA, V_{GS} = 0 V	−20	−	−	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = −250 μA, referenced to 25°C	−	−12	−	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = −16 V, V_{GS} = 0 V	−	−	−1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±8 V, V_{DS} = 0 V	−	−	±10	μA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = −250 μA	−0.4	−0.5	−1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = −250 μA, referenced to 25°C	−	3	−	mV/°C
$r_{DS(on)}$	Drain to Source On Resistance	V_{GS} = −5 V, I_D = −7.8 A	−	19	24	mΩ
		V_{GS} = −4.5 V, I_D = −7 A	−	20	25	
		V_{GS} = −2.5 V, I_D = −5.5 A	−	24	35	
		V_{GS} = −1.8 V, I_D = −4 A	−	29	45	
		V_{GS} = −5 V, I_D = −7.8 A, T_J = 125°C	−	26	34	
g_{FS}	Forward Transconductance	V_{DS} = −5 V, I_D = −7.8 A	−	33	−	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = −10 V, V_{GS} = 0 V, f = 1 MHz	−	1515	2015	pF
C_{oss}	Output Capacitance		−	265	355	pF
C_{rss}	Reverse Transfer Capacitance		−	240	360	pF
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = −10 V, I_D = −7.8 A V_{GS} = −5 V, R_{GEN} = 6 Ω	−	6.4	13	ns
t_r	Rise Time		−	14	25	ns
$t_{d(off)}$	Turn−Off Delay Time		−	192	307	ns
t_f	Fall Time		−	96	154	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{DD} = −10 V, I_D = −7.8 A V_{GS} = −5 V	−	30	42	nC
Q_{gs}	Gate to Source Gate Charge		−	2	−	nC
Q_{gd}	Gate to Drain “Miller” Charge		−	7.5	−	nC
DRAIN−SOURCE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = −2.0 A (Note 2)	−	−0.6	−1.2	V
t_{rr}	Reverse Recovery Time	I_F = −7.8 A, di/dt = 100 A/μs	−	66	106	ns
Q_{rr}	Reverse Recovery Charge		−	44	70	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user’s board design.



a. 52°C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 145°C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

TYPICAL CHARACTERISTICS (T_J = 25°C, unless otherwise noted)

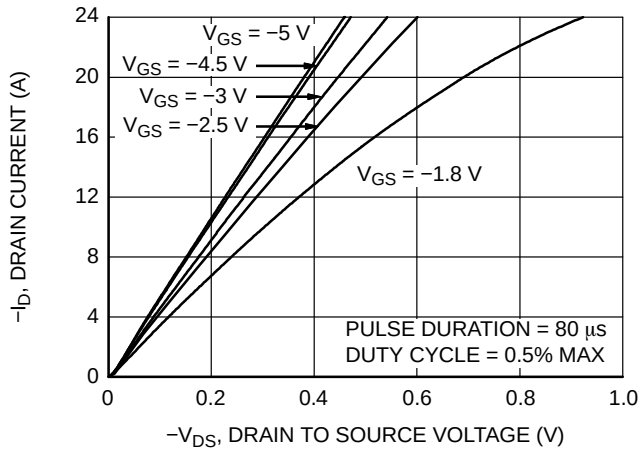


Figure 1. On Region Characteristics

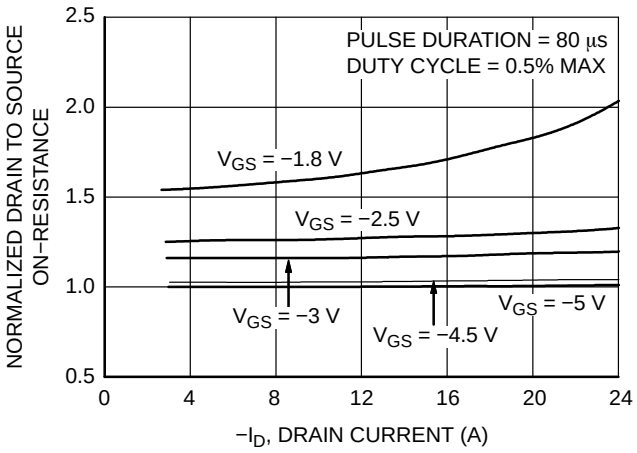


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

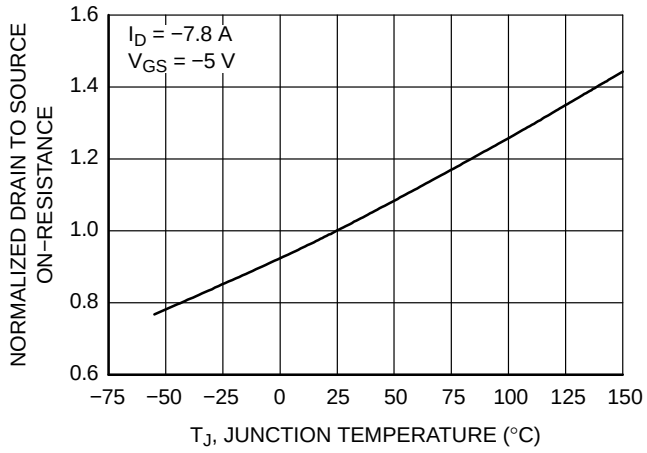


Figure 3. Normalized On Resistance vs. Junction Temperature

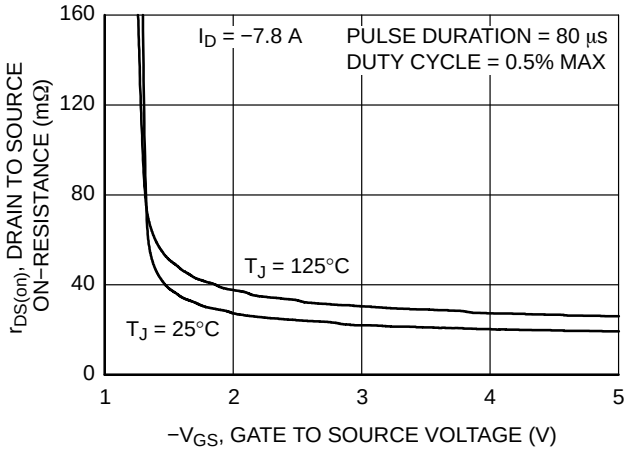


Figure 4. On−Resistance vs. Gate to Source Voltage

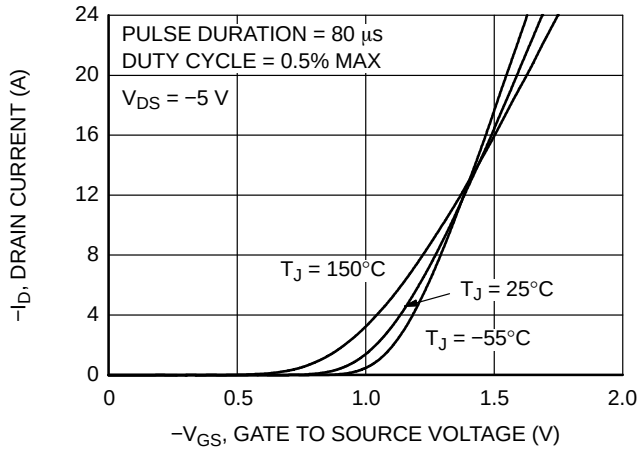


Figure 5. Transfer Characteristics

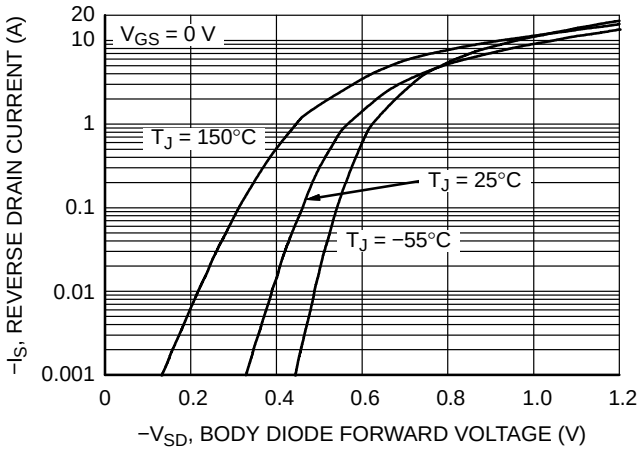


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (T_J = 25°C, unless otherwise noted) (continued)

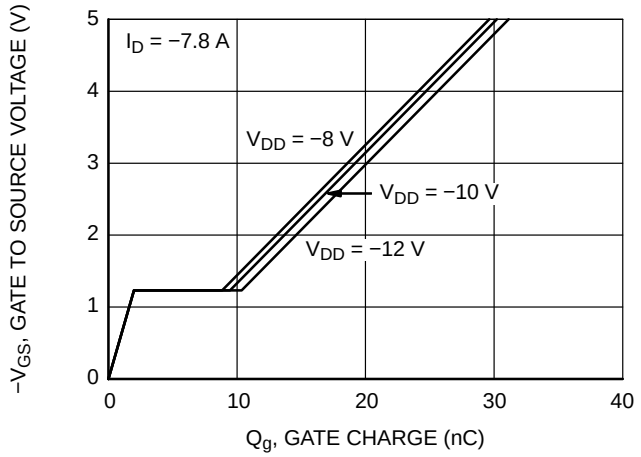


Figure 7. Gate Charge Characteristics

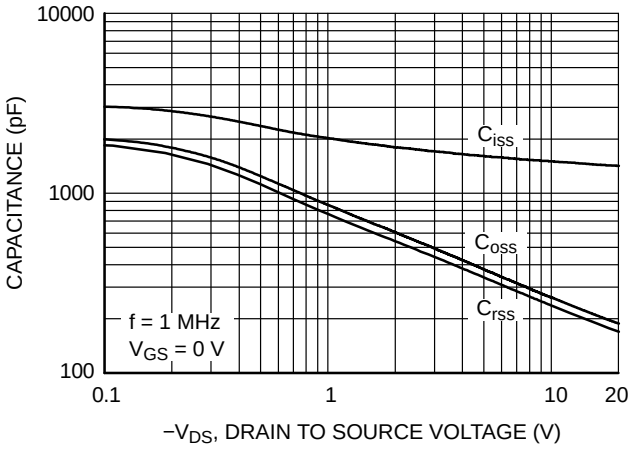


Figure 8. Capacitance vs. Drain to Source Voltage

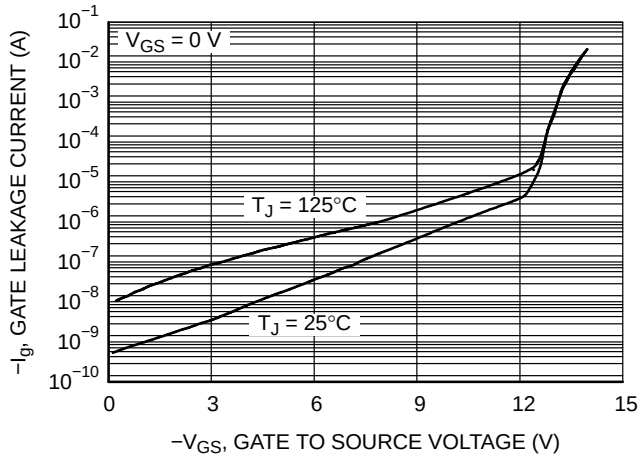


Figure 9. Gate Leakage Current vs. Gate to Source Voltage

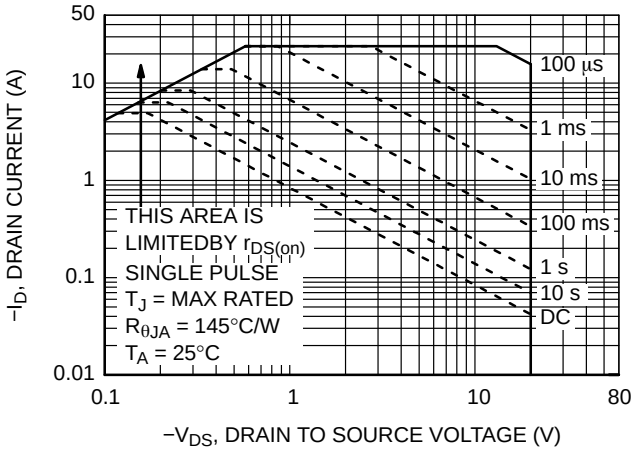


Figure 10. Forward Bias Safe Operating Area

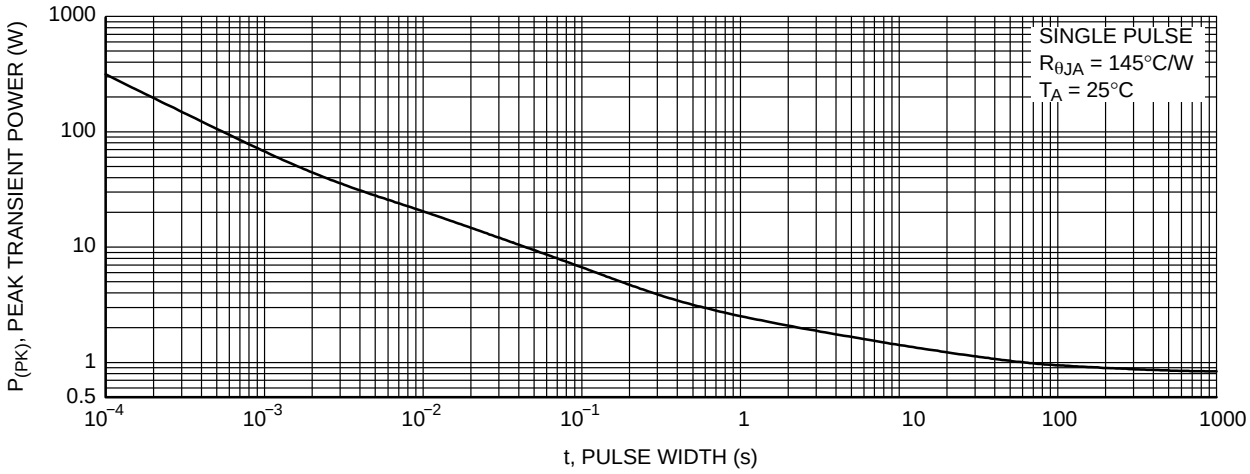


Figure 11. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (T_J = 25°C, unless otherwise noted) (continued)

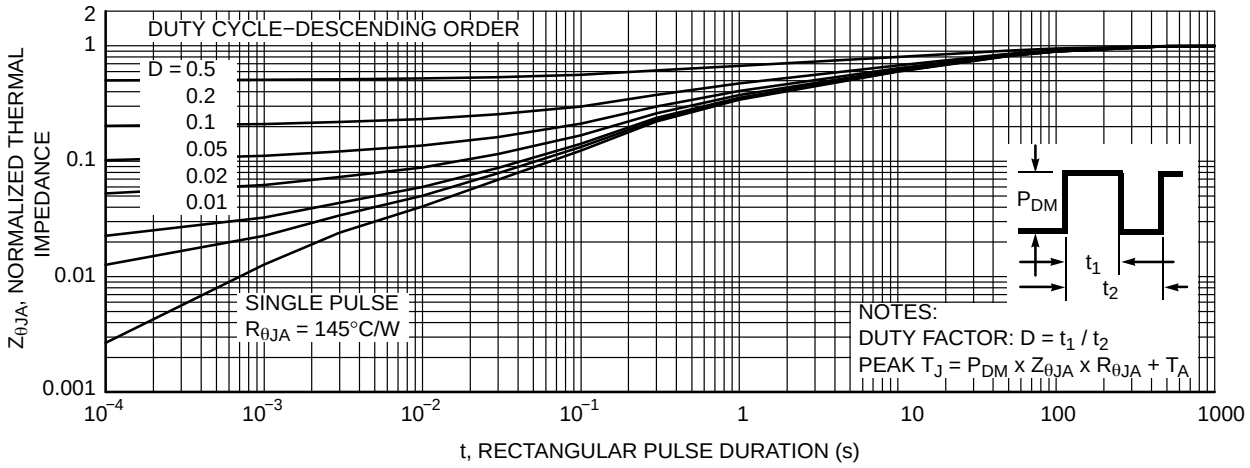


Figure 12. Junction−to−Ambient Transient Thermal Response Curve

PACKAGE MARKING AND ORDERING INFORMATION

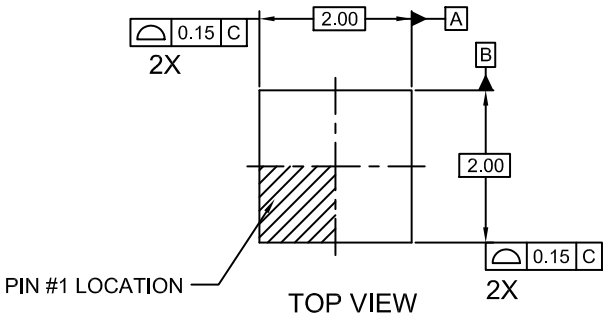
Device	Device Marking	Package	Reel Size	Tape Width	Shipping†
FDMA507PZ	507	WDFN6 2x2, 0.65P (MicroFET 2x2) (Pb−Free, Halide Free)	7”	12 mm	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

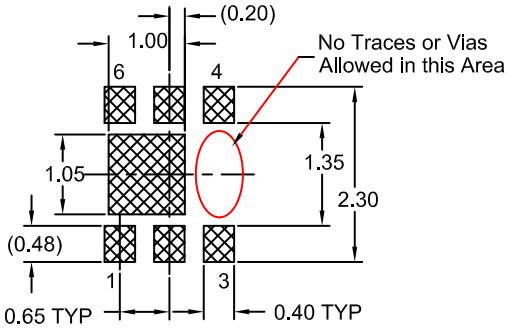
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WDFN6 2x2, 0.65P
CASE 511DB
ISSUE O

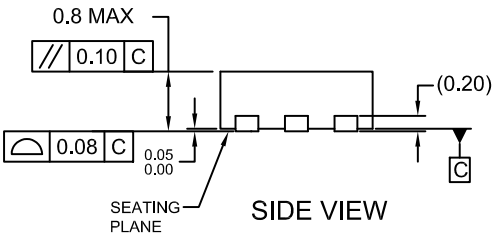
DATE 31 AUG 2016



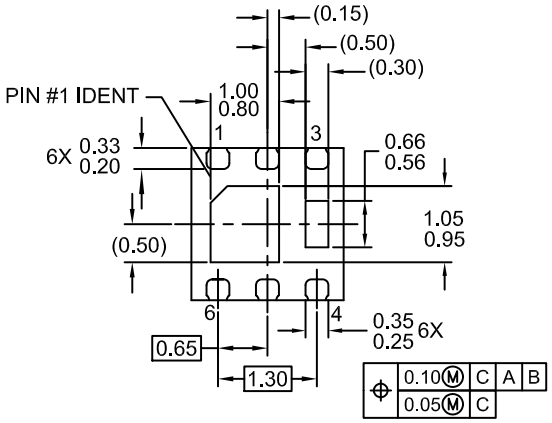
TOP VIEW



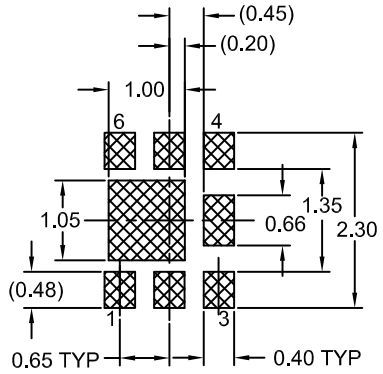
RECOMMENDED LAND PATTERN OPT 1



SIDE VIEW



BOTTOM VIEW



RECOMMENDED LAND PATTERN OPT 2

NOTES:

A. DOES NOT FULLY CONFORM TO JEDEC REGISTRATION
MO-229 DATED AUG/2003
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER
ASME Y14.5M, 1994

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