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FAIRCHILD SEMICONDUCTOR®

December 2011

FDMS3622S

PowerTrench® Power Stage

25V Asymmetric Dual N-Channel MOSFET

Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 5.0 mΩ at V_{GS} = 10 V, I_D = 17.5 A
- Max $r_{DS(on)}$ = 5.7 mΩ at V_{GS} = 4.5 V, I_D = 16 A

Q2: N-Channel

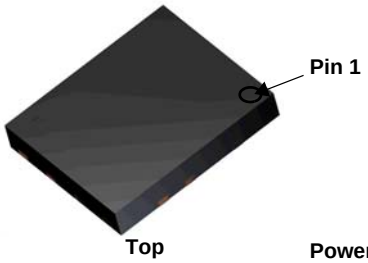
- Max $r_{DS(on)}$ = 1.4 mΩ at V_{GS} = 10 V, I_D = 34 A
- Max $r_{DS(on)}$ = 1.6 mΩ at V_{GS} = 4.5 V, I_D = 32 A
- Low inductance packaging shortens rise/fall times, resulting in lower switching losses
- MOSFET integration enables optimum layout for lower circuit inductance and reduced switch node ringing
- RoHS Compliant

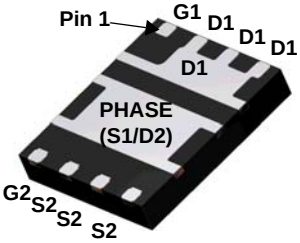
General Description

This device includes two specialized N-Channel MOSFETs in a dual PQFN package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous SyncFET (Q2) have been designed to provide optimal power efficiency.

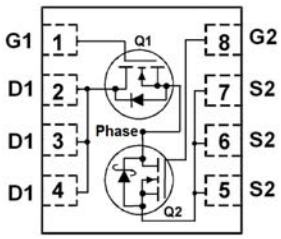
Applications

- Computing
- Communications
- General Purpose Point of Load
- Notebook VCORE





Power 56



MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter		Q1	Q2	Units
V_{DS}	Drain to Source Voltage		25	25	V
V_{GS}	Gate to Source Voltage	(Note 4)	±12	±12	V
I_D	Drain Current -Continuous (Package limited)	T_C = 25 °C	30	70	A
	-Continuous	T_A = 25 °C	17.5[1a]	34[1b]	
	-Pulsed		70	140	
E_{AS}	Single Pulse Avalanche Energy	(Note 3)	29	145	mJ
P_D	Power Dissipation for Single Operation	T_A = 25 °C	2.2[1a]	2.5[1b]	W
	Power Dissipation for Single Operation	T_A = 25 °C	1.0[1c]	1.0[1d]	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150		°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	57[1a]	50[1b]	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	125[1c]	120[1d]	
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.0	1.9	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
08OD 09OD	FDMS3622S	Power 56	13 ”	12 mm	3000 units

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Electrical Characteristics T_J = 25 °C unless otherwise noted

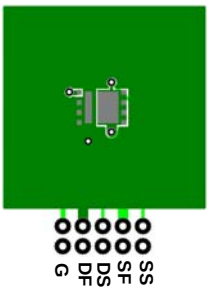
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Off Characteristics							
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V I_D = 1 mA, V_{GS} = 0 V	Q1 Q2	25 25			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C I_D = 10 mA, referenced to 25 °C	Q1 Q2		12 24		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 20 V, V_{GS} = 0 V	Q1 Q2			1 500	μA μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = 12 V/-8 V, V_{DS}= 0 V	Q1 Q2			±100 ±100	nA nA
On Characteristics							
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA V_{GS} = V_{DS}, I_D = 1 mA	Q1 Q2	0.8 1.1	1.2 1.4	2.0 2.2	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C I_D = 10 mA, referenced to 25 °C	Q1 Q2		-4 -4		mV/°C
$r_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 10 V, I_D = 17.5 A V_{GS} = 4.5 V, I_D = 16 A V_{GS} = 10 V, I_D = 17.5 A,T_J =125 °C	Q1		3.8 4.4 5.4	5.0 5.7 7.0	mΩ
		V_{GS} = 10 V, I_D = 34 A V_{GS} = 4.5 V, I_D = 32 A V_{GS} = 10 V, I_D =34 A ,T_J =125 °C	Q2		1.1 1.3 1.5	1.4 1.6 2.0	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 17.5 A V_{DS} = 5 V, I_D = 34 A	Q1 Q2		100 272		S
Dynamic Characteristics							
C_{iss}	Input Capacitance	Q1: V_{DS} = 13 V, V_{GS} = 0 V, f = 1 MHZ	Q1 Q2		1570 5565		pF
C_{oss}	Output Capacitance	Q2: V_{DS} = 13 V, V_{GS} = 0 V, f = 1 MHZ	Q1 Q2		448 1405		pF
C_{rss}	Reverse Transfer Capacitance		Q1 Q2		61 182		pF
R_g	Gate Resistance		Q1 Q2		0.4 0.8		Ω
Switching Characteristics							
$t_{d(on)}$	Turn-On Delay Time	Q1: V_{DD} = 13 V, I_D = 17.5 A, R_{GEN} = 6 Ω Q2: V_{DD} = 13 V, I_D = 34 A, R_{GEN} = 6 Ω	Q1 Q2		7 14		ns
t_r	Rise Time		Q1 Q2		2 7		ns
$t_{d(off)}$	Turn-Off Delay Time		Q1 Q2		23 48		ns
t_f	Fall Time		Q1 Q2		2 6		ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V; Q1 V_{DD} = 13 V, I_D = 17.5 A	Q1 Q2		26 86		nC
Q_g	Total Gate Charge	V_{GS} = 0 V to 4.5 V; Q1 V_{DD} = 13 V, I_D = 17.5 A	Q1 Q2		12 40		nC
Q_{gs}	Gate to Source Gate Charge	Q2 V_{DD} = 13 V, I_D = 34 A	Q1 Q2		3.3 12		nC
Q_{gd}	Gate to Drain “Miller” Charge	Q2 V_{DD} = 13 V, I_D = 34 A	Q1 Q2		2.7 10		nC

Electrical Characteristics T_J = 25 °C unless otherwise noted

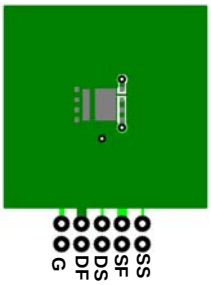
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Drain-Source Diode Characteristics							
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 17.5 A (Note 2) V_{GS} = 0 V, I_S = 34 A (Note 2)	Q1 Q2		0.8 0.8	1.2 1.2	V
t_{rr}	Reverse Recovery Time	Q1 I_F = 17.5 A, di/dt = 100 A/µs	Q1 Q2		23 35		ns
Q_{rr}	Reverse Recovery Charge	Q2 I_F = 34 A, di/dt = 300 A/µs	Q1 Q2		9 43		nC

Notes:

1.$R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 57 °C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 50 °C/W when mounted on a 1 in^2 pad of 2 oz copper



c. 125 °C/W when mounted on a minimum pad of 2 oz copper



d. 120 °C/W when mounted on a minimum pad of 2 oz copper

2 Pulse Test: Pulse Width < 300 µs, Duty cycle < 2.0%.

3. Q1 :E_{AS} of 29 mJ is based on starting T_J = 25 °C; N-ch: L = 1.2 mH, I_{AS} = 7 A, V_{DD} = 23 V, V_{GS} = 10 V. 100% test at L = 0.1 mH, I_{AS} = 16 A.
Q2: E_{AS} of 145 mJ is based on starting T_J = 25 °C; N-ch: L = 0.9 mH, I_{AS} = 18 A, V_{DD} = 23 V, V_{GS} = 10 V. 100% test at L= 0.1 mH, I_{AS} = 39 A.

4. As an N-ch device, the negative Vgs rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted

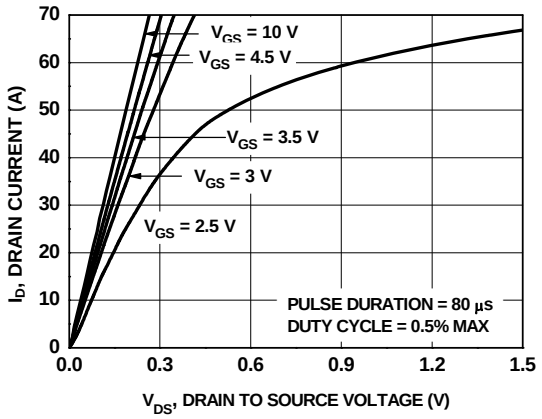


Figure 1. On Region Characteristics

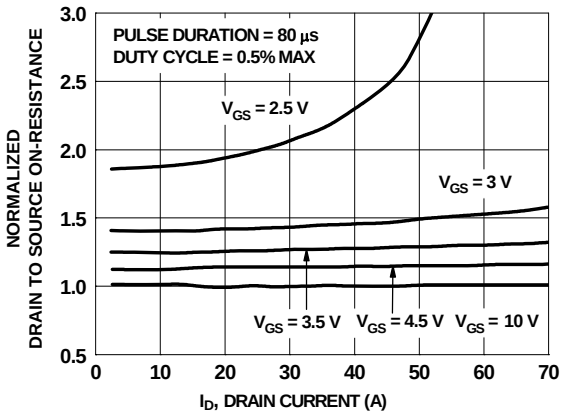


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

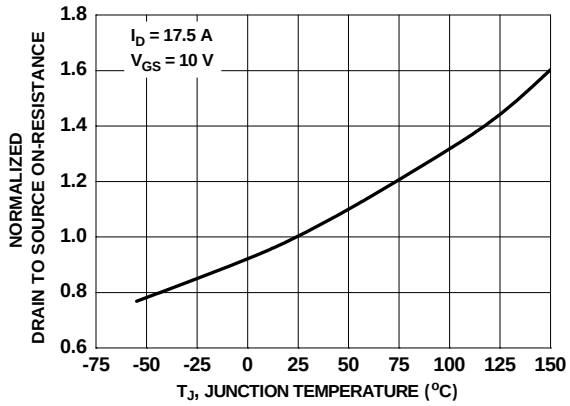


Figure 3. Normalized On Resistance vs Junction Temperature

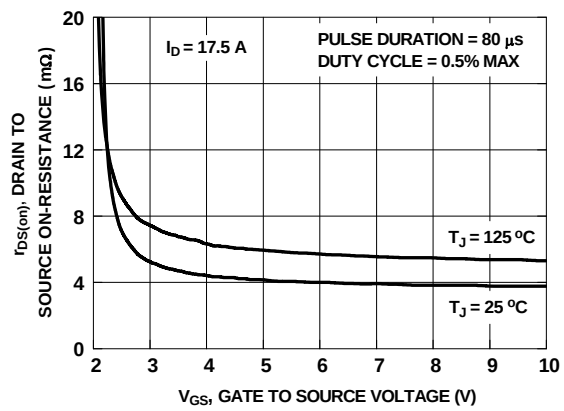


Figure 4. On-Resistance vs Gate to Source Voltage

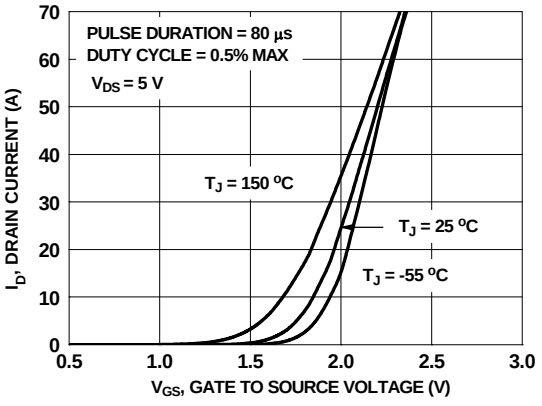


Figure 5. Transfer Characteristics

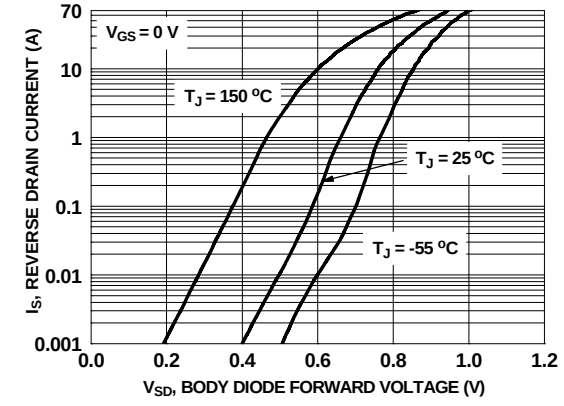


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted

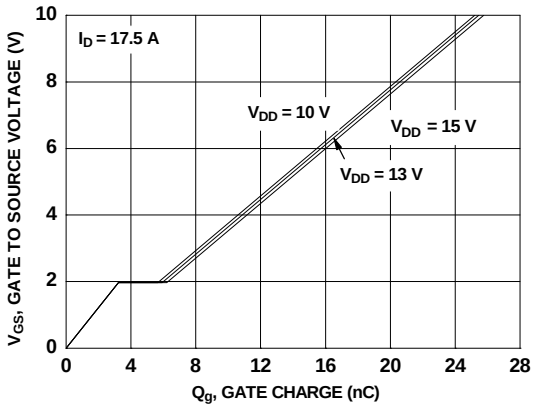


Figure 7. Gate Charge Characteristics

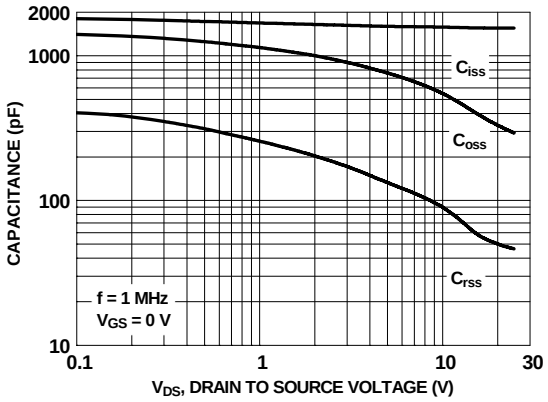


Figure 8. Capacitance vs Drain to Source Voltage

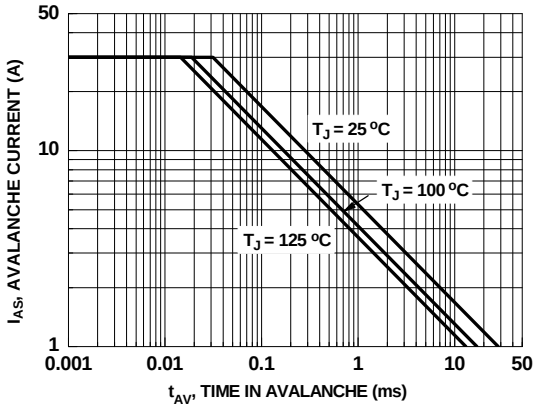


Figure 9. Unclamped Inductive Switching Capability

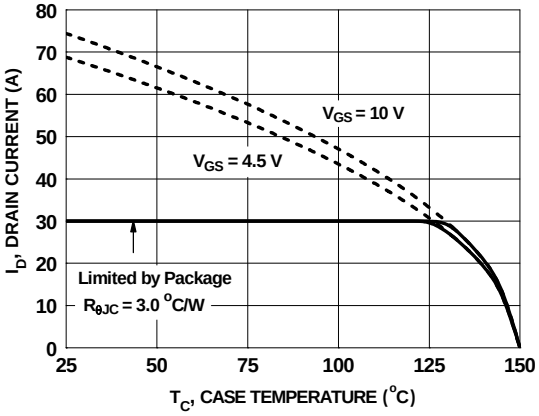


Figure 10. Maximum Continuous Drain Current vs Case Temperature

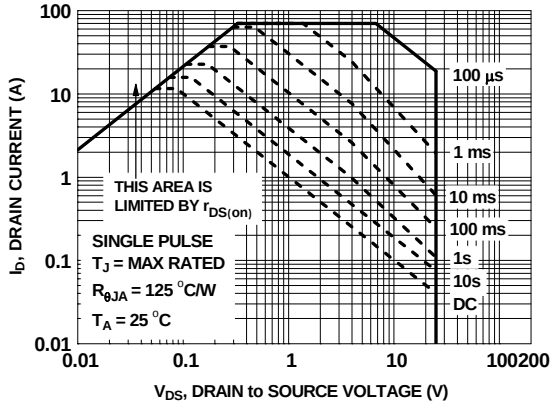


Figure 11. Forward Bias Safe Operating Area

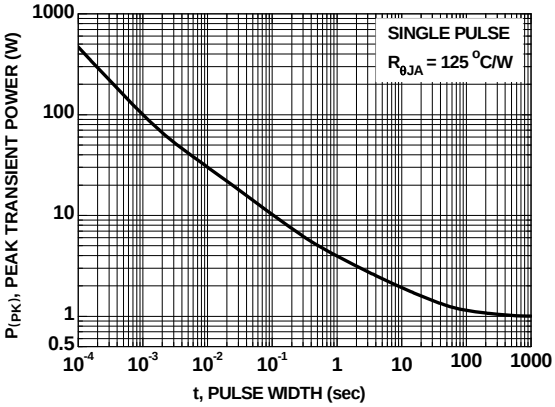


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted

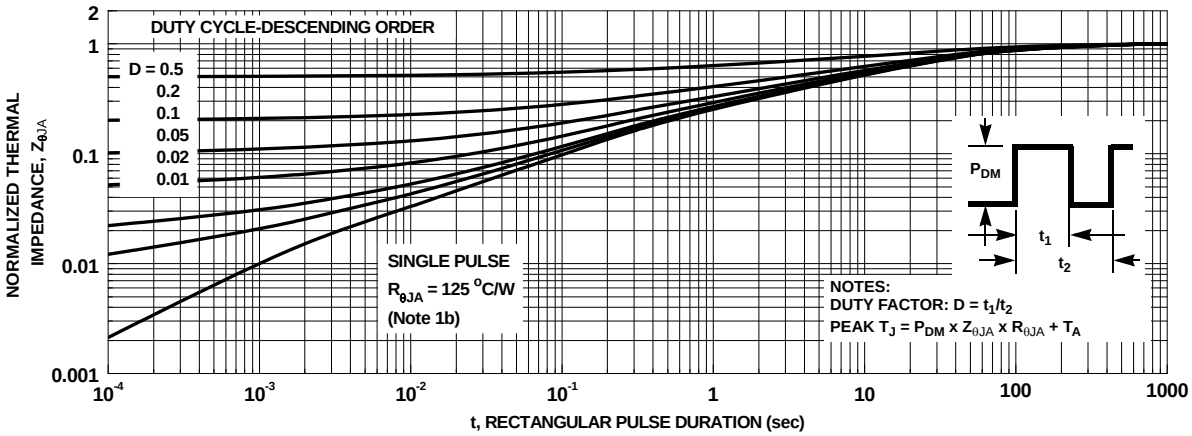


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

Typical Characteristics (Q2 N-Channel) T_J = 25 °C unless otherwise noted

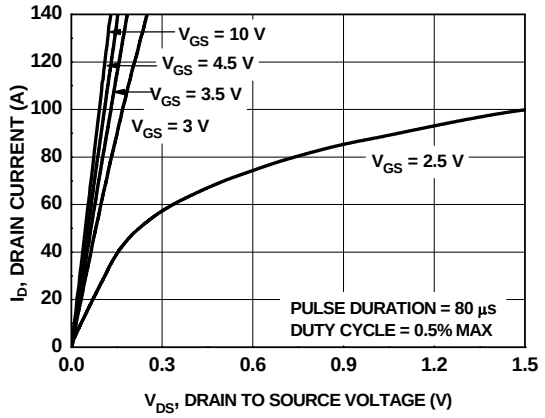


Figure 14. On-Region Characteristics

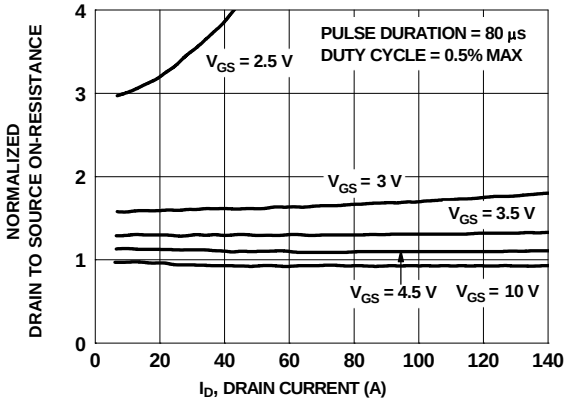


Figure 15. Normalized on-Resistance vs Drain Current and Gate Voltage

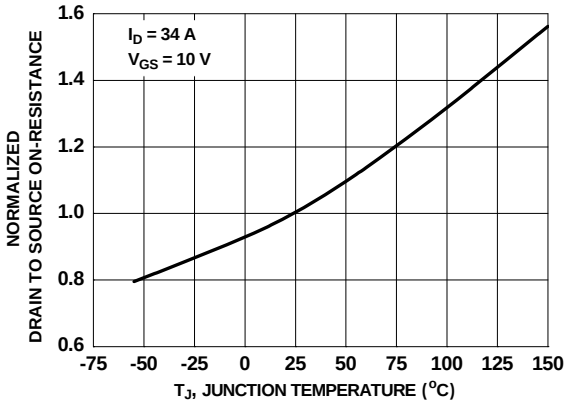


Figure 16. Normalized On-Resistance vs Junction Temperature

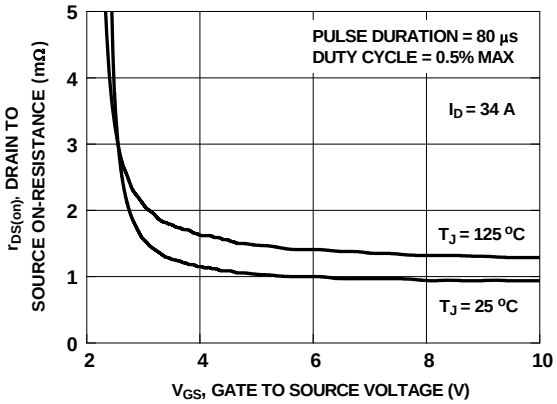


Figure 17. On-Resistance vs Gate to Source Voltage

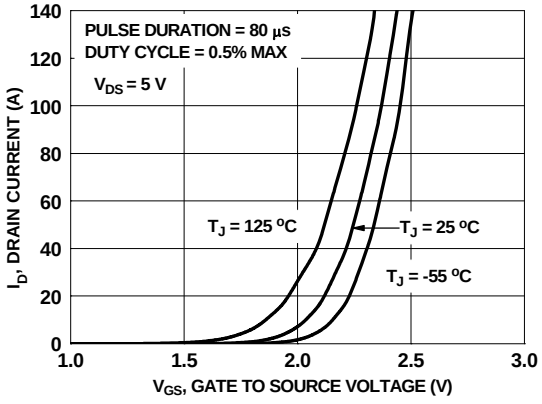


Figure 18. Transfer Characteristics

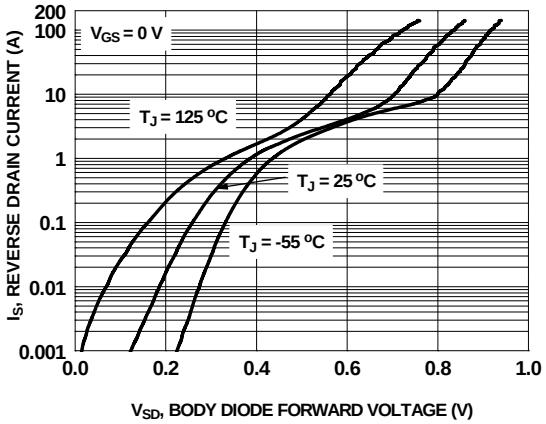


Figure 19. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q2 N-Channel) T_J = 25°C unless otherwise noted

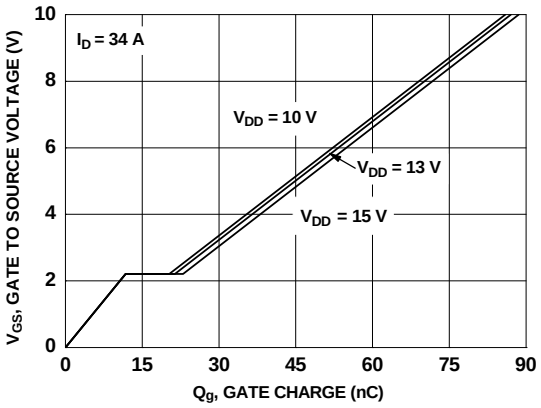


Figure 20. Gate Charge Characteristics

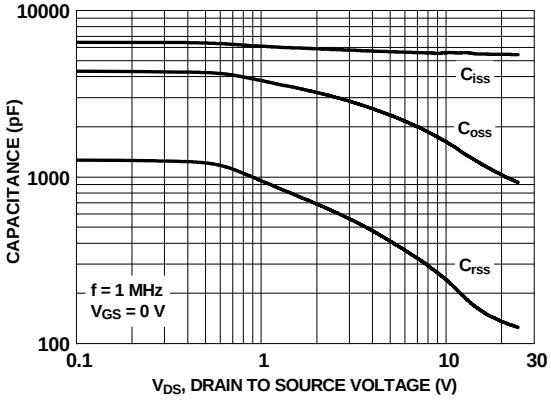


Figure 21. Capacitance vs Drain to Source Voltage

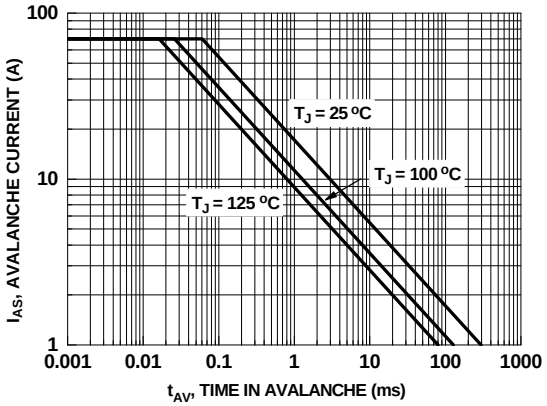


Figure 22. Unclamped Inductive Switching Capability

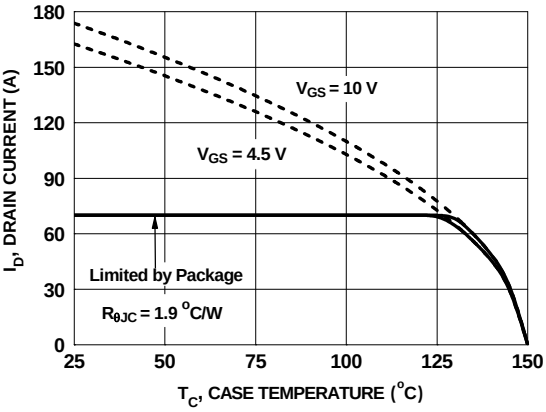


Figure 23. Maximum Continuous Drain Current vs Case Temperature

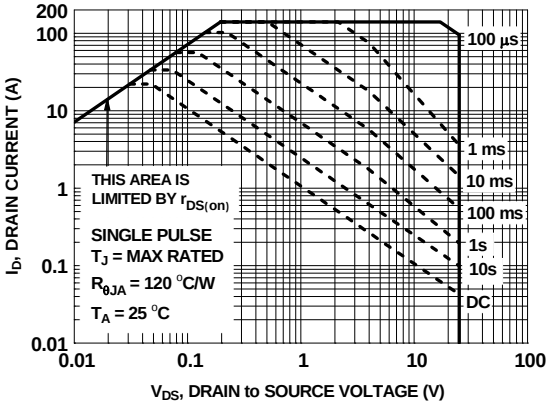


Figure 24. Forward Bias Safe Operating Area

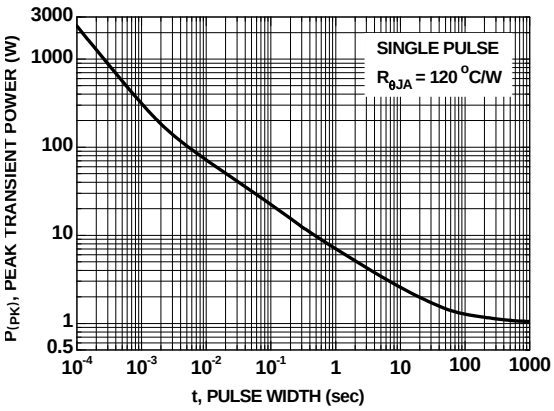


Figure 25. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q2 N-Channel) T_J = 25 °C unless otherwise noted

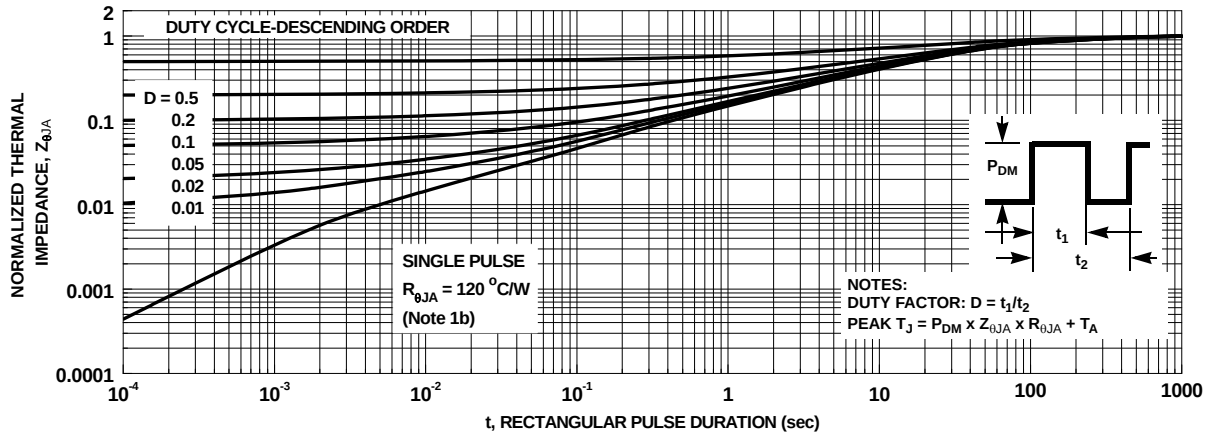


Figure 26. Junction-to-Ambient Transient Thermal Response Curve

Typical Characteristics (continued)

SyncFET Schottky body diode Characteristics

Fairchild's SyncFET process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 27 shows the reverse recovery characteristic of the FDMS3622S.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

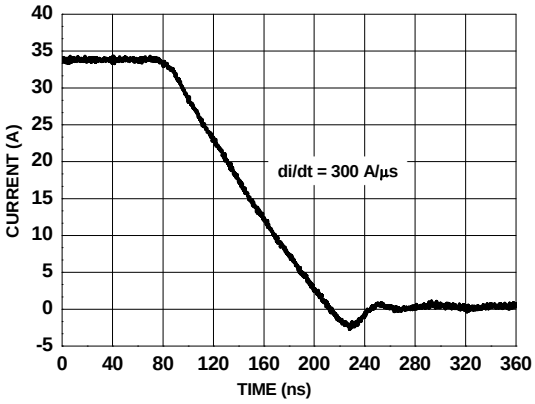


Figure 27. FDMS3622S SyncFET body diode reverse recovery characteristic

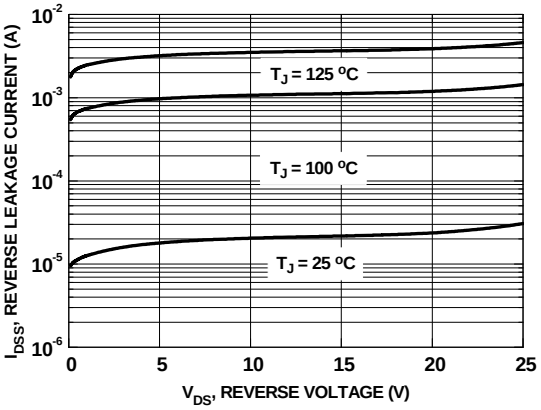
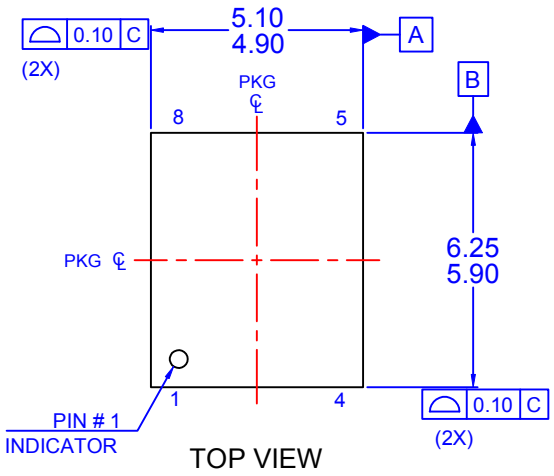
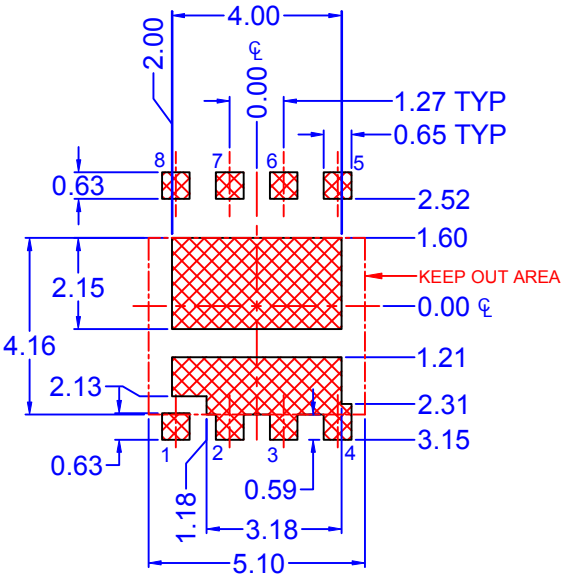


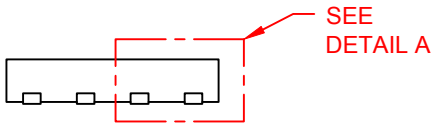
Figure 28. SyncFET body diode reverse leakage versus drain-source voltage



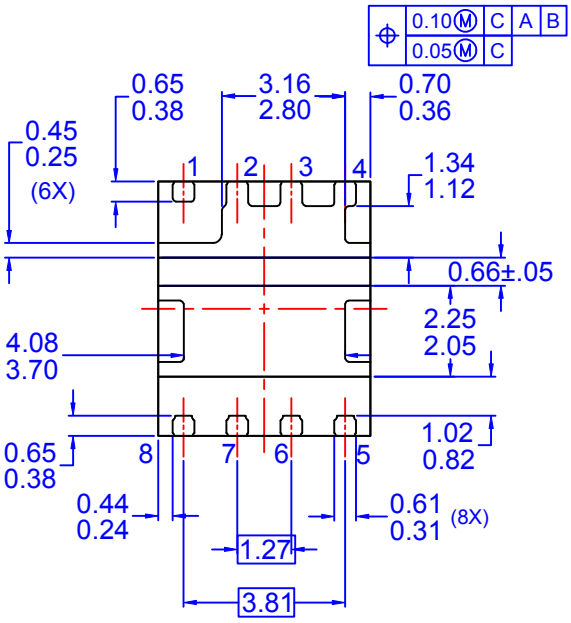
TOP VIEW



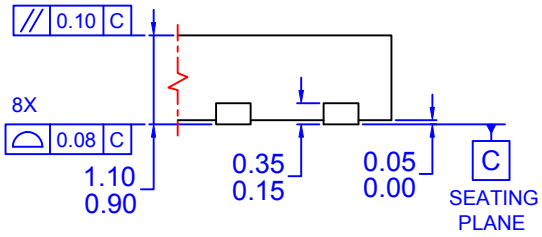
RECOMMENDED LAND PATTERN
FOR SAWN / PUNCHED TYPE



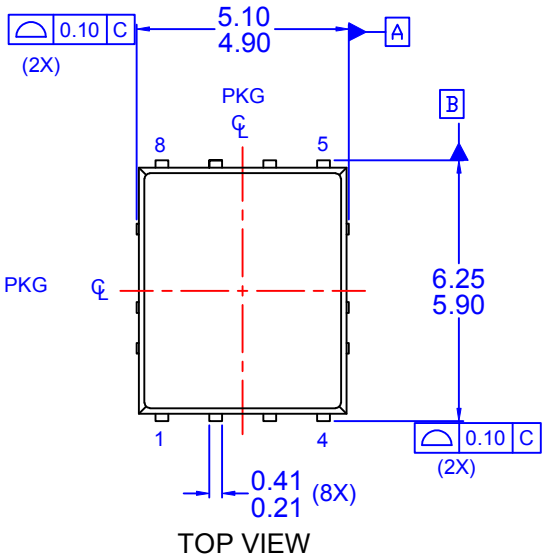
SIDE VIEW



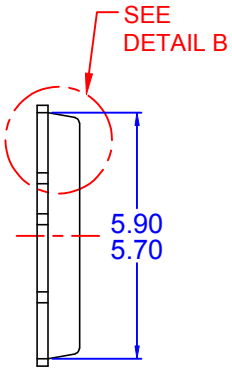
BOTTOM VIEW
OPTION - A (SAWN TYPE)

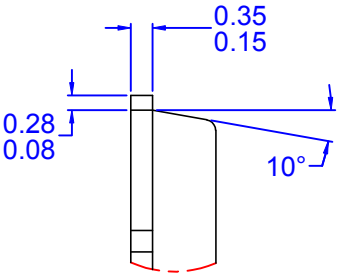


DETAIL 'A'
(SCALE: 2X)

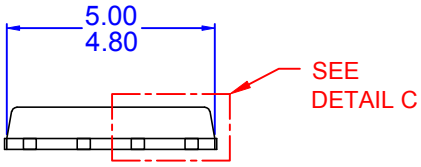


TOP VIEW

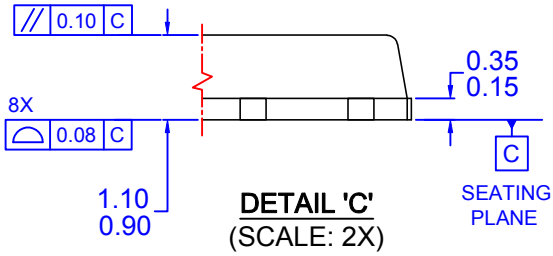




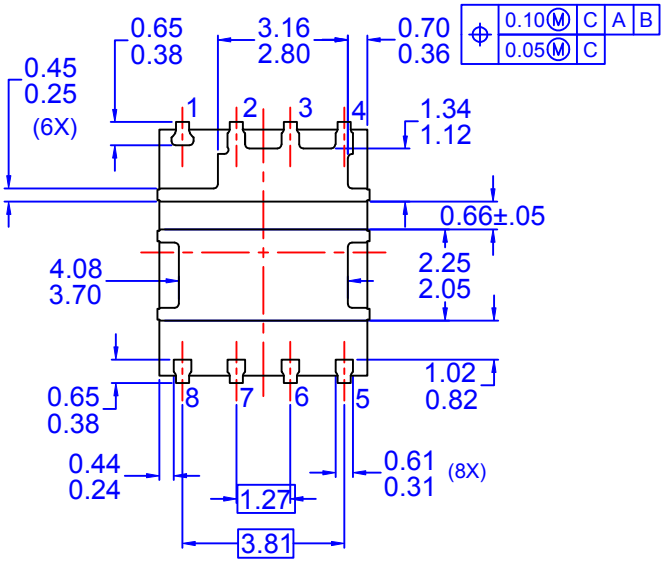
DETAIL 'B'
(SCALE: 2X)



SIDE VIEW



DETAIL 'C'
(SCALE: 2X)



BOTTOM VIEW

OPTION - B (PUNCHED TYPE)

NOTES: UNLESS OTHERWISE SPECIFIED

A) PACKAGE STANDARD REFERENCE: JEDEC REGISTRATION, MO-240, VARIATION AA.

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.

D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

F) DRAWING FILE NAME: PQFN08EREV6.

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