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ON Semiconductor®

FDS6898AZ-F085

Dual N-Channel Logic Level PWM Optimized PowerTrench® MOSFET

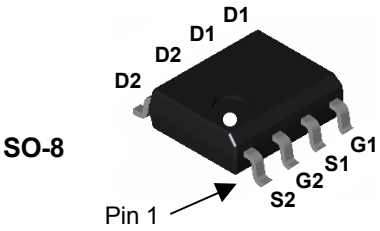
General Description

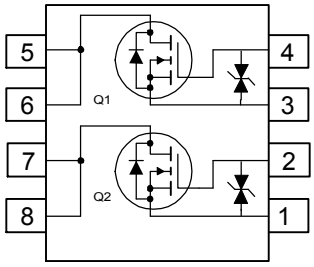
These N-Channel Logic Level MOSFETs are produced using ON Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

Features

- 9.4 A, 20 V $R_{DS(ON)}$ = 14 mΩ @ V_{GS} = 4.5 V
  $R_{DS(ON)}$ = 18 mΩ @ V_{GS} = 2.5 V
- Low gate charge (16 nC typical)
- ESD protection diode (note 3)
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability
- Qualified to AEC Q101
- RoHS Compliant





Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		20	V
V_{GSS}	Gate-Source Voltage		± 12	V
I_D	Drain Current – Continuous	(Note 1a)	9.4	A
	– Pulsed		38	
P_D	Power Dissipation for Dual Operation		2	W
	Power Dissipation for Single Operation	(Note 1a)	1.6	
		(Note 1b)	1	
		(Note 1c)	0.9	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS6898AZ	FDS6898AZ-F085	13''	12mm	2500 units

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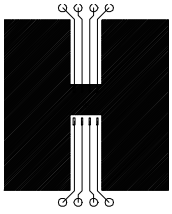
Electrical Characteristics

T_A = 25°C unless otherwise noted

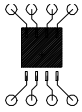
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C		21		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V			1	μA
I_{GSSF}	Gate–Body Leakage, Forward	V_{GS} = 12 V, V_{DS} = 0 V			10	μA
I_{GSSR}	Gate–Body Leakage, Reverse	V_{GS} = –12 V, V_{DS} = 0 V			–10	μA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	0.5	1	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C		–3.5		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = 4.5 V, I_D = 9.4 A V_{GS} = 2.5 V, I_D = 8.3 A V_{GS} = 4.5 V, I_D = 9.4 A, T_J = 125°C		10 13 14	14 18 21	mΩ
$I_{D(on)}$	On–State Drain Current	V_{GS} = 4.5V, V_{DS} = 5 V	19			A
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 9.4 A		47		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz		1821		pF
C_{oss}	Output Capacitance			440		pF
C_{rss}	Reverse Transfer Capacitance			208		pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = 10 V, I_D = 1 A, V_{GS} = 4.5 V, R_{GEN} = 6 Ω		10	20	ns
t_r	Turn–On Rise Time			15	27	ns
$t_{d(off)}$	Turn–Off Delay Time			34	55	ns
t_f	Turn–Off Fall Time			16	29	ns
Q_g	Total Gate Charge	V_{DS} = 10 V, I_D = 9.4 A, V_{GS} = 4.5 V		16	23	nC
Q_{gs}	Gate–Source Charge			3		nC
Q_{gd}	Gate–Drain Charge			4		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				1.3	A
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.3 A (Note 2)		0.7	1.2	V

Notes:

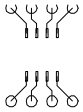
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 78°C/W when mounted on a 0.5in^2 pad of 2 oz copper



b) 125°C/W when mounted on a 0.02 in^2 pad of 2 oz copper



c) 135°C/W when mounted on a minimum mounting pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%

3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied

Typical Characteristics

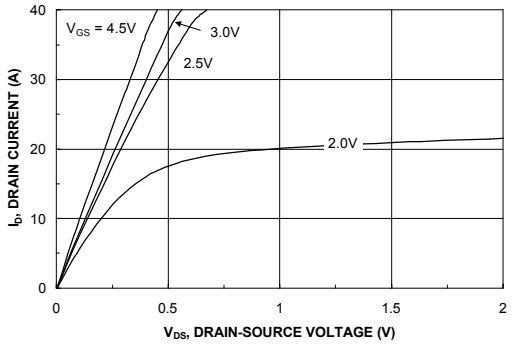


Figure 1. On-Region Characteristics.

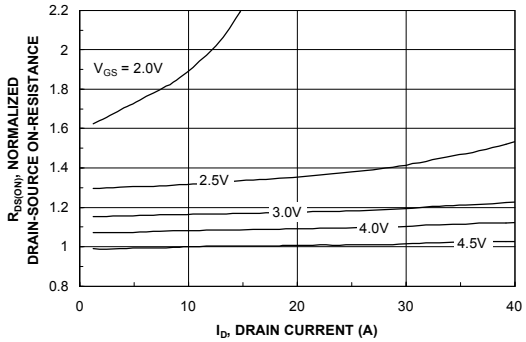


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

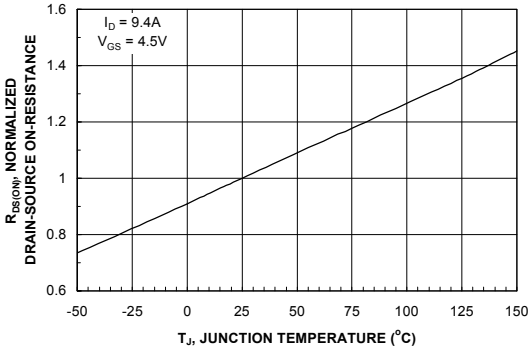


Figure 3. On-Resistance Variation with Temperature.

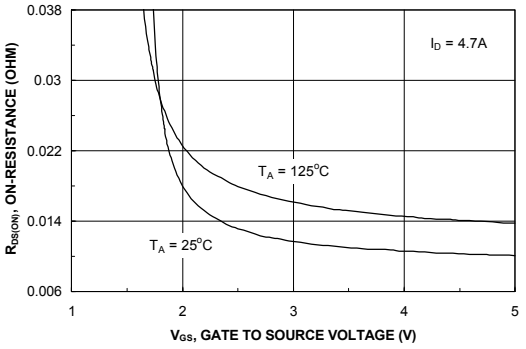


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

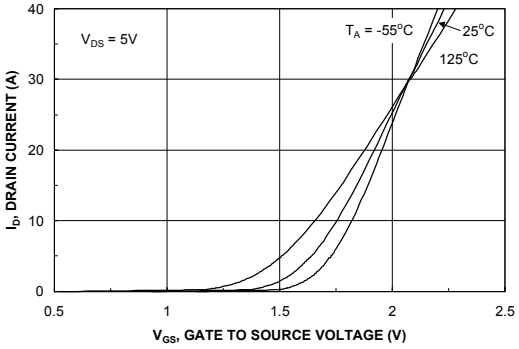


Figure 5. Transfer Characteristics.

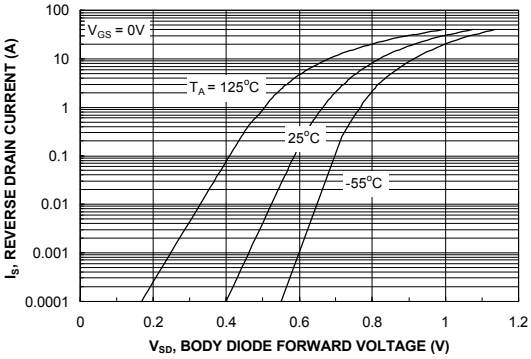


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

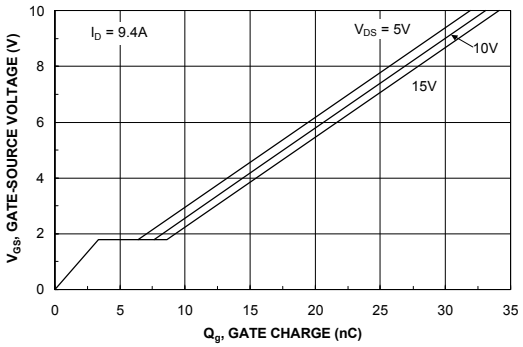


Figure 7. Gate Charge Characteristics.

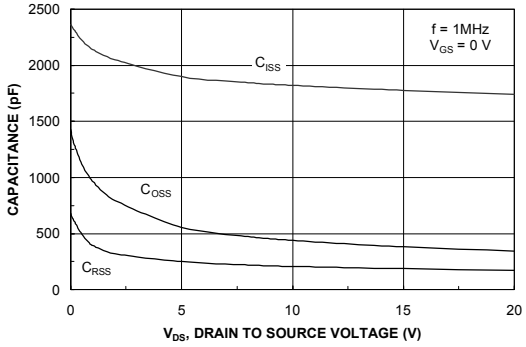


Figure 8. Capacitance Characteristics.

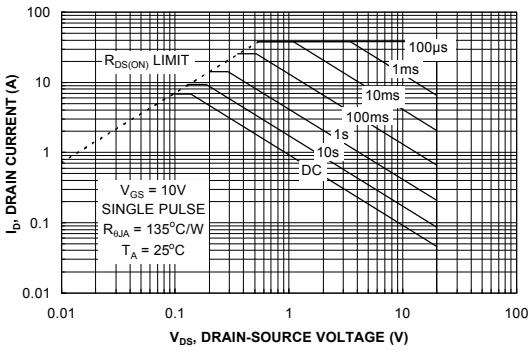


Figure 9. Maximum Safe Operating Area.

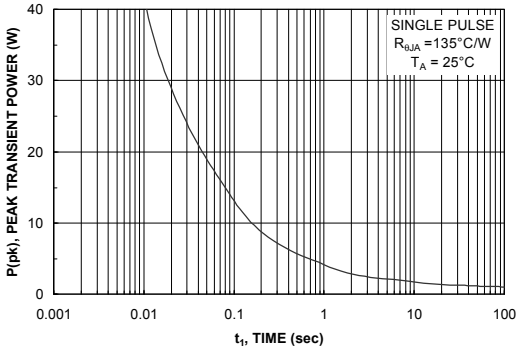


Figure 10. Single Pulse Maximum Power Dissipation.

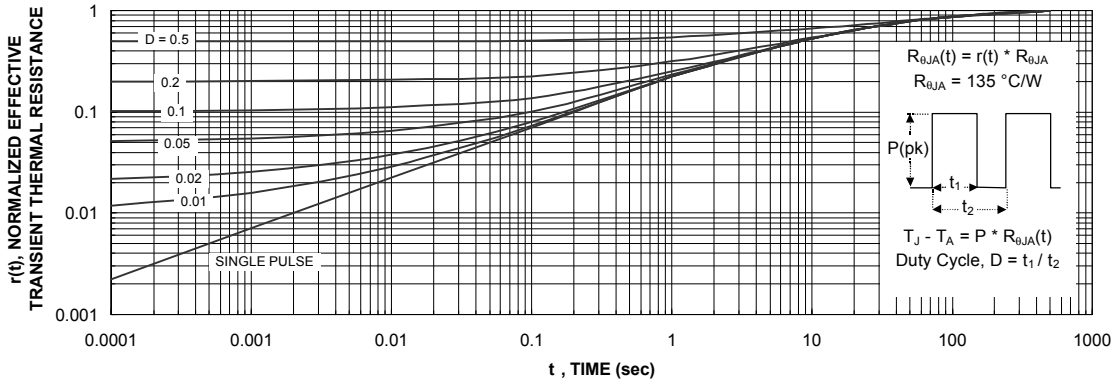


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

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