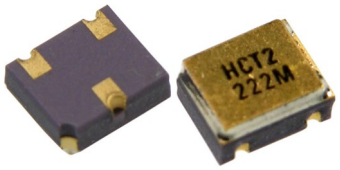
N-Channel Enhancement Mode MOS Transistor

HCT7000M, HCT70000MTX, HCT7000MTXV

Features:

- 200 mA I_D
- Ultra small surface mount package
- $R_{DS(ON)}$ < 5Ω
- Pin-out compatible with most SOT23 MOSFETS



Description:

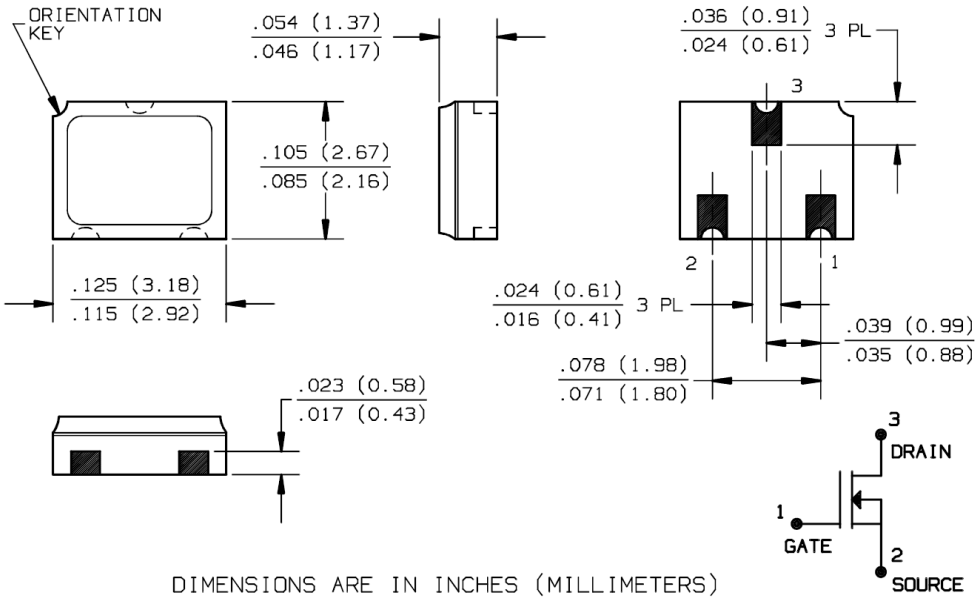
The HCT7000M is a high performance enhancement mode N-channel MOS transistor chip packaged in the ultra small 3 pin ceramic LCC package. Electrical characteristics are similar to those of the JEDEC 2N7000. The pin-out and footprint matches that of most enhancement mode MOS transistors built in SOT23 plastic packages.

TX and TXV devices are processed to OPTEK's military screening program patterned after MIL-PRF-19500.
TX products receive a V_{GS} HTRB at 24 V for 48 hrs. at 150° C and a V_{DS} HTRB at 48 V for 260 hrs.at 150° C.

Applications:

- Switching applications: small servo motor control, power MOSFET gate drives
- Relay Drivers
- High Speed Line Drivers
- Power Supplies

Part Number	Sensor Type	V_{DSS} Min	$V_{GS(TH)}$ Min/ Max	$I_{D(ON)}$ (mA) Min	G_{fs} (ms) Min	$t_{(ON)}$ / $t_{(OFF)}$ (ns) Max	Package
HCT7000M	N-Channel Enhanced MOSFET	60	0.8 / 3.0	75	100	10 / 10	3-pin Ceramic
HCT7000MTX							
HCT7000MTXV							



General Note
TT Electronics reserves the right to make changes in product specification without notice or liability. All information is subject to TT Electronics' own data and is considered accurate at time of going to print.

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N-Channel Enhancement Mode MOS Transistor

HCT7000M, HCT70000MTX, HCT7000MTXV

Performance

Absolute Maximum Ratings	
Drain Source Voltage	60V
Gate-Source Voltage	±40 V
Drain Current	200 mA
Power Dissipation (T_A = 25° C)	300 mW
Power Dissipation (T_S[(1)] = 25° C)	600 mW[(2)]
Operating and Storage Temperature	-55° C to 150° C
Thermal Resistance $R_{ØJC}$	100° C/W
Thermal Resistance $R_{ØJA}$	583° C/W

Electrical Characteristics (T_A = 25° C unless otherwise noted)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{DSS}	Drain Source Voltage	60		V	V_{GS} = 0 V, I_D = 10 µa
$V_{GS(TH)}$	Gate Threshold Voltage	.8	3.0	V	V_{DS} = V_{GS}, I_D = 1 mA
I_{GSS}	Gate Leakage		±10	nA	V_{DS} = 0 V, V_{GS} = ±15 V
I_{DSS}	Zero Gate Voltage Drain Current		1	µA	V_{GS} = 0 V, V_{DS} = 48 V
$I_{D(ON)}$	On-Site Drain Current	75		mA	V_{DS} = 10 V, V_{GS} = 4.5 V
$R_{DS(ON)}$	Drain Source on-Resistance		5	Ω	V_{GS} = 10 V, I_D = 0.5 A
$V_{DS(ON)}$	Drain Source on-Voltage		2.5	V	V_{GS} = 10 V, I_D = 0.5 A
G_{fs}	Forward Transconductance	100		mS	V_{DS} = 10 V, I_D = 0.2 A
C_{iss}	Input Capacitance		60	pF	V_{DS} = 25 V, V_{GS} = 0 V, f = 1MHz
C_{oss}	Output Capacitance		25	pF	
C_{rss}	Reverse Transfer Capacitance		5	pF	
$t_{(on)}$	Turn-on Time		10	ns	V_{DD} = 15 V, I_D = 0.5 A, V_{gen} = 10 V, R_g = 25Ω
$t_{(off)}$	Turn-off Time		10	ns	

Note:
1) T_S = Substrate temperature that the chip carrier is mounted on.
2) This rating is provided as an aid to designers. It is dependent upon mounting material and methods and is not measurable as an outgoing test.

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