IRGP4760PbF
IRGP4760-EPbF

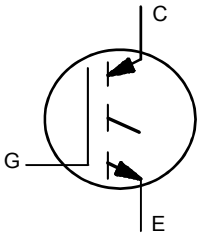
Insulated Gate Bipolar Transistor

V_{CES} = 650V

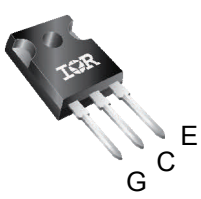
I_C = 60A, T_C =100°C

$t_{SC} \geq$ 5.5µs, $T_{J(max)}$ = 175°C

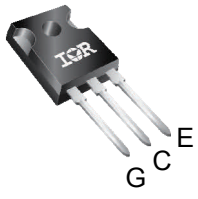
$V_{CE(ON)}$ typ. = 1.7V @ I_C = 48A



n-channel



IRGP4760PbF
TO-247AC



IRGP4760-EPbF
TO-247AD

G	C	E
Gate	Collector	Emitter

Applications

- Industrial Motor Drive
- UPS
- Solar Inverters
- Welding

Features →	Benefits
Low $V_{CE(ON)}$ and Switching Losses	High Efficiency in a Wide Range of Applications
5.5µs Short Circuit SOA Square RBSOA	Rugged Transient Performance
Maximum Junction Temperature 175°C	Increased Reliability
Positive $V_{CE\ (ON)}$ Temperature Coefficient	Excellent Current Sharing in Parallel Operation
Lead-Free, RoHs compliant	Environmentally friendly

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRGP4760PbF	TO-247AC	Tube	25	IRGP4760PbF
IRGP4760-EPbF	TO-247AD	Tube	25	IRGP4760-EPbF

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	650	V
I_C @ T_C = 25°C	Continuous Collector Current	90	A
I_C @ T_C = 100°C	Continuous Collector Current	60	
I_{CM}	Pulse Collector Current, V_{GE}=15V	144	
I_{LM}	Clamped Inductive Load Current, V_{GE}=20V ①	192	
V_{GE}	Continuous Gate-to-Emitter Voltage	±20	V
P_D @ T_C = 25°C	Maximum Power Dissipation	325	W
P_D @ T_C = 100°C	Maximum Power Dissipation	160	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-40 to +175	C
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw	10 lbf·in (1.1 N·m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Thermal Resistance Junction-to-Case ②	–––	–––	0.46	°C/W
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink (flat, greased surface)	–––	0.24	–––	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (typical socket mount)	–––	40	–––	

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Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	650	—	—	V	V_{GE} = 0V, I_C = 100µA ③
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.69	—	V/°C	V_{GE} = 0V, I_C = 3mA (25°C-175°C)
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	1.7	2.0	V	I_C = 48A, V_{GE} = 15V, T_J = 25°C
		—	2.1	—		I_C = 48A, V_{GE} = 15V, T_J = 175°C
$V_{GE(th)}$	Gate Threshold Voltage	5.5	—	7.4	V	V_{CE} = V_{GE}, I_C = 1.4mA
$\Delta V_{GE(th)}/\Delta T_J$	Threshold Voltage Temperature Coeff.	—	-23	—	mV/°C	V_{CE} = V_{GE}, I_C = 1.4mA (25°C-150°C)
gfe	Forward Transconductance	—	31	—	S	V_{CE} = 50V, I_C = 48A, PW = 20µs
I_{CES}	Collector-to-Emitter Leakage Current	—	1.0	25	µA	V_{GE} = 0V, V_{CE} = 650V
		—	700	—		V_{GE} = 0V, V_{CE} = 650V, T_J = 175°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max④	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	96	145	nC	I_C = 48A
Q_{ge}	Gate-to-Emitter Charge (turn-on)	—	30	45		V_{GE} = 15V
Q_{gc}	Gate-to-Collector Charge (turn-on)	—	40	60		V_{CC} = 400V
E_{on}	Turn-On Switching Loss	—	1.7	2.6	mJ	I_C = 48A, V_{CC} = 400V, V_{GE}=15V R_G = 10Ω, L = 210µH, T_J = 25°C Energy losses include tail & diode reverse recovery ⑤⑥
E_{off}	Turn-Off Switching Loss	—	1.0	1.9		
E_{total}	Total Switching Loss	—	2.7	4.5		
$t_{d(on)}$	Turn-On delay time	—	70	90	ns	
t_r	Rise time	—	60	80		
$t_{d(off)}$	Turn-Off delay time	—	140	160		
t_f	Fall time	—	30	50		
E_{on}	Turn-On Switching Loss	—	2.9	—	mJ	I_C = 48A, V_{CC} = 400V, V_{GE}=15V R_G = 10Ω, L = 210µH, T_J = 175°C Energy losses include tail & diode reverse recovery ⑤⑥
E_{off}	Turn-Off Switching Loss	—	1.4	—		
E_{total}	Total Switching Loss	—	4.3	—		
$t_{d(on)}$	Turn-On delay time	—	55	—	ns	
t_r	Rise time	—	60	—		
$t_{d(off)}$	Turn-Off delay time	—	145	—		
t_f	Fall time	—	65	—		
C_{ies}	Input Capacitance	—	3000	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	150	—		V_{CC} = 30V
C_{res}	Reverse Transfer Capacitance	—	80	—		f = 1.0MHz
RBSOA	Reverse Bias Safe Operating Area	FULL SQUARE				T_J = 175°C, I_C = 192A V_{CC} = 520V, Vp ≤ 650V V_{GE} = +20V to 0V
SCSOA	Short Circuit Safe Operating Area	5.5	—	—	µs	T_J = 150°C,V_{CC} = 400V, Vp ≤ 650V V_{GE} = +15V to 0V

Notes:

① V_{CC} = 80% (V_{CES}), V_{GE} = 20V.

② R_θ is measured at T_J of approximately 90°C.

③ Refer to AN-1086 for guidelines for measuring $V_{(BR)CES}$ safely.

④ Maximum limits are based on statistical sample size characterization.

⑤ Pulse width limited by max. junction temperature.

⑥ Values influenced by parasitic L and C in measurement.

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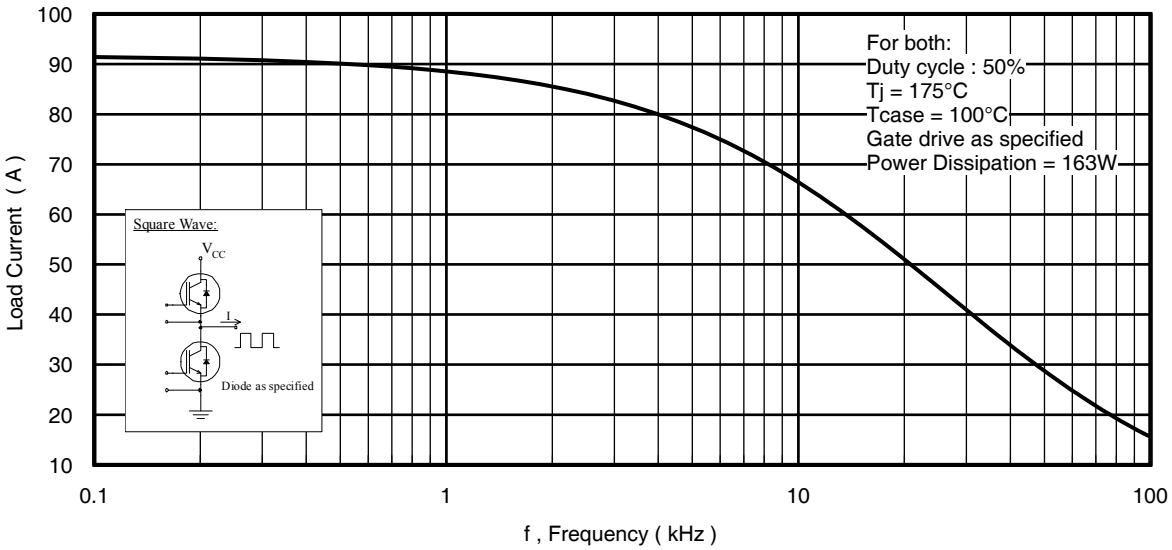


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = IRMS of fundamental)

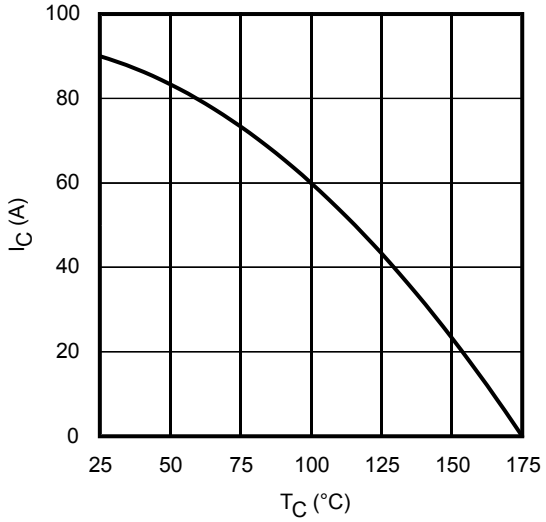


Fig. 2 - Maximum DC Collector Current vs. Case Temperature

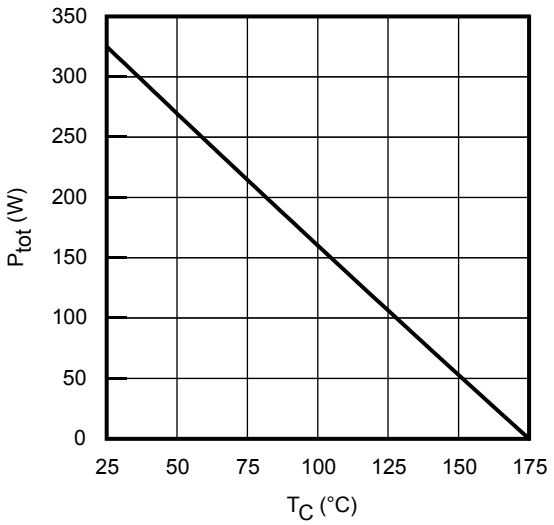


Fig. 3 - Power Dissipation vs. Case Temperature

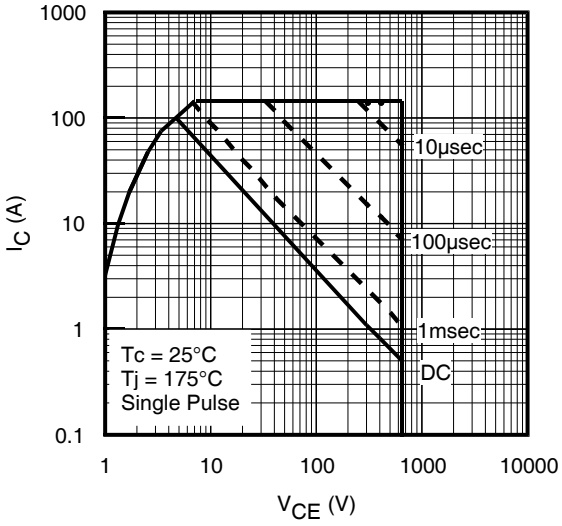


Fig. 4 - Forward SOA
T_C = 25°C; T_J ≤ 175°C; V_{GE} = 15V

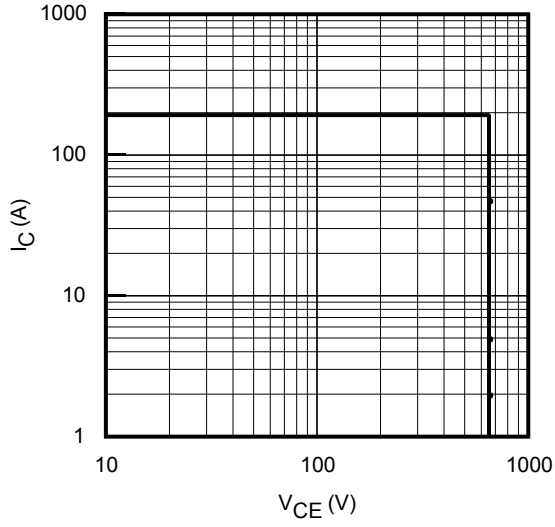


Fig. 5 - Reverse Bias SOA
T_J = 175°C; V_{GE} = 20V

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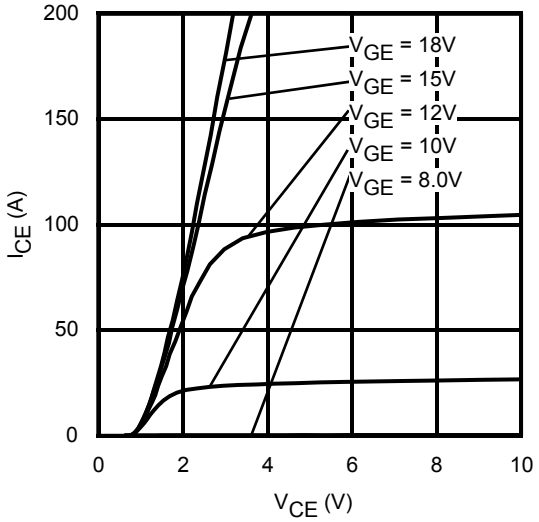


Fig. 6 - Typ. IGBT Output Characteristics
T_J = -40°C; tp = 20µs

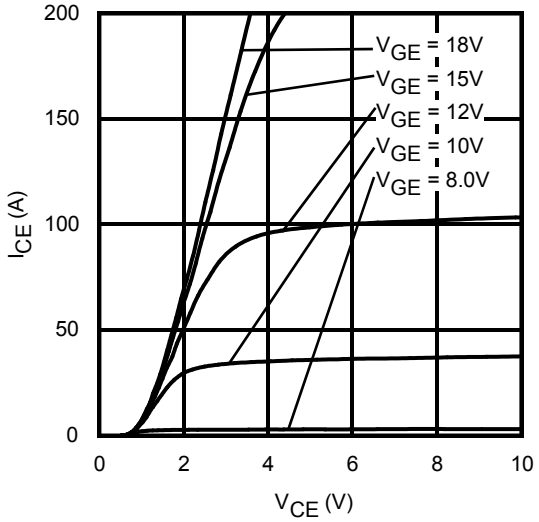


Fig. 7 - Typ. IGBT Output Characteristics
T_J = 25°C; tp = 20µs

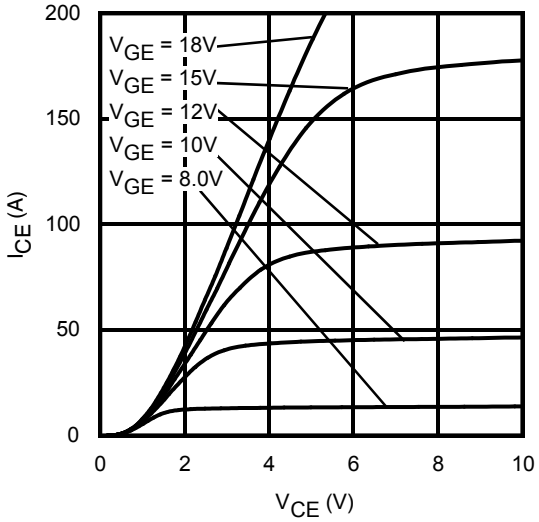


Fig. 8 - Typ. IGBT Output Characteristics
T_J = 175°C; tp = 20µs

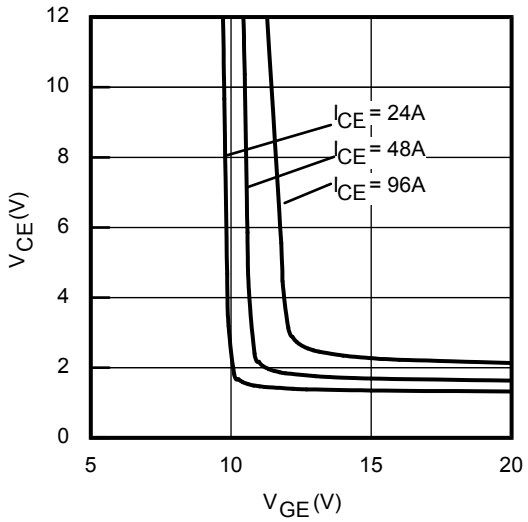


Fig. 9 - Typical V_{CE} vs. V_{GE}
T_J = -40°C

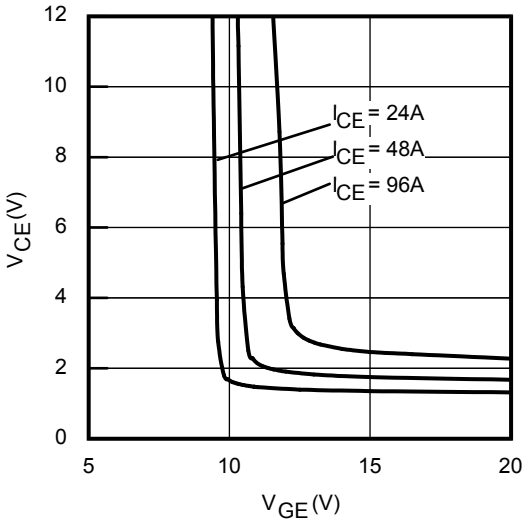


Fig. 10 - Typical V_{CE} vs. V_{GE}
T_J = 25°C

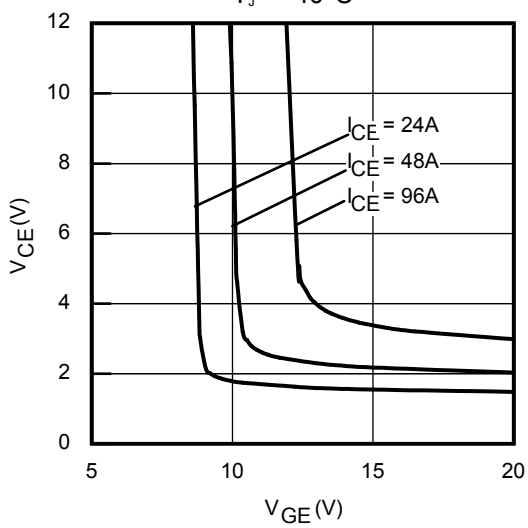


Fig. 11 - Typical V_{CE} vs. V_{GE}
T_J = 175°C

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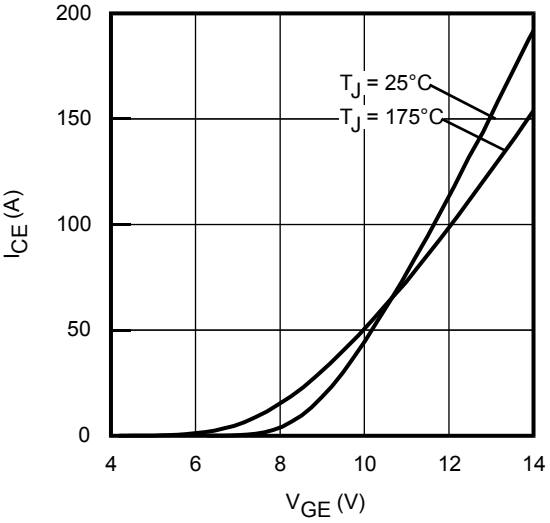


Fig. 12 - Typ. Transfer Characteristics
V_{CE} = 50V; tp = 20µs

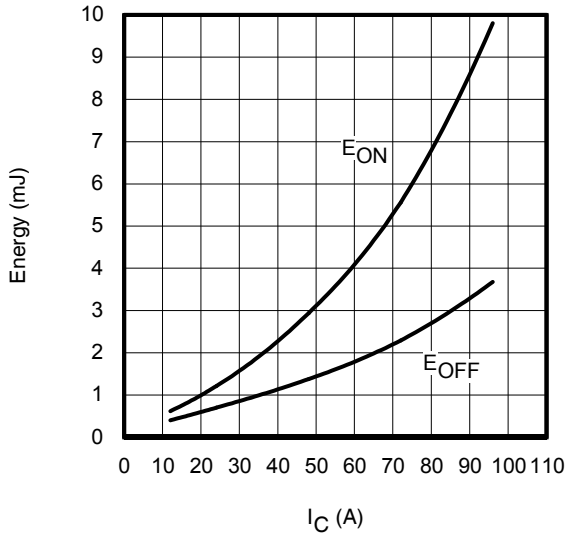


Fig. 13 - Typ. Energy Loss vs. I_C
T_J = 175°C; L = 210µH; V_{CE} = 400V, R_G = 10Ω; V_{GE} = 15V

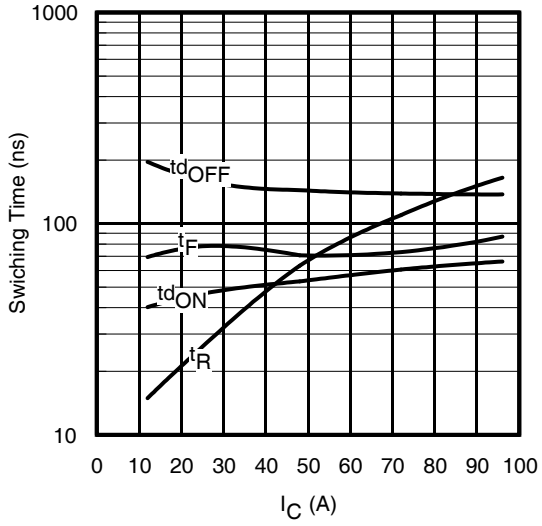


Fig. 14 - Typ. Switching Time vs. I_C
T_J = 175°C; L = 210µH; V_{CE} = 400V, R_G = 10Ω; V_{GE} = 15V

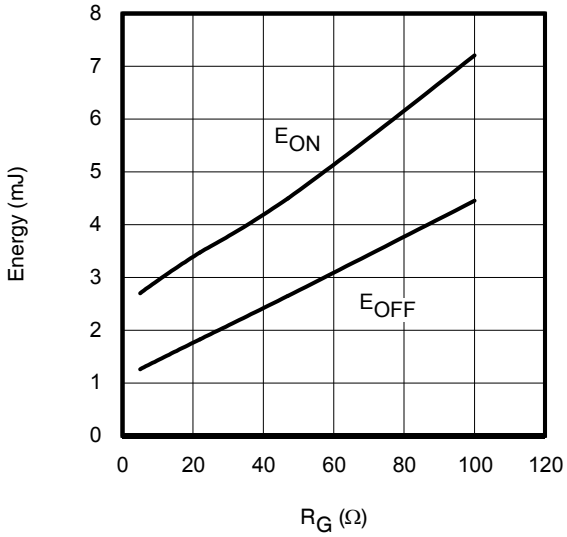


Fig. 15 - Typ. Energy Loss vs. R_G
T_J = 175°C; L = 210µH; V_{CE} = 400V, I_{CE} = 48A; V_{GE} = 15V

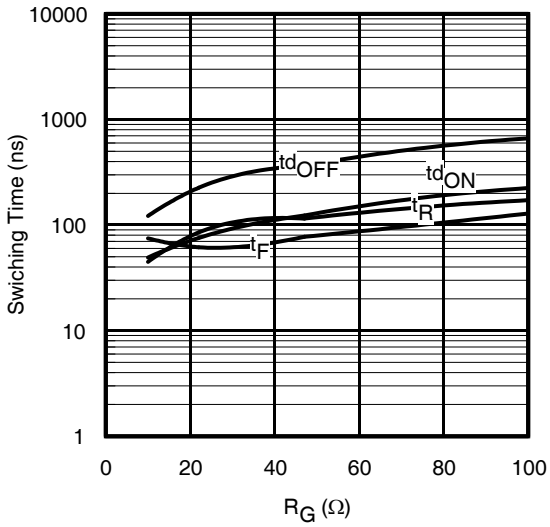


Fig. 16 - Typ. Switching Time vs. R_G
T_J = 175°C; L = 210µH; V_{CE} = 400V, I_{CE} = 48A; V_{GE} = 15V

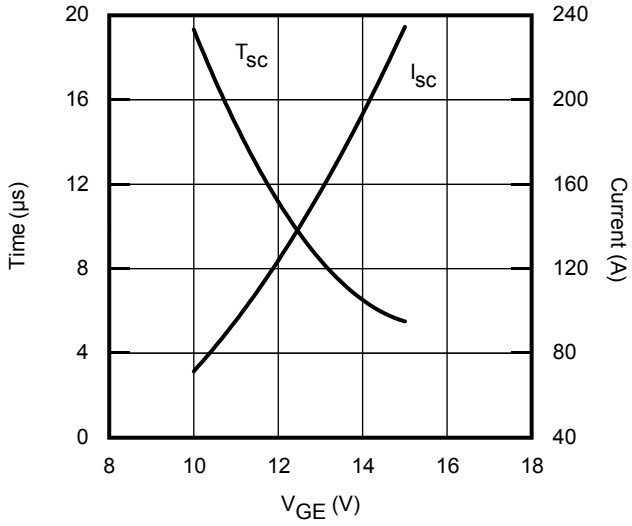


Fig. 17 - V_{GE} vs. Short Circuit Time
V_{CC} = 400V; T_C = 150°C

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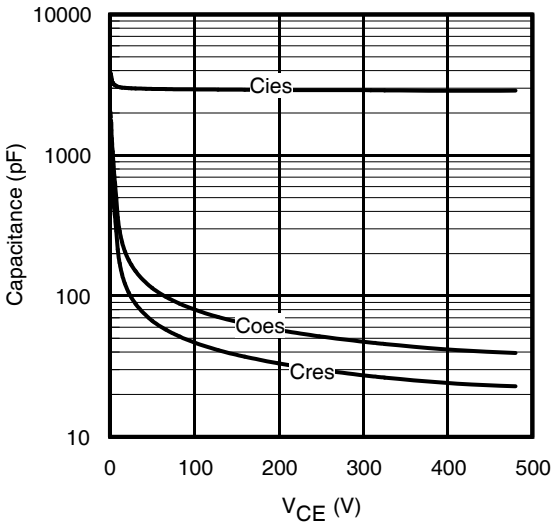


Fig. 18 - Typ. Capacitance vs. V_{CE}
V_{GE}= 0V; f = 1MHz

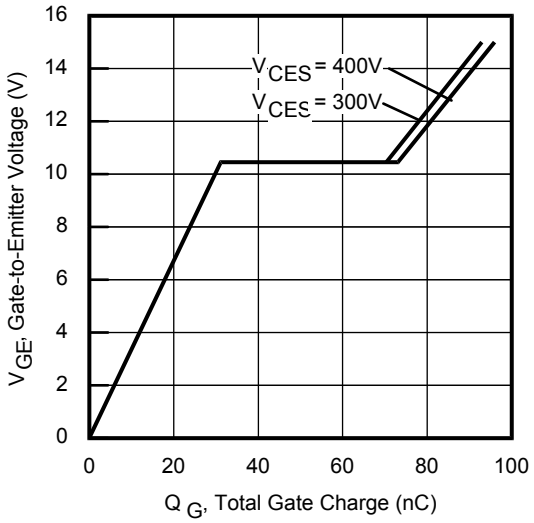


Fig. 19 - Typical Gate Charge vs. V_{GE}
I_{CE} = 48A

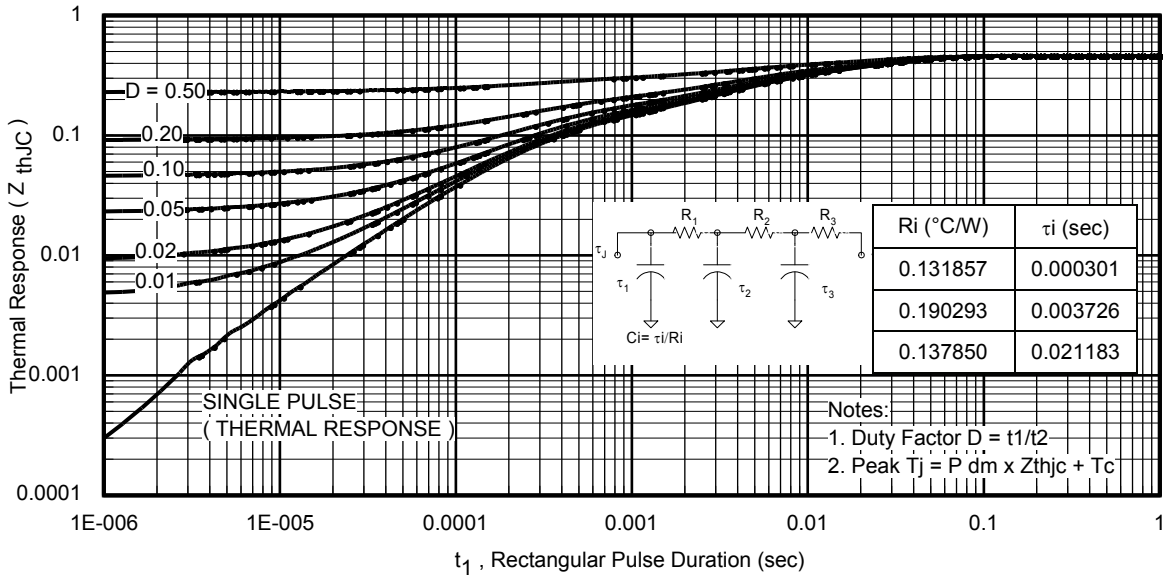


Fig. 20 - Maximum Transient Thermal Impedance, Junction-to-Case

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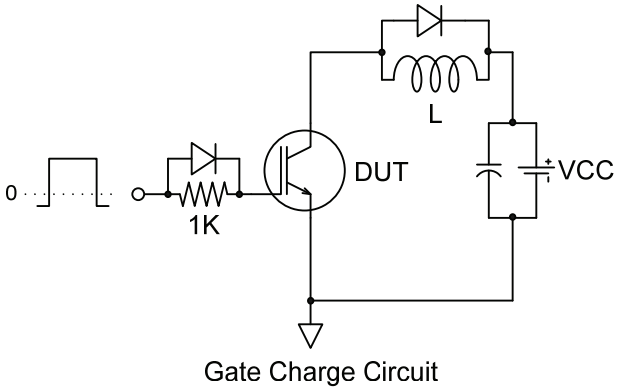


Fig.C.T.1 - Gate Charge Circuit (turn-off)

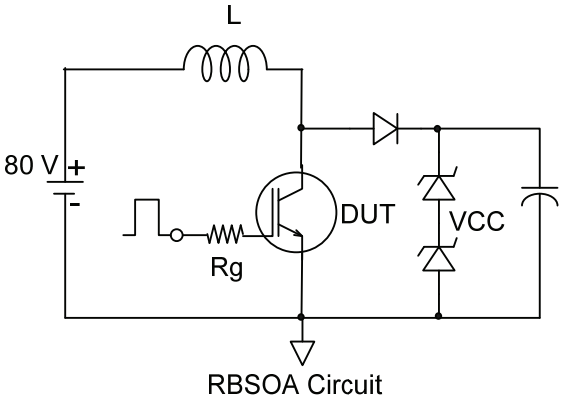


Fig.C.T.2 - RBSOA Circuit

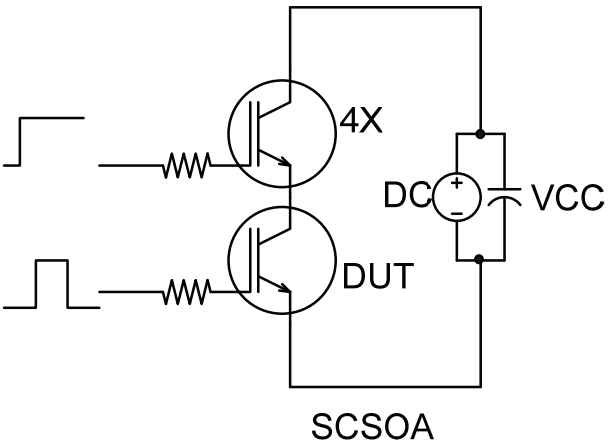


Fig.C.T.3 - S.C. SOA Circuit

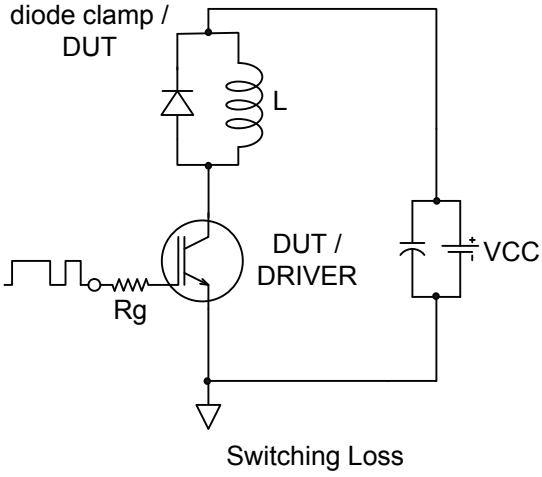


Fig.C.T.4 - Switching Loss Circuit

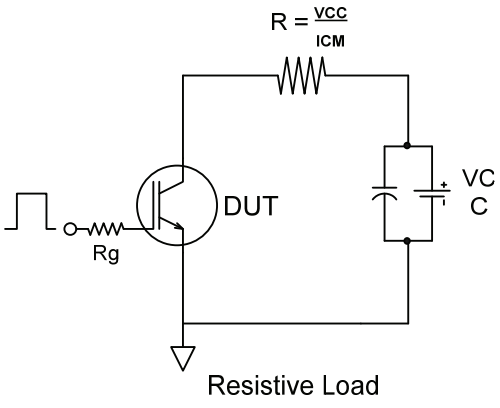


Fig.C.T.5 - Resistive Load Circuit

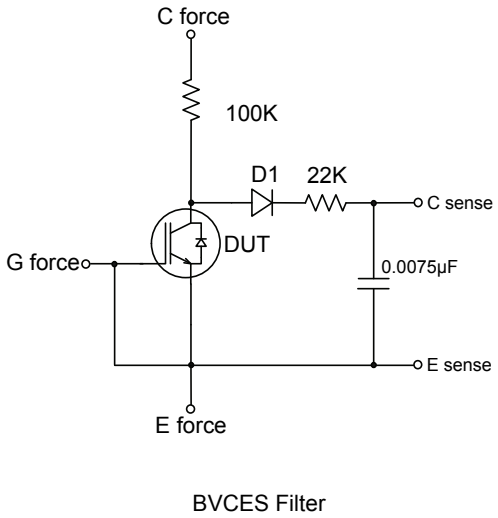


Fig.C.T.6 - BVCES Filter Circuit

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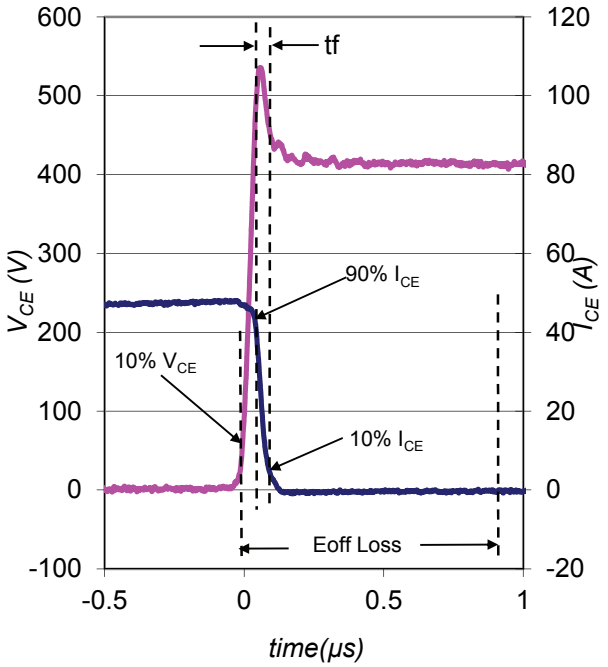


Fig. WF1 - Typ. Turn-off Loss Waveform
@ T_J = 175°C using Fig. CT.4

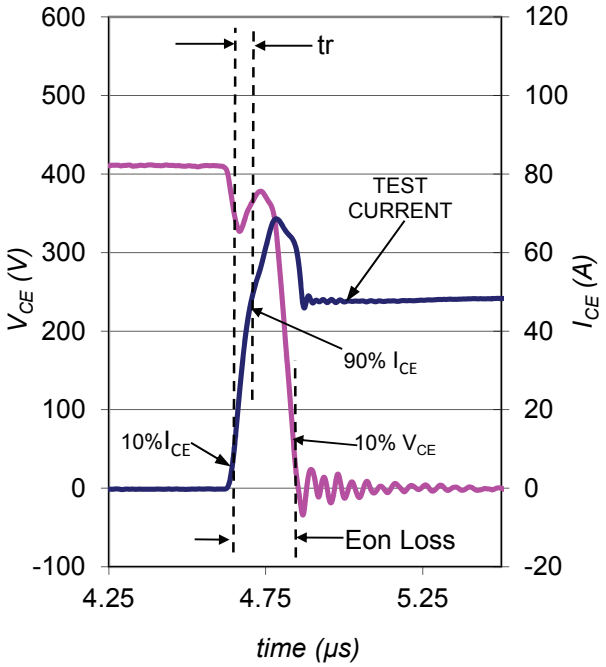


Fig. WF2 - Typ. Turn-on Loss Waveform
@ T_J = 175°C using Fig. CT.4

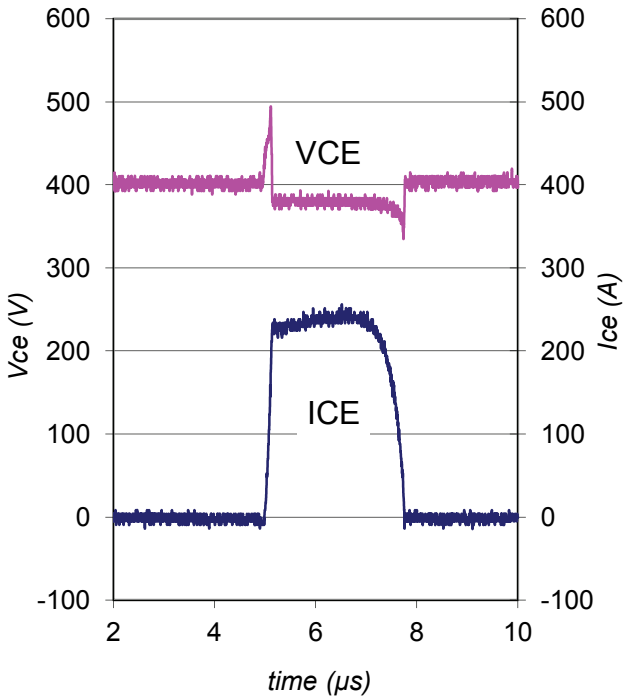
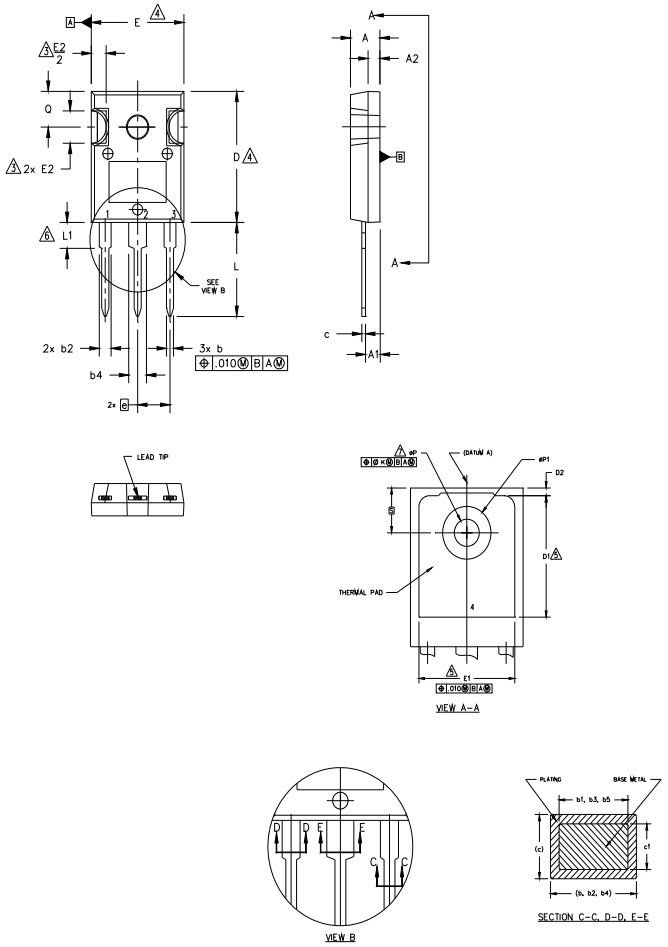


Fig. WF3 - Typ. S.C. Waveform
@ T_J = 150°C using Fig. CT.3

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TO-247AC Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES.
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
6. LEAD FINISH UNCONTROLLED IN L1.
7. øP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5 ° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AC .

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	4
D1	.515	–	13.08	–	5
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	4
E1	.530	–	13.46	–	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		
øk	.010		0.25		
L	.559	.634	14.20	16.10	
L1	.146	.169	3.71	4.29	
øP	.140	.144	3.56	3.66	
øP1	–	.291	–	7.39	
Q	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

LEAD ASSIGNMENTS

HEXFET

1.– GATE
2.– DRAIN
3.– SOURCE
4.– DRAIN

IGBTs, CoPACK

1.– GATE
2.– COLLECTOR
3.– EMITTER
4.– COLLECTOR

DIODES

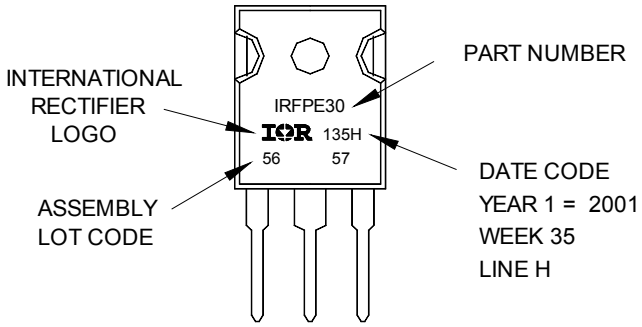
1.– ANODE/OPEN
2.– CATHODE
3.– ANODE

TO-247AC Part Marking Information

Notes: This part marking information applies to devices produced after 02/26/2001

EXAMPLE: THIS IS AN IRFPE30
WITH ASSEMBLY
LOT CODE 5657
ASSEMBLED ON WW 35, 2001
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position
indicates "Lead-Free"



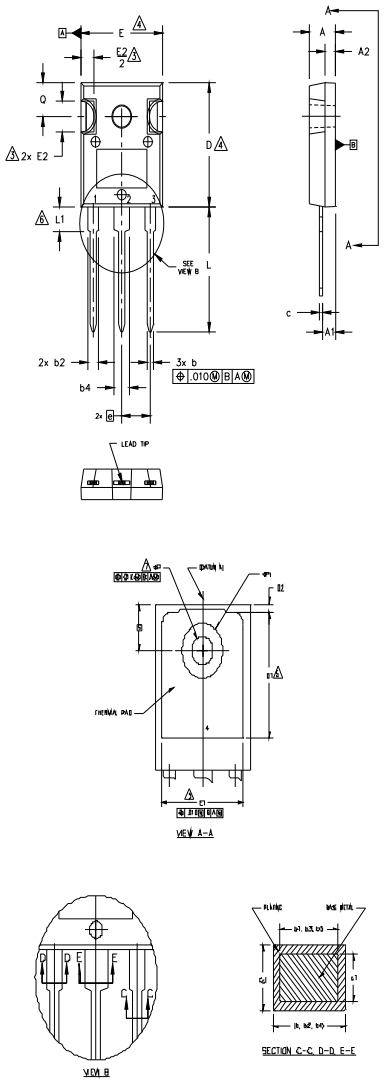
TO-247AC package is not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

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TO-247AD Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES.
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
6. LEAD FINISH UNCONTROLLED IN L1.
7. øP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5 ° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AD.

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	4
D1	.515	–	13.08	–	5
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	4
E1	.530	–	13.46	–	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		
øk	.010		0.25		
L	.780	.827	19.57	21.00	
L1	.146	.169	3.71	4.29	
øP	.140	.144	3.56	3.66	
øP1	–	.291	–	7.39	
Q	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

LEAD ASSIGNMENTS

HEXFET

1.- GATE
2.- DRAIN
3.- SOURCE
4.- DRAIN

IGBTs, CoPACK

1.- GATE
2.- COLLECTOR
3.- EMITTER
4.- COLLECTOR

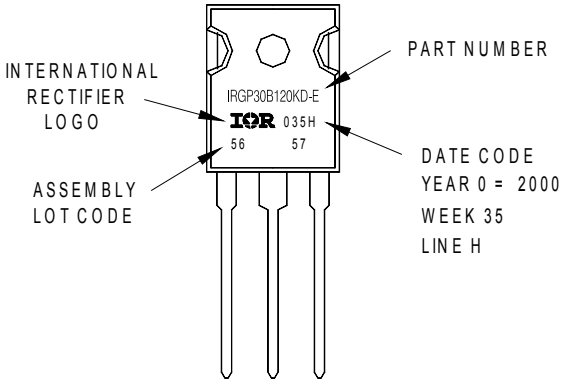
DIODES

1.- ANODE/OPEN
2.- CATHODE
3.- ANODE

TO-247AD Part Marking Information

EXAMPLE: THIS IS AN IRGP30B120KD-E
WITH ASSEMBLY
LOT CODE 5657
ASSEMBLED ON WW 35, 2000
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position
indicates "Lead-Free"



TO-247AD package is not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

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Qualification Information†

Qualification Level	Industrial (per JEDEC JESD47F) ††	
Moisture Sensitivity Level	TO-247AC	N/A
	TO-247AD	N/A
RoHS Compliant	Yes	

† Qualification standards can be found at International Rectifier's web site: http://www.irf.com/product-info/reliability/

†† Applicable version of JEDEC standard at the time of product release.

Revision History

Date	Comments
8/22/2014	• Updated I_C vs. T_C graph Fig.2 to match page1 spec data on page 3.

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To contact International Rectifier, please visit http://www.irf.com/whoto-call/

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