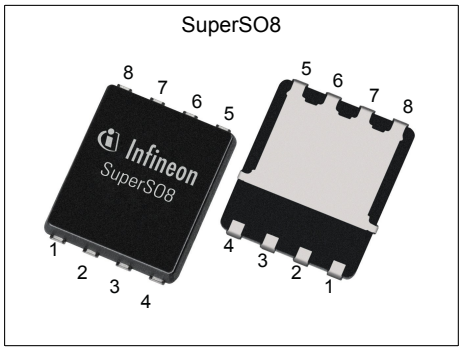
MOSFET

OptiMOS™ Power-Transistor, -150 V



Features

- P-Channel
- Very low on-resistance RDS(on) @ VGS=4.5 V
- 100% avalanche tested
- Logic Level
- Enhancement mode
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product validation

Fully qualified according to JEDEC for Industrial Applications

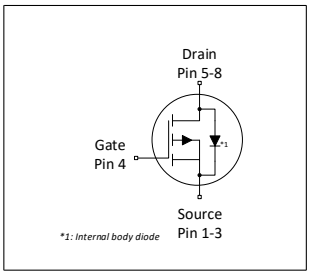


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	-150	V
$R_{DS(on),max}$	160	mΩ
I_D	-22	A

Type / Ordering Code	Package	Marking	Related Links
ISC16DP15LM	PG-TDSON-8	16DP15LM	-

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1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D	- - -	- - -	-22 -15.2 -2.5	A	V_{GS}=-10 V, T_C=25 °C V_{GS}=-10 V, T_C=100 °C V_{GS}=-4.5 V,T_A=25°C,R_{thJA}=60°C/W[2]
Pulsed drain current[3]	$I_{D,pulse}$	-	-	-86.1	A	T_A=25 °C
Avalanche energy, single pulse[4]	E_{AS}	-	-	700	mJ	I_D=-17 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	- -	- -	188 2.5	W	T_C=25 °C T_A=25 °C, R_{thJA}=60 °C/W[2]
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	0.42	0.8	°C/W	-
Device on PCB, 6 cm² cooling area	R_{thJA}	-	-	60	°C/W	-

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.
[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.
[3] See Diagram 3 for more detailed information
[4] See Diagram 13 for more detailed information

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	-150	-	-	V	V_{GS}=0 V, I_D=-250 µA
Gate threshold voltage	$V_{GS(th)}$	-1	-1.6	-2	V	V_{DS}=V_{GS}, I_D=-2304 µA
Zero gate voltage drain current	I_{DSS}	- -	-0.1 -10	-1 -100	µA	V_{DS}=-150 V, V_{GS}=0 V, T_j=25 °C V_{DS}=-150 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	-10	-100	nA	V_{GS}=-20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	134 136	160 160	mΩ	V_{GS}=-10 V, I_D=-10 A V_{GS}=-4.5 V, I_D=-8 A
Gate resistance	R_G	-	5	-	Ω	-
Transconductance	g_{fs}	-	31	-	S	|V_{DS}|≥2|I_D|$R_{DS(on)max}$, I_D=-10 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance[1)]	C_{iss}	-	3500	4600	pF	V_{GS}=0 V, V_{DS}=-75 V, f=1 MHz
Output capacitance[1)]	C_{oss}	-	140	180	pF	V_{GS}=0 V, V_{DS}=-75 V, f=1 MHz
Reverse transfer capacitance[1)]	C_{rss}	-	30	52	pF	V_{GS}=0 V, V_{DS}=-75 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	67.76	-	ns	V_{DD}=-75 V, V_{GS}=-4.5 V, I_D=-10 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r	-	18.24	-	ns	V_{DD}=-75 V, V_{GS}=-4.5 V, I_D=-10 A, $R_{G,ext}$=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	73.92	-	ns	V_{DD}=-75 V, V_{GS}=-4.5 V, I_D=-10 A, $R_{G,ext}$=1.6 Ω
Fall time	t_f	-	32.06	-	ns	V_{DD}=-75 V, V_{GS}=-4.5 V, I_D=-10 A, $R_{G,ext}$=1.6 Ω

Table 6 Gate charge characteristics[2)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	-9.4	-	nC	V_{DD}=-75 V, I_D=-10 A, V_{GS}=0 to -4.5 V
Gate charge at threshold	$Q_{g(th)}$	-	-5.6	-	nC	V_{DD}=-75 V, I_D=-10 A, V_{GS}=0 to -4.5 V
Gate to drain charge[1)]	Q_{gd}	-	-21	-32	nC	V_{DD}=-75 V, I_D=-10 A, V_{GS}=0 to -4.5 V
Switching charge	Q_{sw}	-	-25	-	nC	V_{DD}=-75 V, I_D=-10 A, V_{GS}=0 to -4.5 V
Gate charge total[1)]	Q_g	-	-46	-58	nC	V_{DD}=-75 V, I_D=-10 A, V_{GS}=0 to -4.5 V
Gate plateau voltage	$V_{plateau}$	-	-2.7	-	V	V_{DD}=-75 V, I_D=-10 A, V_{GS}=0 to -4.5 V
Gate charge total[1)]	Q_g	-	-94	-125	nC	V_{DD}=-75 V, I_D=-10 A, V_{GS}=0 to -10 V
Output charge[2)]	Q_{oss}	-	-26	-35	nC	V_{DS}=-75 V, V_{GS}=0 V

[1)] Defined by design. Not subject to production test.
[2)] See ″Gate charge waveforms″ for parameter definition

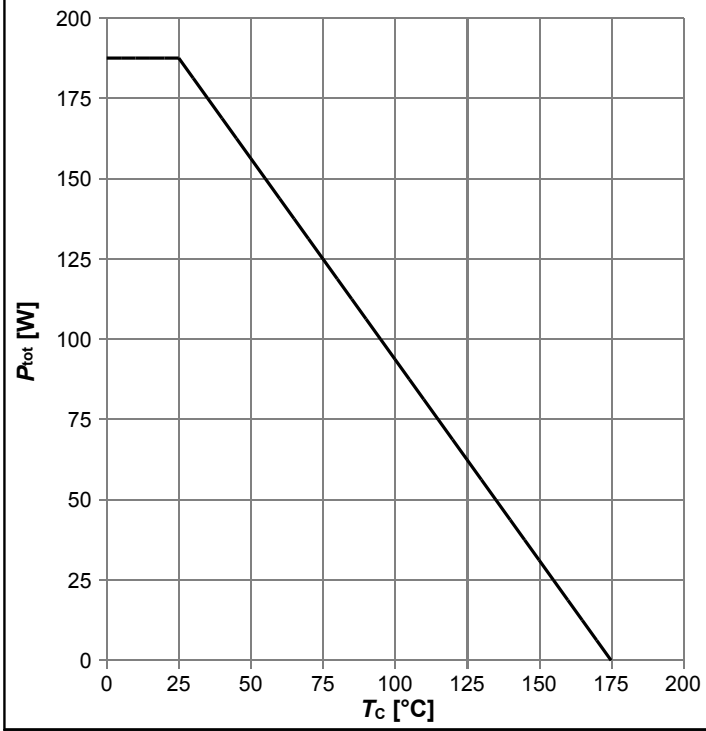
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	-22	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	-86.1	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	-0.8	-1.2	V	V_{GS}=0 V, I_F=-10 A, T_j=25 °C
Reverse recovery time[1)]	t_{rr}	-	96.2	192.4	ns	V_R=-75 V, I_F=-10 A, di_F/dt=-100 A/µs
Reverse recovery charge[1)]	Q_{rr}	-	-396.4	-792.8	nC	V_R=-75 V, I_F=-10 A, di_F/dt=-100 A/µs

[1)] Defined by design. Not subject to production test.

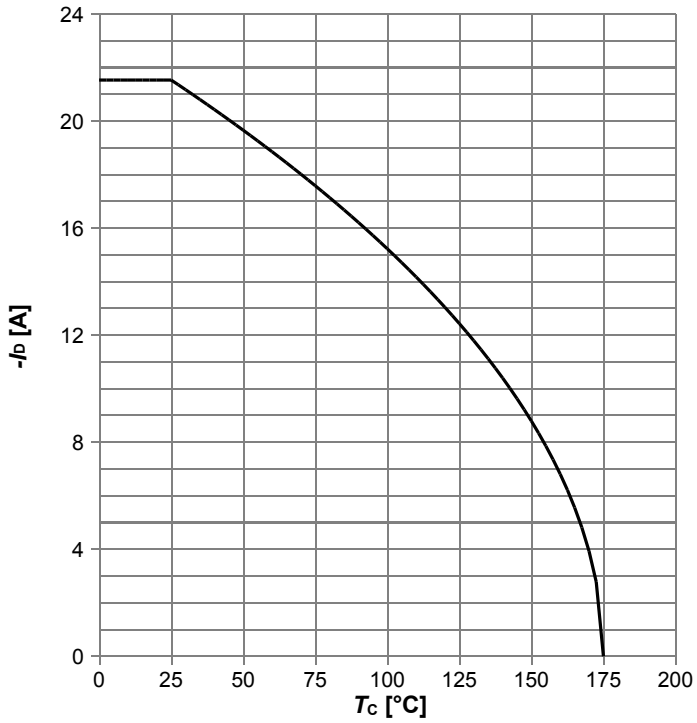
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



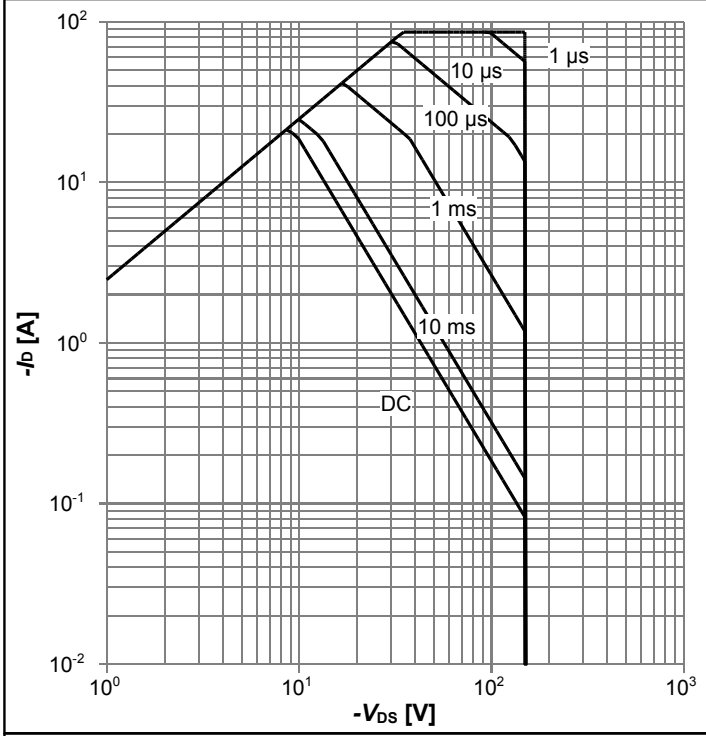
$P_{tot}=f(T_C)$

Diagram 2: Drain current



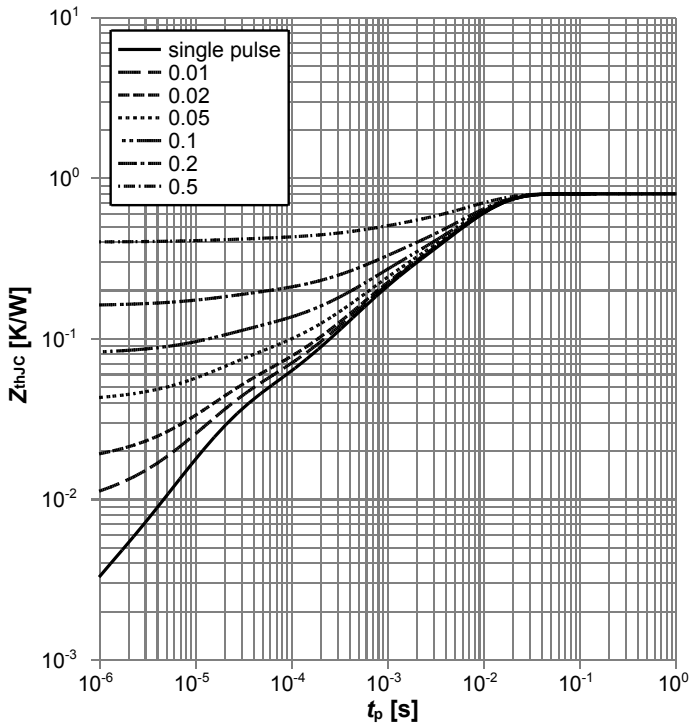
$I_D=f(T_C)$; $|V_{GS}|\geq 10$ V

Diagram 3: Safe operating area



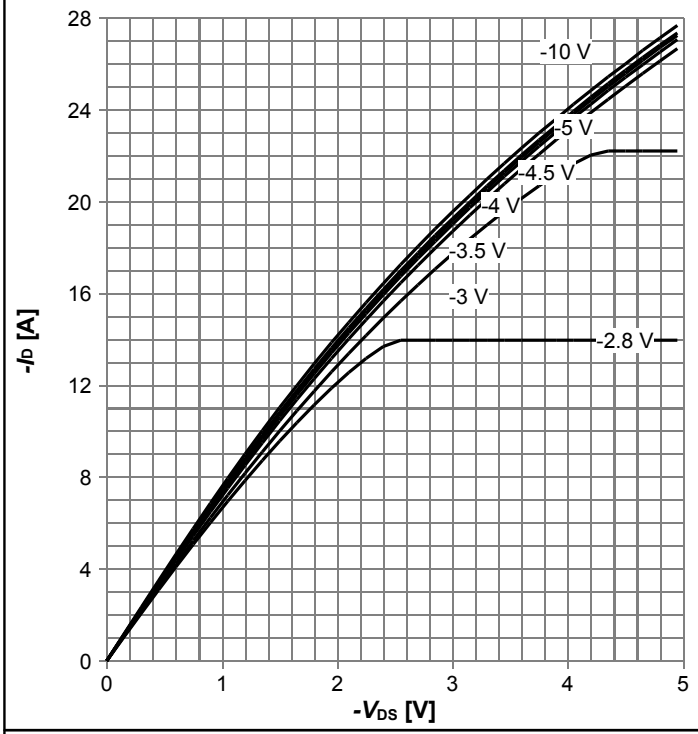
$I_D=f(V_{DS})$; T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



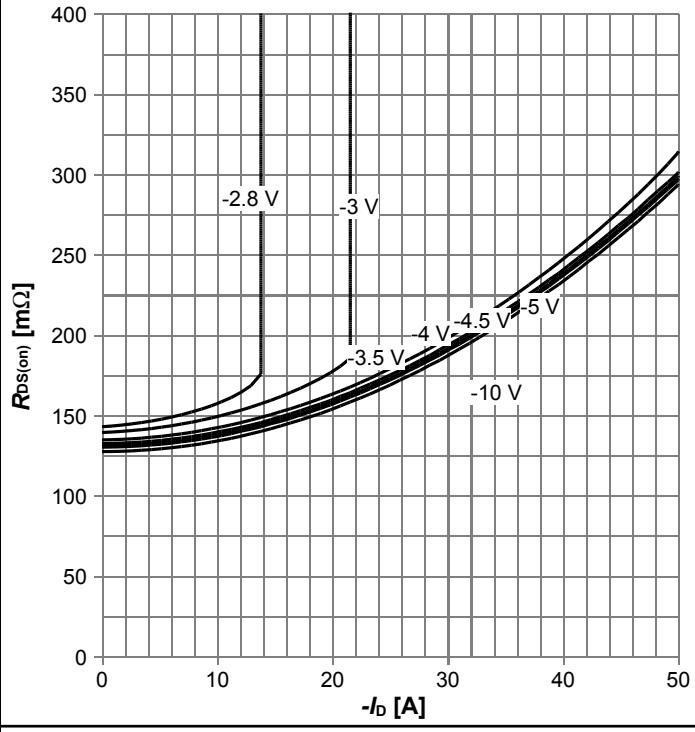
$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

Diagram 5: Typ. output characteristics



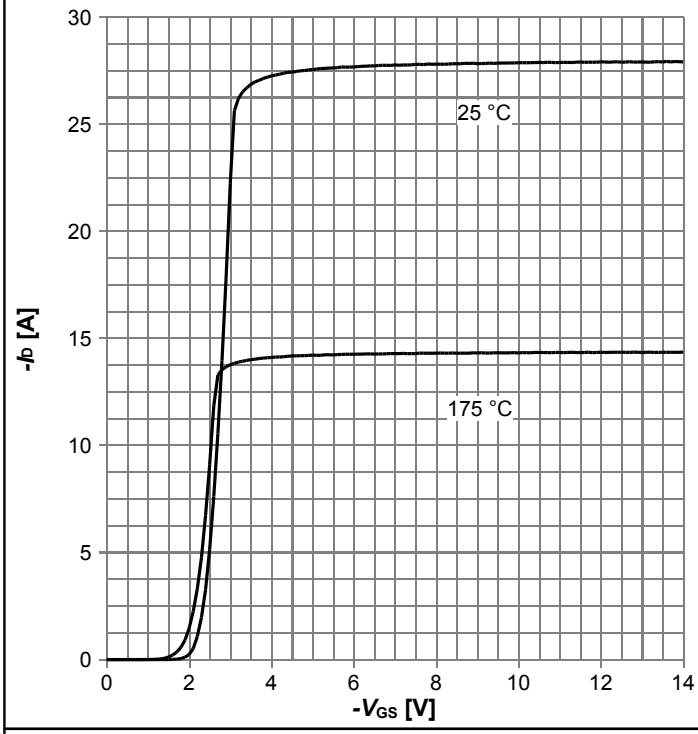
I_D=f(V_{DS}), T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



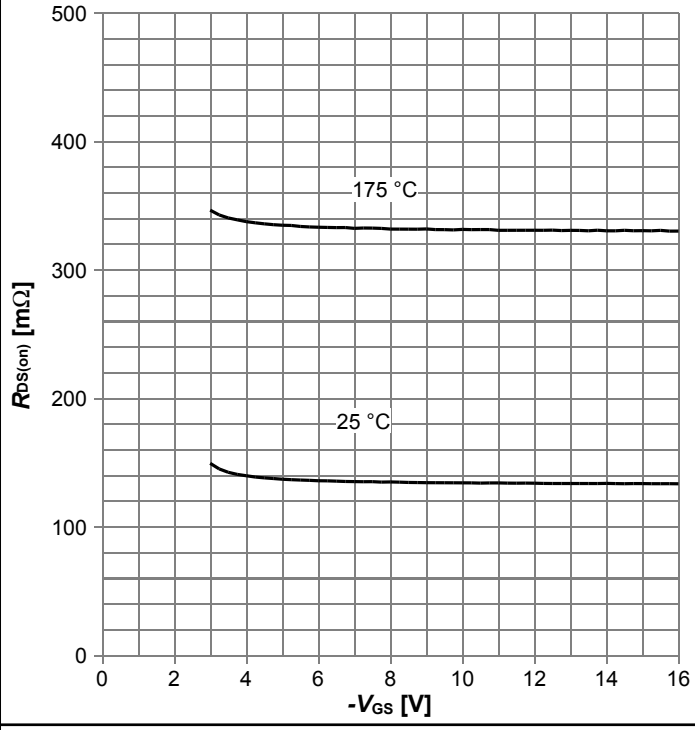
$R_{DS(on)}$=f(I_D), T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



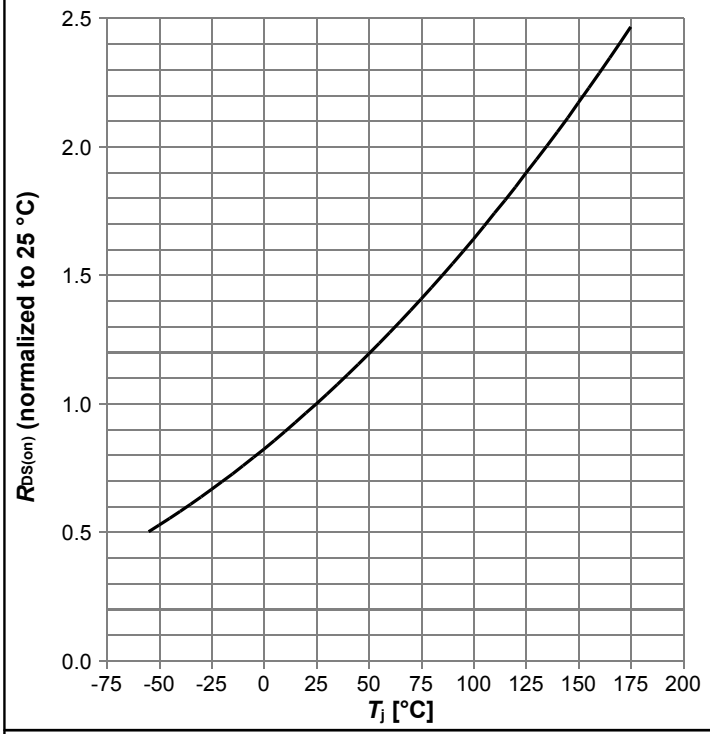
I_D=f(V_{GS}), |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



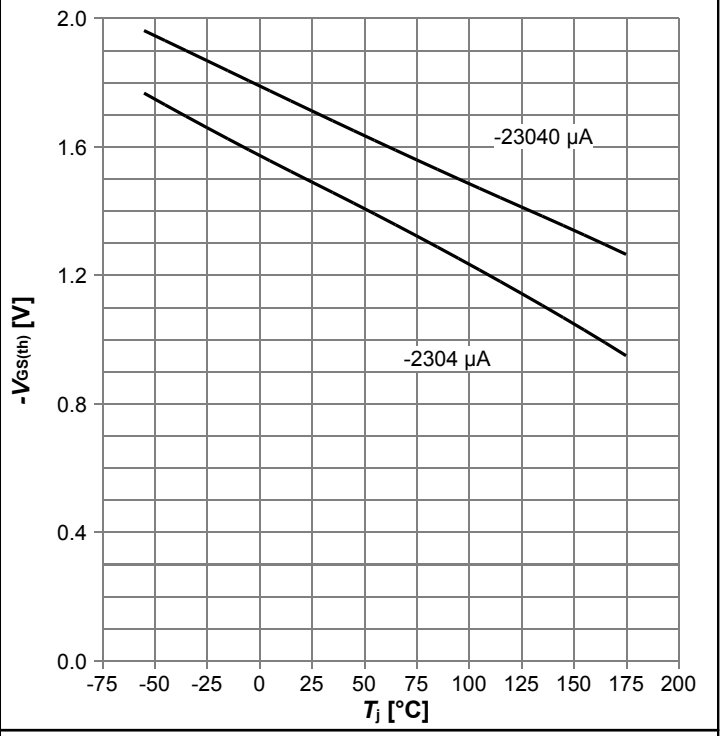
$R_{DS(on)}$=f(V_{GS}), I_D=-10 A; parameter: T_j

Diagram 9: Normalized drain-source on resistance



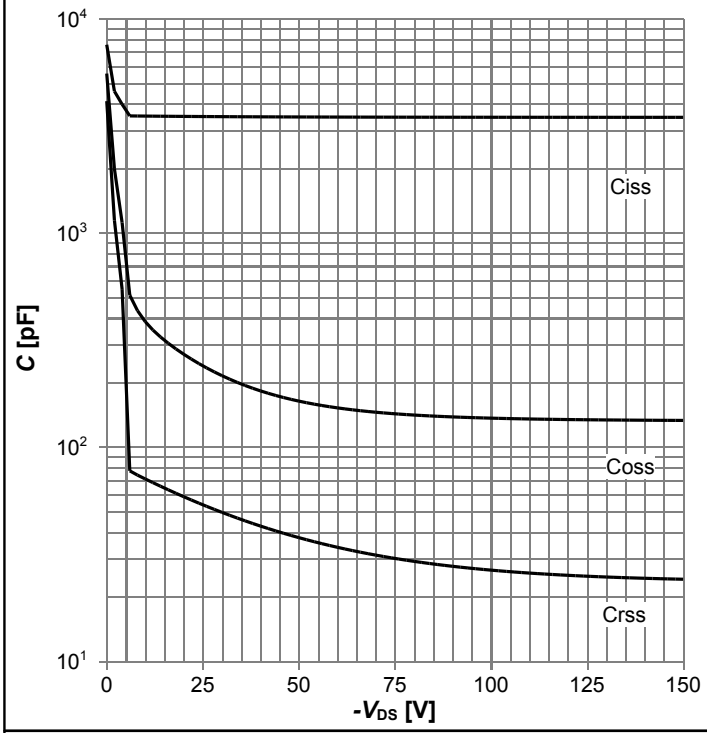
$R_{DS(on)}$=f(T_j), I_D=-10 A, V_{GS}=-10 V

Diagram 10: Typ. gate threshold voltage



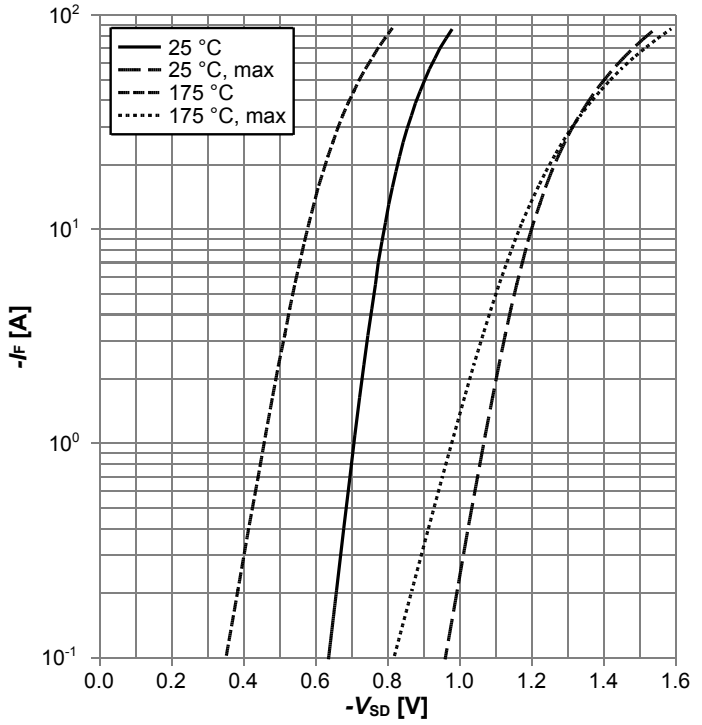
$V_{GS(th}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

Diagram 11: Typ. capacitances



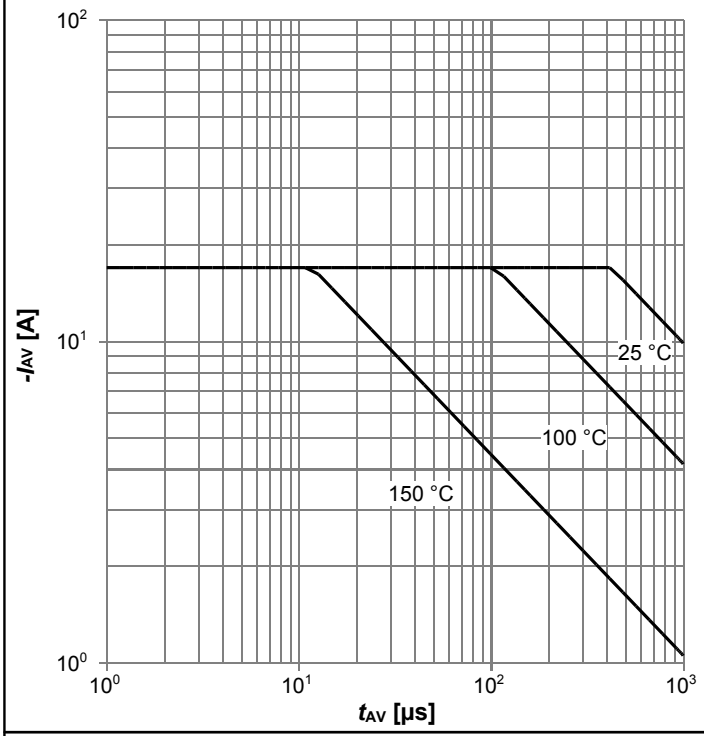
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode



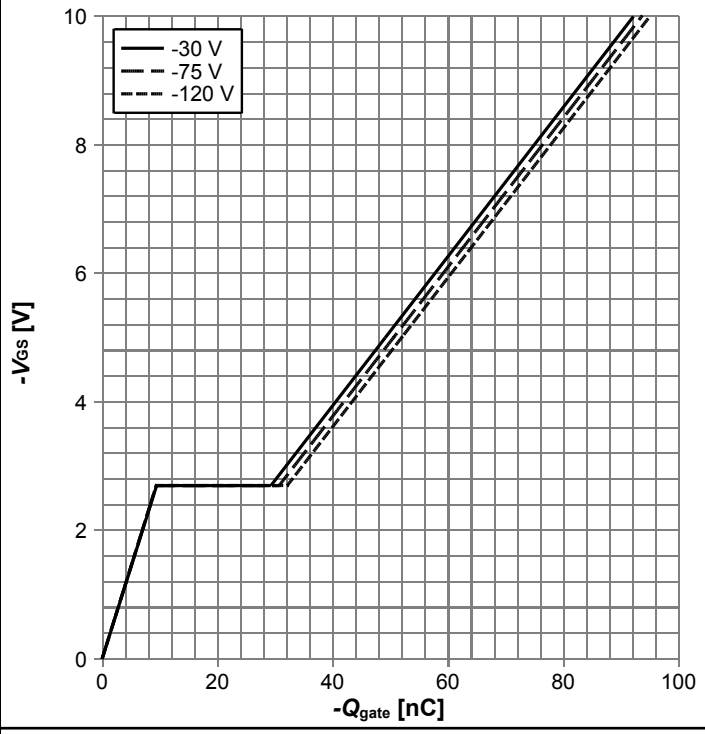
I_F=f(V_{SD}); parameter: T_j

Diagram 13: Avalanche characteristics



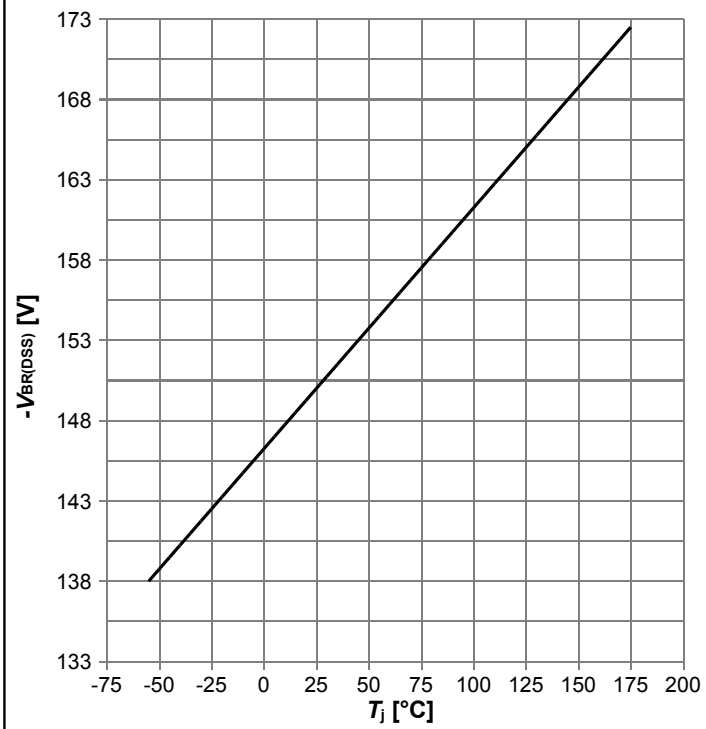
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



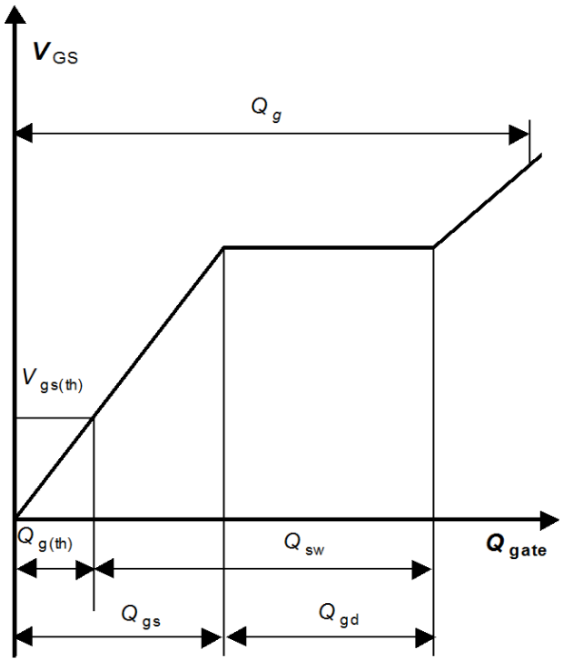
$V_{GS}=f(Q_{gate})$, I_D=-10 A pulsed, T_j=25 °C; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

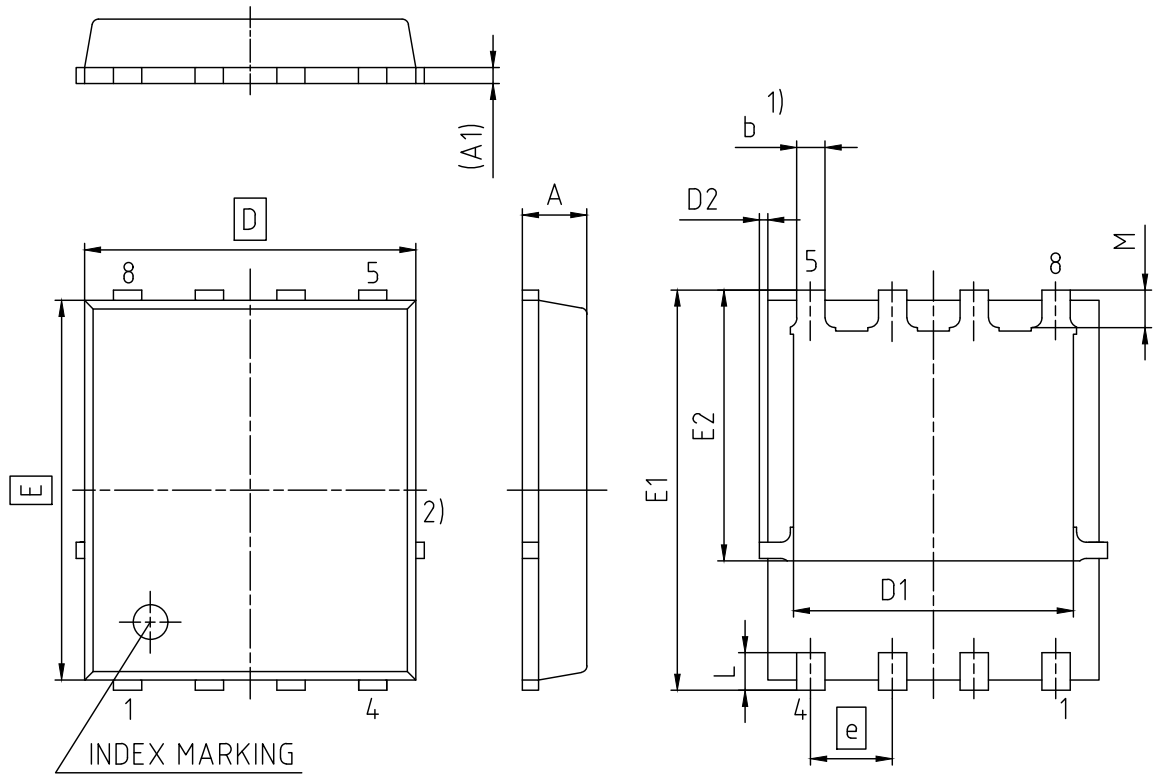


$V_{BR(DSS)}=f(T_j)$; I_D=-250 µA

Diagram Gate charge waveforms



5 Package Outlines



1) EXCLUDING MOLD FLASH
2) REMOVAL ON MOLD GATE
INTRUSION 0.1 MM
PROTRUSION 0.1 MM
LEAD LENGTH UP TO ANTI FLASH LINE
ALL METAL SURFACES ARE PLATED, EXCEPT AREA OF CUT

DIMENSION	MILLIMETERS	
	MIN.	MAX.
A	0.90	1.20
A1	0.15	0.35
b	0.34	0.54
D	4.80	5.35
D1	3.90	4.40
D2	0.00	0.22
E	5.70	6.10
E1	5.90	6.42
E2	3.88	4.31
e	1.27	
L	0.45	0.71
M	0.45	0.69

DOCUMENT NO.	Z8B00003332
REVISION	08
SCALE 10:1	0 1 2 3mm
EUROPEAN PROJECTION	
ISSUE DATE	05.11.2019

Figure 1 Outline PG-TDSON-8, dimensions in mm

Revision History

ISC16DP15LM

Revision: 2022-10-07, Rev. 2.0

Previous Revision		
Revision	Date	Subjects (major changes since last revision)
2.0	2022-10-07	Release of final version

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