# 1.5A Fast-Response High-Accuracy LDO Linear Regulator with Enable

**Check for Samples: LP38855**

## FEATURES

- **Standard $V_{OUT}$ Values of 0.8V and 1.2V**
- **Wide $V_{BIAS}$ Supply Operating Range of 3.0V to 5.5V**
- **Stable with 10 µF Ceramic Capacitors**
- **Dropout Voltage of 130 mV (Typical) at 1.5A Load Current**
- **Precision Output Voltage Across All Line and Load Conditions:**
  - **±1.0% for $T_J$ = 25°C**
  - **±2.0% for 0°C ≤ $T_J$ ≤ +125°C**
  - **±3.0% for -40°C ≤ $T_J$ ≤ +125°C**
- **Over-Temperature and Over-Current Protection**
- **Available in 5 Lead TO-220 and DDPAK/TO-263 Packages**
- **Custom $V_{OUT}$ Values between 0.8V and 1.2V are Available**
- **-40°C to +125°C Operating Temperature Range**

## APPLICATIONS

- **ASIC Power Supplies In:**
  - **Desktops, Notebooks, and Graphics Cards, Servers**
  - **Gaming Set Top Boxes, Printers and Copiers**
- **Server Core and I/O Supplies**
- **DSP and FPGA Power Supplies**
- **SMPS Post-Regulator**

## DESCRIPTION

The LP38855 is a high-current, fast-response regulator which can maintain output voltage regulation with an extremely low input to output voltage drop. Fabricated on a CMOS process, the device operates from two input voltages: $V_{BIAS}$ provides power for the internal bias and control circuits, as well as drive for the gate of the N-MOS power transistor, while $V_{IN}$ supplies power to the load. The use of an external bias rail allows the part to operate from ultra low $V_{IN}$ voltages. Unlike bipolar regulators, the CMOS architecture consumes extremely low quiescent current at any output load current. The use of an N-MOS power transistor results in wide bandwidth, yet minimum external capacitance is required to maintain loop stability.

The fast transient response of this device makes it suitable for use in powering DSP, Microcontroller Core voltages and Switch Mode Power Supply post regulators. The LP38855 is available in TO-220 and DDPAK/TO-263 5-Lead packages.

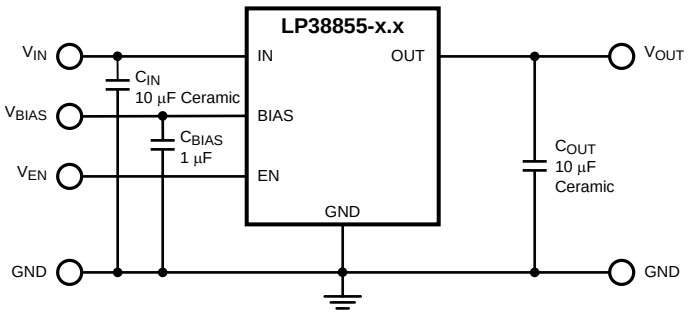
**Dropout Voltage:** 130 mV (typical) at 1.5A load current.

**Low Ground Pin Current:** 10 mA (typical) at 1.5A load current.

**Shutdown Current:** 1 µA (typical) $I_{IN(GND)}$ when EN pin is low.

**Precision Output Voltage:** ±1.0% for $T_J$ = 25°C and ±2.0% for 0°C ≤ $T_J$ ≤ +125°C, across all line and load conditions

### Typical Application Circuit




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## Connection Diagrams

Top View

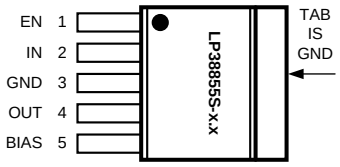



**Figure 1. DDPAK/TO-263 Package**
**See Package Number KTT0005B**

Top View

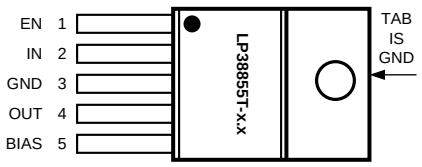



**Figure 2. TO-220 Package**
**See Package Number NDH0005D**

**PIN DESCRIPTIONS**
**TO-220–5 and DDPAK/TO-263–5 Packages**

| Pin # | Pin Symbol | Pin Description |
|---|---|---|
| 1 | EN | The device Enable pin. |
| 2 | IN | The unregulated input voltage pin |
| 3 | GND | Ground |
| 4 | OUT | The regulated output voltage pin |
| 5 | BIAS | The supply for the internal control and reference circuitry |
| TAB | TAB | The TAB is a thermal connection that is physically attached to the backside of the die, and is used as a thermal heat-sink connection. See the Application Information section for details |



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings[1][2]

| | | |
|---|---|---|
| Storage Temperature Range | | −65°C to +150°C |
| Lead Temperature | Soldering, 5 seconds | 260°C |
| ESD Rating | Human Body Model[3] | ±2 kV |
| Power Dissipation[4] | | Internally Limited |
| $V_{IN}$ Supply Voltage (Survival) | | −0.3V to +6.0V |
| $V_{BIAS}$ Supply Voltage (Survival) | | −0.3V to +6.0V |
| $V_{EN}$ Voltage (Survival) | | −0.3V to +6.0V |
| $V_{OUT}$ Voltage (Survival) | | −0.3V to +6.0V |
| $I_{OUT}$ Current (Survival) | | Internally Limited |
| Junction Temperature | | −40°C to +150°C |

(1) Absolute maximum ratings indicate limits beyond which damage to the component may occur. Operating ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications, see Electrical Characteristics. Specifications do not apply when operating the device outside of its rated operating conditions.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The Human Body Model (HBM) is a 100 pF capacitor discharged through a 1.5k resistor into each pin. Test method is per JESD22-A114. The HBM rating for device pin 1 (EN) is ±1.5 kV.
(4) Device power dissipation must be de-rated based on device power dissipation ($T_D$), ambient temperature ($T_A$), and package junction to ambient thermal resistance ($\theta_{JA}$). Additional heat-sinking may be required to ensure that the device junction temperature ($T_J$) does not exceed the maximum operating rating. See the Application Information section for details.


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## Operating Ratings(1)

| | |
|---|---|
| $V_{IN}$ Supply Voltage | ($V_{OUT}$ + $V_{DO}$) to $V_{BIAS}$ |
| $V_{BIAS}$ Supply Voltage | 3.0V to 5.5V |
| $V_{EN}$ Enable Input Voltage | 0.0V to $V_{BIAS}$ |
| $I_{OUT}$ | 0 mA to 1.5A |
| Junction Temperature Range(2) | −40°C to +125°C |

(1) Absolute maximum ratings indicate limits beyond which damage to the component may occur. Operating ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications, see Electrical Characteristics. Specifications do not apply when operating the device outside of its rated operating conditions.
(2) Device power dissipation must be de-rated based on device power dissipation ($T_D$), ambient temperature ($T_A$), and package junction to ambient thermal resistance ($\theta_{JA}$). Additional heat-sinking may be required to ensure that the device junction temperature ($T_J$) does not exceed the maximum operating rating. See the Application Information section for details.

## Electrical Characteristics

Unless otherwise specified: $V_{IN} = V_{OUT(NOM)} + 1V$, $V_{BIAS} = 3.0V$, $I_{OUT} = 10$ mA, $C_{IN} = C_{OUT} = 10$ µF, $C_{BIAS} = 1$µF, $V_{EN} = V_{BIAS}$. Limits in standard type are for $T_J = 25°C$ only; limits in **boldface type** apply over the junction temperature ($T_J$) range of -40°C to +125°C. Minimum and Maximum limits are ensured through test, design, or statistical correlation. Typical values represent the most likely parametric norm at $T_J = 25°C$, and are provided for reference purposes only.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{OUT}$ | Output Voltage Tolerance | $V_{OUT(NOM)} + 1V \le V_{IN} \le V_{BIAS}$, $3.0V \le V_{BIAS} \le 5.5V$, $10\text{ mA} \le I_{OUT} \le 1.5A$ | -1.0<br>**-3.0** | 0 | +1.0<br>**+3.0** | % |
| | | $V_{OUT(NOM)} + 1V \le V_{IN} \le V_{BIAS}$, $3.0V \le V_{BIAS} \le 5.5V$, $10\text{ mA} \le I_{OUT} \le 1.5A$, $0°C \le T_J \le 125°C$ | -2.0 | 0 | +2.0 | |
| $\Delta V_{OUT}/\Delta V_{IN}$ | Line Regulation, $V_{IN}$(1) | $V_{OUT(NOM)} + 1V \le V_{IN} \le V_{BIAS}$ | - | 0.04 | - | %/V |
| $\Delta V_{OUT}/\Delta V_{BIAS}$ | Line Regulation, $V_{BIAS}$(1) | $3.0V \le V_{BIAS} \le 5.5V$ | - | 0.10 | - | %/V |
| $\Delta V_{OUT}/\Delta I_{OUT}$ | Output Voltage Load Regulation(2) | $10\text{ mA} \le I_{OUT} \le 1.5A$ | - | 0.2 | - | %/A |
| $V_{DO}$ | Dropout Voltage, $V_{IN} - V_{OUT}$(3) | $I_{OUT} = 1.5A$ | - | 130 | 165<br>**180** | mV |
| $I_{GND(IN)}$ | Ground Pin Current Drawn from $V_{IN}$ Supply | LP38855-0.8<br>$10\text{ mA} \le I_{OUT} \le 1.5A$ | - | 7.0 | 8.5<br>**9.0** | mA |
| | | LP38855-1.2<br>$10\text{ mA} \le I_{OUT} \le 1.5A$ | - | 11 | 12<br>**15** | |
| | | $V_{EN} \le 0.5V$ | - | 1.0 | 10<br>**300** | µA |
| $I_{GND(BIAS)}$ | Ground Pin Current Drawn from $V_{BIAS}$ Supply | $10\text{ mA} \le I_{OUT} \le 1.5A$ | - | 3.0 | 3.8<br>**4.5** | mA |
| | | $V_{EN} \le 0.5V$ | - | 100 | 170<br>**200** | µA |
| UVLO | Under-Voltage Lock-Out Threshold | $V_{BIAS}$ rising until device is functional | 2.20<br>**2.00** | 2.45 | 2.70<br>**2.90** | V |
| $UVLO_{(HYS)}$ | Under-Voltage Lock-Out Hysteresis | $V_{BIAS}$ falling from UVLO threshold until device is non-functional | 60<br>**50** | 150 | 300<br>**350** | mV |
| $I_{SC}$ | Output Short-Circuit Current | $V_{IN} = V_{OUT(NOM)} + 1V$, $V_{BIAS} = 3.0V$, $V_{OUT} = 0.0V$ | - | 4.5 | - | A |

(1) Output voltage line regulation is defined as the change in output voltage from nominal value resulting from a change in input voltage.
(2) Output voltage load regulation is defined as the change in output voltage from nominal value as the load current increases from no load to full load.
(3) Dropout voltage is defined the as input to output voltage differential ($V_{IN}$ - $V_{OUT}$) where the input voltage is low enough to cause the output voltage to drop 2% from the nominal value.

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## Electrical Characteristics (continued)

Unless otherwise specified: $V_{IN} = V_{OUT(NOM)} + 1V$, $V_{BIAS} = 3.0V$, $I_{OUT} = 10$ mA, $C_{IN} = C_{OUT} = 10$ µF, $C_{BIAS} = 1$µF, $V_{EN} = V_{BIAS}$. Limits in standard type are for $T_J = 25°C$ only; limits in **boldface type** apply over the junction temperature ($T_J$) range of -40°C to +125°C. Minimum and Maximum limits are ensured through test, design, or statistical correlation. Typical values represent the most likely parametric norm at $T_J = 25°C$, and are provided for reference purposes only.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **ENABLE Pin** | | | | | | |
| $I_{EN}$ | ENABLE pin Current | $V_{EN} = V_{BIAS}$ | - | 0.01 | - | µA |
| | | $V_{EN} = 0.0V$, $V_{BIAS} = 5.5V$ | -19<br>**-13** | -30 | -40<br>**-51** | |
| $V_{EN(ON)}$ | Enable Voltage Threshold | $V_{EN}$ rising until Output = ON | 1.00<br>**0.90** | 1.25 | 1.50<br>**1.55** | V |
| $V_{EN(HYS)}$ | Enable Voltage Hysteresis | $V_{EN}$ falling from $V_{EN(ON)}$ until Output = OFF | 50<br>**30** | 100 | 150<br>**200** | mV |
| $t_{OFF}$ | Turn-OFF Delay Time | $R_{LOAD} \times C_{OUT} << t_{OFF}$ | - | 20 | - | µs |
| $t_{ON}$ | Turn-ON Delay Time | $R_{LOAD} \times C_{OUT} << t_{ON}$ | - | 15 | - | |
| **AC Parameters** | | | | | | |
| PSRR ($V_{IN}$) | Ripple Rejection for $V_{IN}$ Input Voltage | $V_{IN} = V_{OUT}$ +1V, f = 120 Hz | - | 80 | - | dB |
| | | $V_{IN} = V_{OUT}$ + 1V, f = 1 kHz | - | 65 | - | |
| PSRR ($V_{BIAS}$) | Ripple Rejection for $V_{BIAS}$ Voltage | $V_{BIAS} = V_{OUT}$ + 3V, f = 120 Hz | - | 58 | - | dB |
| | | $V_{BIAS} = V_{OUT}$ + 3V, f = 1 kHz | - | 58 | - | |
| $e_n$ | Output Noise Density | f = 120 Hz | - | 1 | - | $\mu V/\sqrt{Hz}$ |
| | Output Noise Voltage | BW = 10 Hz − 100 kHz | - | 150 | - | $\mu V_{RMS}$ |
| | | BW = 300 Hz − 300 kHz | - | 90 | - | |
| **Thermal Parameters** | | | | | | |
| $T_{SD}$ | Thermal Shutdown Junction Temperature | | - | 160 | - | °C |
| $T_{SD(HYS)}$ | Thermal Shutdown Hysteresis | | - | 10 | - | |
| $\theta_{JA}$ | Thermal Resistance, Junction to Ambient(4) | TO-220-5 | - | 60 | - | °C/W |
| | | DDPAK/TO-263-5 | - | 60 | - | |
| $\theta_{JC}$ | Thermal Resistance, Junction to Case(4) | TO-220-5 | - | 3 | - | |
| | | DDPAK/TO-263-5 | - | 3 | - | |

(4) Device power dissipation must be de-rated based on device power dissipation ($T_D$), ambient temperature ($T_A$), and package junction to ambient thermal resistance ($\theta_{JA}$). Additional heat-sinking may be required to ensure that the device junction temperature ($T_J$) does not exceed the maximum operating rating. See the Application Information section for details.


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## Typical Performance Characteristics

Unless otherwise specified: $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(NOM)}$ + 1V, $V_{BIAS}$ = 3.0V, $I_{OUT}$ = 10 mA, $C_{IN}$ = $C_{OUT}$ = 10 µF Ceramic, $C_{BIAS}$ = 1 µF Ceramic, $V_{EN}$ = $V_{BIAS}$.

**$V_{BIAS}$ Ground Pin Current ($I_{GND(BIAS)}$) vs $V_{BIAS}$**

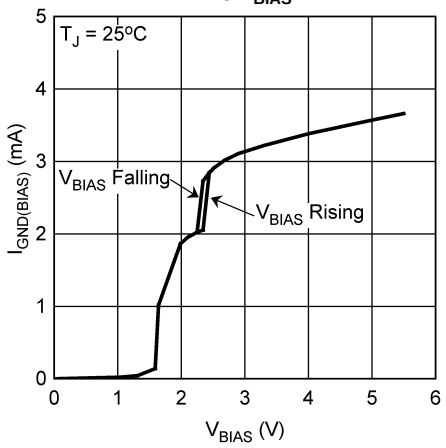



**Figure 3.**

**$V_{BIAS}$ Ground Pin Current ($I_{GND(BIAS)}$) vs Temperature**

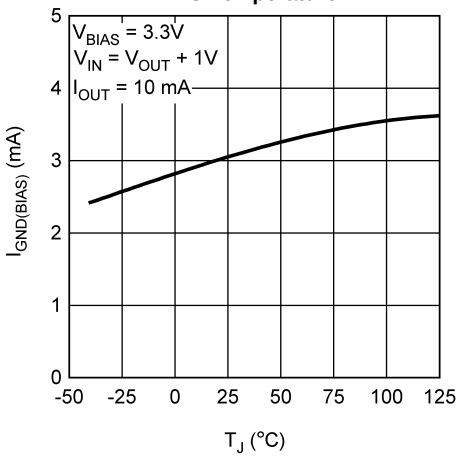



**Figure 4.**

**$V_{IN}$ Ground Pin Current ($I_{GND(IN)}$) vs Temperature**

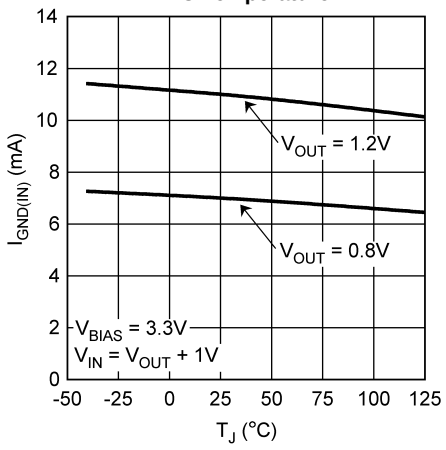



**Figure 5.**

**Load Regulation vs Temperature**

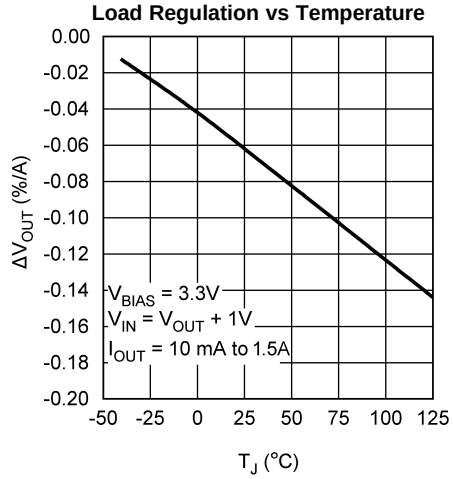



**Figure 6.**

**Dropout Voltage ($V_{DO}$) vs Temperature**

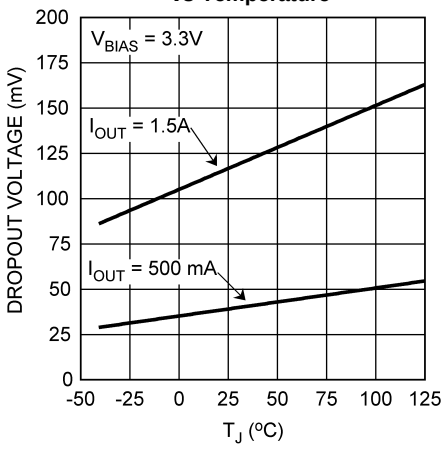



**Figure 7.**

**Output Current Limit ($I_{SC}$) vs Temperature**

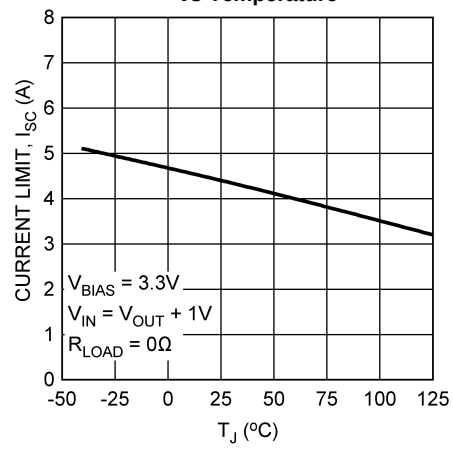



**Figure 8.**

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## Typical Performance Characteristics (continued)

Unless otherwise specified: $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(NOM)}$ + 1V, $V_{BIAS}$ = 3.0V, $I_{OUT}$ = 10 mA, $C_{IN}$ = $C_{OUT}$ = 10 µF Ceramic, $C_{BIAS}$ = 1 µF Ceramic, $V_{EN}$ = $V_{BIAS}$.

**$V_{OUT}$ vs Temperature**

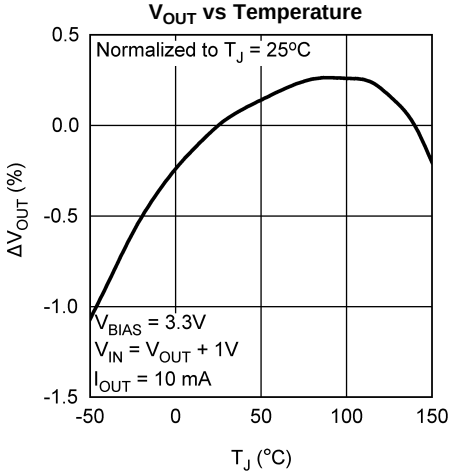



**Figure 9.**

**UVLO Thresholds vs Temperature**

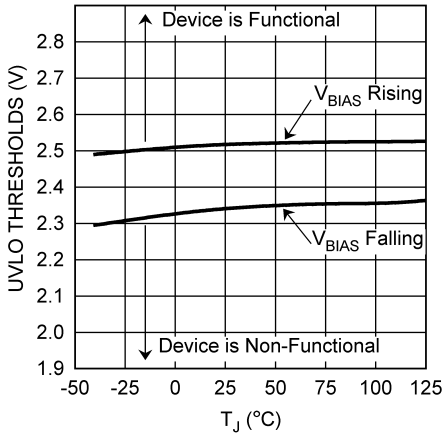



**Figure 10.**

**Enable Thresholds ($V_{EN}$) vs Temperature**

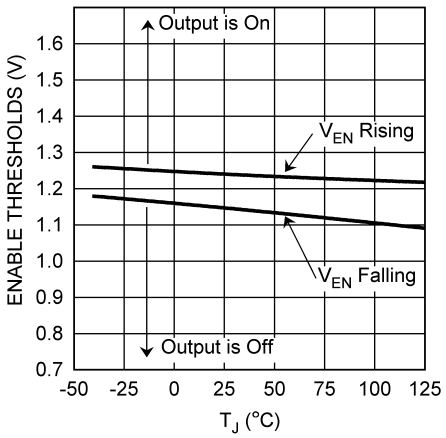



**Figure 11.**

**Enable Pull-Down Current ($I_{EN}$) vs Temperature**

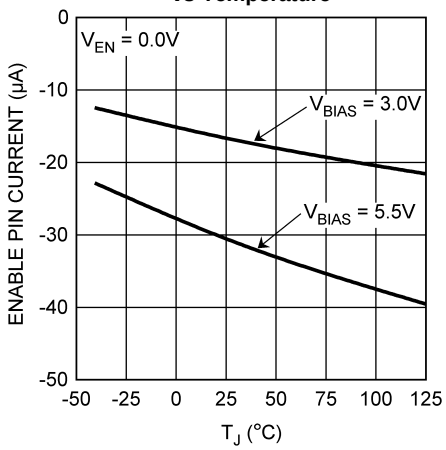



**Figure 12.**

**Enable Pull-Up Resistor ($r_{EN}$) vs Temperature**

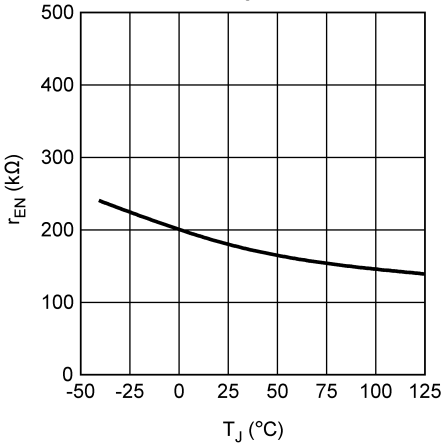



**Figure 13.**

**$V_{IN}$ Line Transient Response**

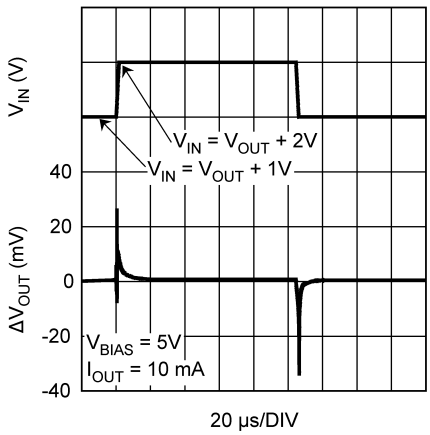



**Figure 14.**


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## Typical Performance Characteristics (continued)

Unless otherwise specified: $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(NOM)}$ + 1V, $V_{BIAS}$ = 3.0V, $I_{OUT}$ = 10 mA, $C_{IN}$ = $C_{OUT}$ = 10 µF Ceramic, $C_{BIAS}$ = 1 µF Ceramic, $V_{EN}$ = $V_{BIAS}$.

**$V_{IN}$ Line Transient Response**

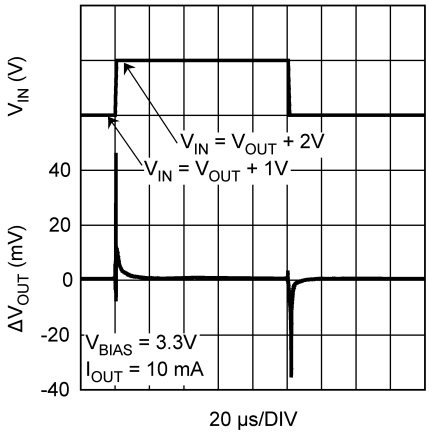



**Figure 15.**

**$V_{BIAS}$ Line Transient Response**

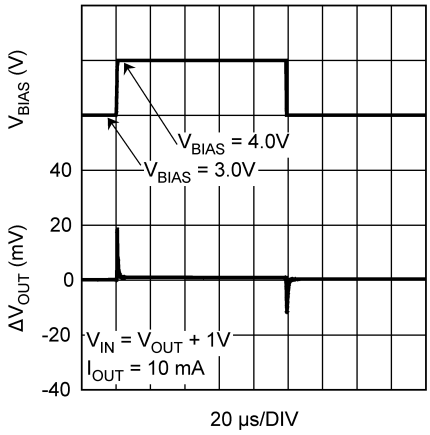



**Figure 16.**

**$V_{BIAS}$ Line Transient Response**

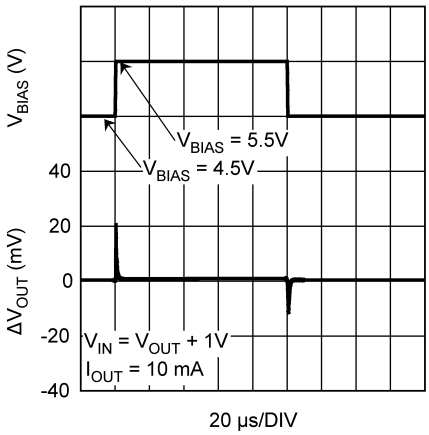



**Figure 17.**

**Load Transient Response, $C_{OUT}$ = 10 µF Ceramic**

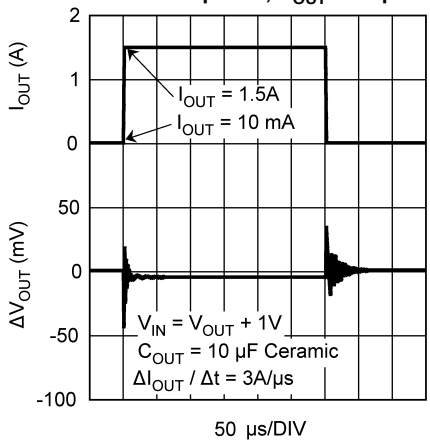



**Figure 18.**

**Load Transient Respose, $C_{OUT}$ = 10 µF Ceramic**

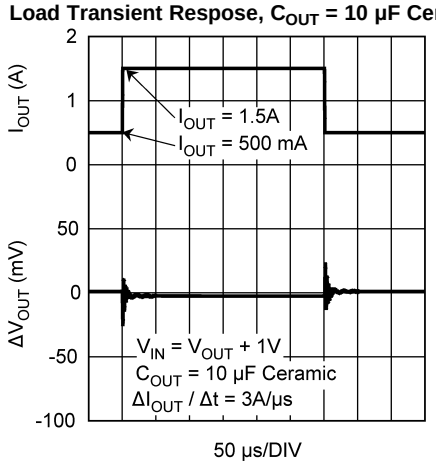



**Figure 19.**

**Load Transient Response, $C_{OUT}$ = 100 µF Ceramic**

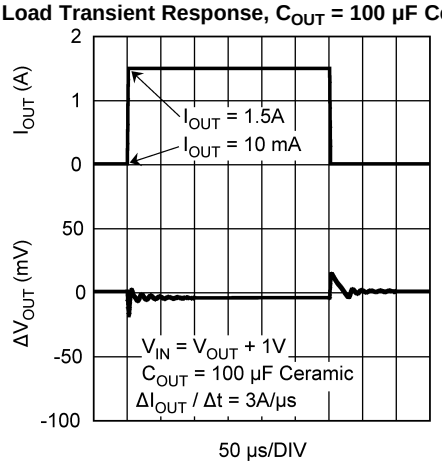



**Figure 20.**

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## Typical Performance Characteristics (continued)

Unless otherwise specified: $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(NOM)}$ + 1V, $V_{BIAS}$ = 3.0V, $I_{OUT}$ = 10 mA, $C_{IN}$ = $C_{OUT}$ = 10 µF Ceramic, $C_{BIAS}$ = 1 µF Ceramic, $V_{EN}$ = $V_{BIAS}$.

**Load Transient Response, $C_{OUT}$ = 100 µF Ceramic**

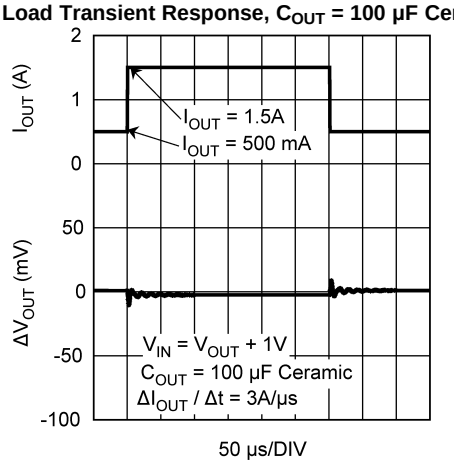



**Figure 21.**

**Load Transient Response, $C_{OUT}$ = 100 µF Tantalum**

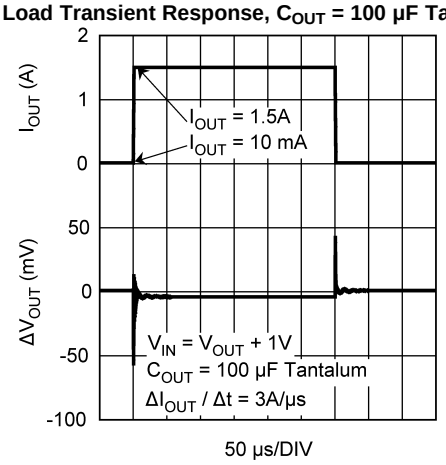



**Figure 22.**

**Load Transient Response, $C_{OUT}$ = 100 µF Tantalum**

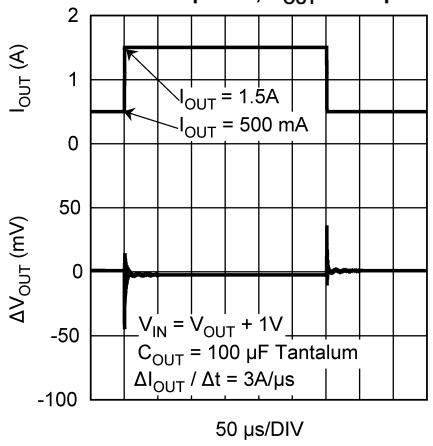



**Figure 23.**

**$V_{BIAS}$ PSRR**

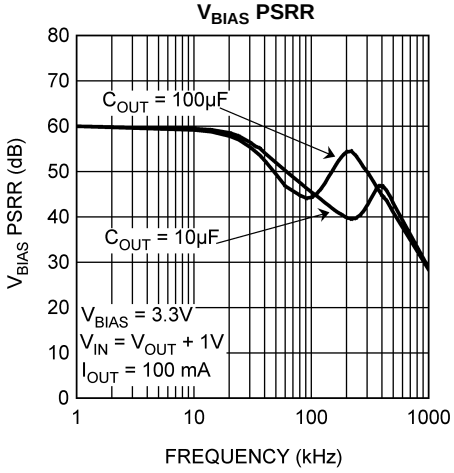



**Figure 24.**

**$V_{IN}$ PSRR**

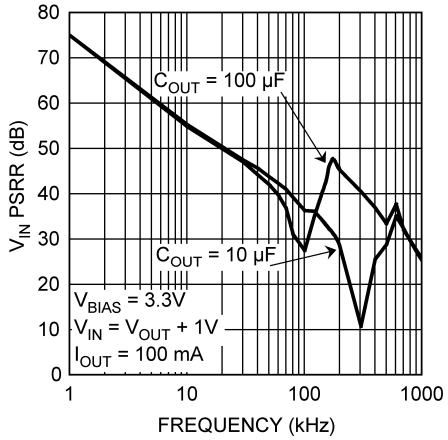



**Figure 25.**

**Output Noise**

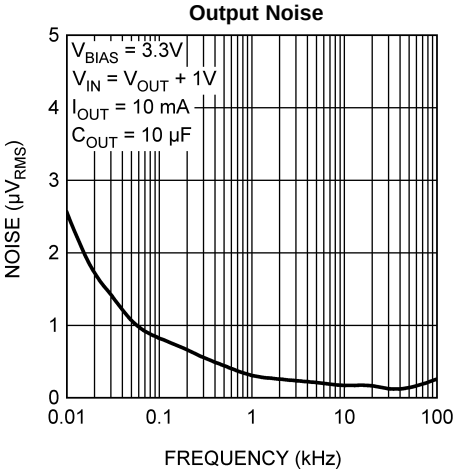
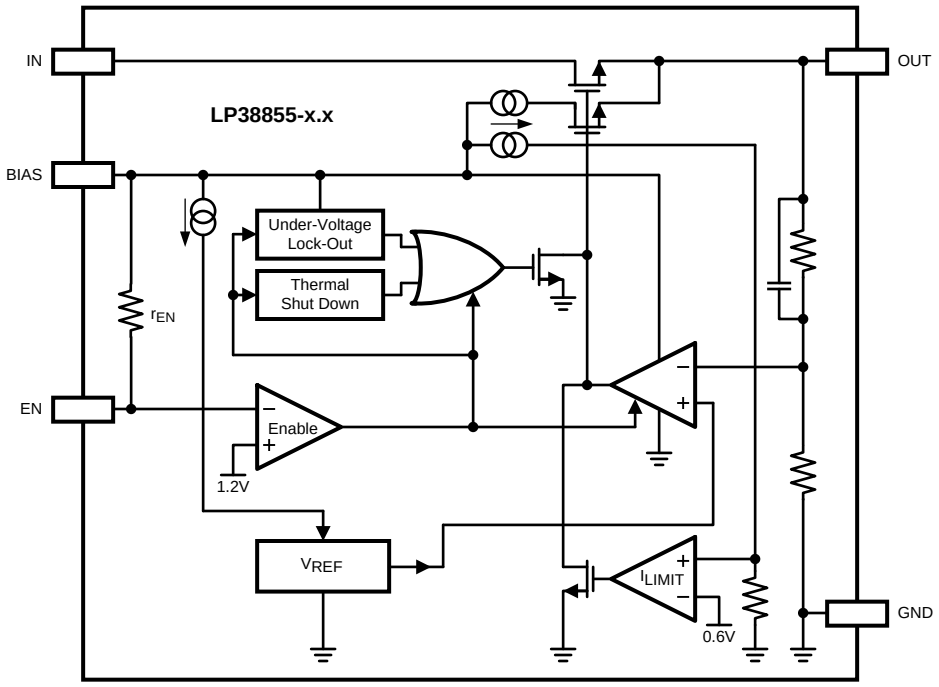



**Figure 26.**


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## Block Diagram




## APPLICATION INFORMATION

### EXTERNAL CAPACITORS

To assure regulator stability, capacitors are required on the input, output and bias pins as shown in the Typical Application Circuit.

#### Output Capacitor

A minimum output capacitance of 10 µF, ceramic, is required for stability. The amount of output capacitance can be increased without limit. The output capacitor must be located less than 1 cm from the output pin of the IC and returned to the device ground pin with a clean analog ground.

Only high quality ceramic types such as X5R or X7R should be used, as the Z5U and Y5F types do not provide sufficient capacitance over temperature.

Tantalum capacitors will also provide stable operation across the entire operating temperature range. However, the effects of ESR may provide variations in the output voltage during fast load transients. Using the minimum recommended 10 µF ceramic capacitor at the output will allow unlimited capacitance, Tantalum and/or Aluminum, to be added in parallel.

#### Input Capacitor

The input capacitor must be at least 10 µF, but can be increased without limit. It's purpose is to provide a low source impedance for the regulator input. A ceramic capacitor, X5R or X7R, is recommended.

Tantalum capacitors may also be used at the input pin. There is no specific ESR limitation on the input capacitor (the lower, the better).

Aluminum electrolytic capacitors can be used, but are not recommended as their ESR increases very quickly at cold temperatures. They are not recommended for any application where the ambient temperature falls below 0°C.

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### Bias Capacitor

The capacitor on the bias pin must be at least 1 µF. It can be any good quality capacitor (ceramic is recommended).

## INPUT VOLTAGE

The input voltage ($V_{IN}$) is the high current external voltage rail that will be regulated down to a lower voltage, which is applied to the load. The input voltage must be at least $V_{OUT}$ + $V_{DO}$, and no higher than whatever value is used for $V_{BIAS}$.

## BIAS VOLTAGE

The bias voltage ($V_{BIAS}$) is a low current external voltage rail required to bias the control circuitry and provide gate drive for the N-FET pass transistor. The bias voltage must be in the range of 3.0V to 5.5V to ensure proper operation of the device.

## UNDER VOLTAGE LOCKOUT

The bias voltage is monitored by a circuit which prevents the device from functioning when the bias voltage is below the Under-Voltage Lock-Out (UVLO) threshold of approximately 2.45V.

As the bias voltage rises above the UVLO threshold the device control circuitry become active. There is approximately 150 mV of hysteresis built into the UVLO threshold to provide noise immunity.

When the bias voltage is between the UVLO threshold and the Minimum Operating Rating value of 3.0V the device will be functional, but the operating parameters will not be within the specified limits.

## SUPPLY SEQUENCING

There is no requirement for the order that $V_{IN}$ or $V_{BIAS}$ are applied or removed. However, the output voltage cannot be ensured until both $V_{IN}$ and $V_{BIAS}$ are within the range of specified operating values.

If used in a dual-supply system where the regulator load is returned to a negative supply, the output pin must be diode clamped to ground. A Schottky diode is recommend for this diode clamp.

## REVERSE VOLTAGE

A reverse voltage condition will exist when the voltage at the output pin is higher than the voltage at the input pin. Typically this will happen when $V_{IN}$ is abruptly taken low and $C_{OUT}$ continues to hold a sufficient charge such that the input to output voltage becomes reversed.

The NMOS pass element, by design, contains no body diode. This means that, as long as the gate of the pass element is not driven, there will not be any reverse current flow through the pass element during a reverse voltage event. The gate of the pass element is not driven when $V_{BIAS}$ is below the UVLO threshold, or the EN pin is held low.

When $V_{BIAS}$ is above the UVLO threshold, and the EN pin is above the $V_{EN(ON)}$ threshold, the control circuitry is active and will attempt to regulate the output voltage. Since the input voltage is less than the output voltage the control circuit will drive the gate of the pass element to the full $V_{BIAS}$ potential when the output voltage begins to fall. In this condition, reverse current will flow from the output pin to the input pin, limited only by the $R_{DS(ON)}$ of the pass element and the output to input voltage differential. Discharging an output capacitor up to 1000 µF in this manner will not damage the device as the current will decay rapidly. However, continuous reverse current should be avoided.


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## ENABLE OPERATION

The Enable pin (EN) provides a mechanism to enable, or disable, the regulator output stage. The Enable pin has an internal pull-up, through a typical 180 kΩ resistor, to $V_{BIAS}$.

If the Enable pin is actively driven, pulling the Enable pin above the $V_{EN}$ threshold of 1.25V (typical) will turn the regulator output on, while pulling the Enable pin below the $V_{EN}$ threshold will turn the regulator output off. There is approximately 100 mV of hysteresis built into the Enable threshold provide noise immunity.

If the Enable function is not needed this pin should be left open, or connected directly to $V_{BIAS}$. If the Enable pin is left open, stray capacitance on this pin must be minimized, otherwise the output turn-on will be delayed while the stray capacitance is charged through the internal resistance ($r_{EN}$).

## POWER DISSIPATION AND HEAT-SINKING

A heat-sink may be required depending on the maximum power dissipation and maximum ambient temperature of the application. Under all possible conditions, the junction temperature must be within the range specified under operating conditions.

The total power dissipation of the device is the sum of three different points of dissipation in the device.

The first part is the power that is dissipated in the NMOS pass element, and can be determined with the formula:

$$P_{D(PASS)} = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (1)$$

The second part is the power that is dissipated in the bias and control circuitry, and can be determined with the formula:

$$P_{D(BIAS)} = V_{BIAS} \times I_{GND(BIAS)}$$

where

- $I_{GND(BIAS)}$ is the portion of the operating ground current of the device that is related to $V_{BIAS}$ (2)

The third part is the power that is dissipated in portions of the output stage circuitry, and can be determined with the formula:

$$P_{D(IN)} = V_{IN} \times I_{GND(IN)}$$

where

- $I_{GND(IN)}$ is the portion of the operating ground current of the device that is related to $V_{IN}$ (3)

The total power dissipation is then:

$$P_D = P_{D(PASS)} + P_{D(BIAS)} + P_{D(IN)} \quad (4)$$

The maximum allowable junction temperature rise ($\Delta T_J$) depends on the maximum anticipated ambient temperature ($T_{A(MAX)}$) for the application, and the maximum allowable operating junction temperature ($T_{J(MAX)}$):

$$\Delta T_J = T_{J(MAX)} - T_{A(MAX)} \quad (5)$$

The maximum allowable value for junction to ambient Thermal Resistance, $\theta_{JA}$, can be calculated using the formula:

$$\theta_{JA} \leq \frac{\Delta T_J}{P_D} \quad (6)$$

### Heat-Sinking the TO-220 Package

The TO-220 package has a $\theta_{JA}$ rating of 60°C/W, and a $\theta_{JC}$ rating of 3°C/W. These ratings are for the package only, no additional heat-sinking, and with no airflow.

The thermal resistance of a TO-220 package can be reduced by attaching it to a heat-sink or a copper plane on a PC board. If a copper plane is to be used, the values of $\theta_{JA}$ will be same as shown in next section for DDPAK/TO-263 package.

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The heat-sink to be used in the application should have a heat-sink to ambient thermal resistance, $\theta_{HA}$:

$$\theta_{HA} \leq \theta_{JA} - (\theta_{CH} + \theta_{JC}) \quad (7)$$

where

- $\theta_{JA}$ is the required total thermal resistance from the junction to the ambient air
- $\theta_{CH}$ is the thermal resistance from the case to the surface of the heat sink
- $\theta_{JC}$ is the thermal resistance from the junction to the surface of the case

For this equation, $\theta_{JC}$ is about 3°C/W for a TO-220 package. The value for $\theta_{CH}$ depends on method of attachment, insulator, etc. $\theta_{CH}$ varies between 1.5°C/W to 2.5°C/W. Consult the heat-sink manufacturer datasheet for details and recommendations.

### Heat-Sinking the DDPAK/TO-263 Package

The DDPAK/TO-263 package has a $\theta_{JA}$ rating of 60°C/W, and a $\theta_{JC}$ rating of 3°C/W. These ratings are for the package only, no additional heat-sinking, and with no airflow.

The DDPAK/TO-263 package uses the copper plane on the PCB as a heat-sink. The tab of this package is soldered to the copper plane for heat-sinking. The graph below shows a curve for the $\theta_{JA}$ of TO-263 package for different copper area sizes, using a typical PCB with 1 ounce copper and no solder mask over the copper area for heat-sinking.

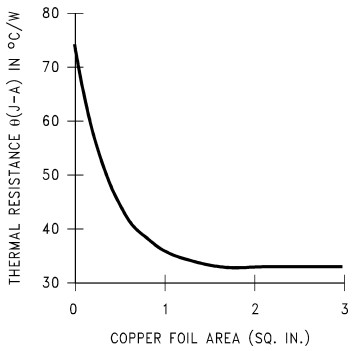



**Figure 27. $\theta_{JA}$ vs Copper (1 Ounce) Area for the DDPAK/TO-263 package**

As shown in Figure 27, increasing the copper area beyond 1 square inch produces very little improvement. The minimum value for $\theta_{JA}$ for the DDPAK/TO-263 package mounted to a PCB is 32°C/W.

Figure 28 shows the maximum allowable power dissipation for DDPAK/TO-263 packages for different ambient temperatures, assuming $\theta_{JA}$ is 35°C/W and the maximum junction temperature is 125°C.

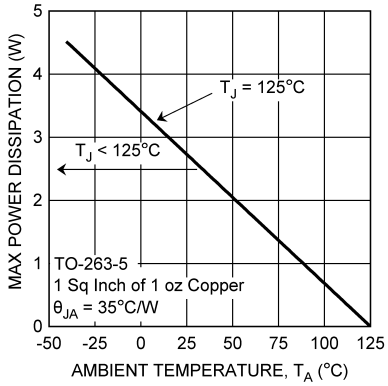



**Figure 28. Maximum Power Dissipation vs Ambient Temperature for DDPAK/TO-263 Package**


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## REVISION HISTORY

| Changes from Revision C (April 2013) to Revision D | Page |
|---|---|
| • Changed layout of National Data Sheet to TI format | 12 |

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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| LP38855S-1.2/NOPB | Active | Production | DDPAK/ TO-263 (KTT) \| 5 | 45 \| TUBE | ROHS Exempt | SN | Level-3-245C-168 HR | -40 to 125 | LP38855S -1.2 |
| LP38855S-1.2/NOPB.A | Active | Production | DDPAK/ TO-263 (KTT) \| 5 | 45 \| TUBE | ROHS Exempt | SN | Level-3-245C-168 HR | -40 to 125 | LP38855S -1.2 |
| LP38855SX-1.2/NOPB | Active | Production | DDPAK/ TO-263 (KTT) \| 5 | 500 \| LARGE T&R | ROHS Exempt | SN | Level-3-245C-168 HR | -40 to 125 | LP38855S -1.2 |
| LP38855SX-1.2/NOPB.A | Active | Production | DDPAK/ TO-263 (KTT) \| 5 | 500 \| LARGE T&R | ROHS Exempt | SN | Level-3-245C-168 HR | -40 to 125 | LP38855S -1.2 |
| LP38855T-0.8/NOPB | Active | Production | TO-220 (NDH) \| 5 | 45 \| TUBE | Yes | SN | Level-1-NA-UNLIM | -40 to 125 | LP38855T -0.8 |
| LP38855T-0.8/NOPB.A | Active | Production | TO-220 (NDH) \| 5 | 45 \| TUBE | Yes | SN | Level-1-NA-UNLIM | -40 to 125 | LP38855T -0.8 |
| LP38855T-1.2/NOPB | Active | Production | TO-220 (NDH) \| 5 | 45 \| TUBE | Yes | SN | Level-1-NA-UNLIM | -40 to 125 | LP38855T -1.2 |
| LP38855T-1.2/NOPB.A | Active | Production | TO-220 (NDH) \| 5 | 45 \| TUBE | Yes | SN | Level-1-NA-UNLIM | -40 to 125 | LP38855T -1.2 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

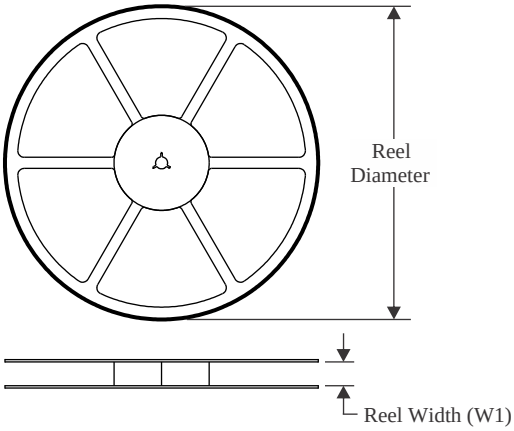
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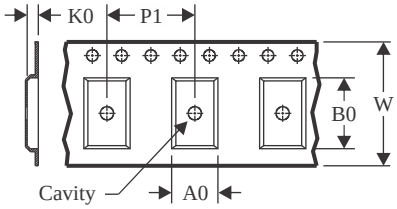
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## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

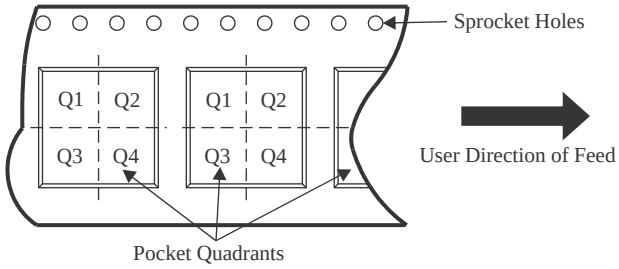



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

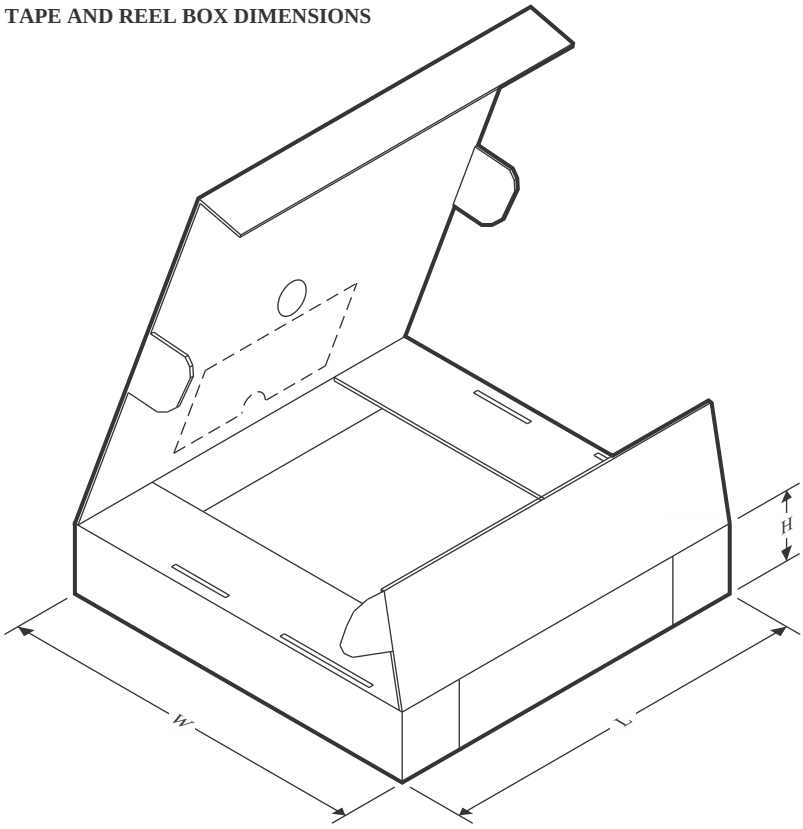
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LP38855SX-1.2/NOPB | DDPAK/ TO-263 | KTT | 5 | 500 | 330.0 | 24.4 | 10.75 | 14.85 | 5.0 | 16.0 | 24.0 | Q2 |

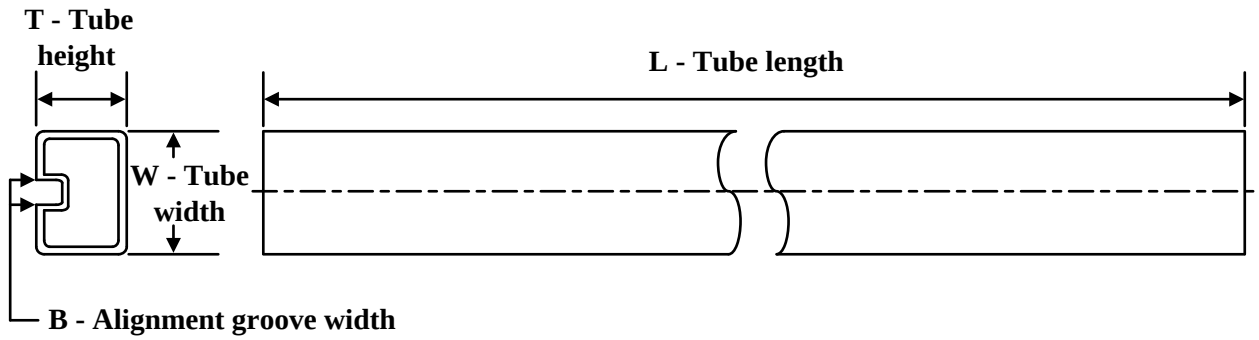
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LP38855SX-1.2/NOPB | DDPAK/TO-263 | KTT | 5 | 500 | 356.0 | 356.0 | 45.0 |

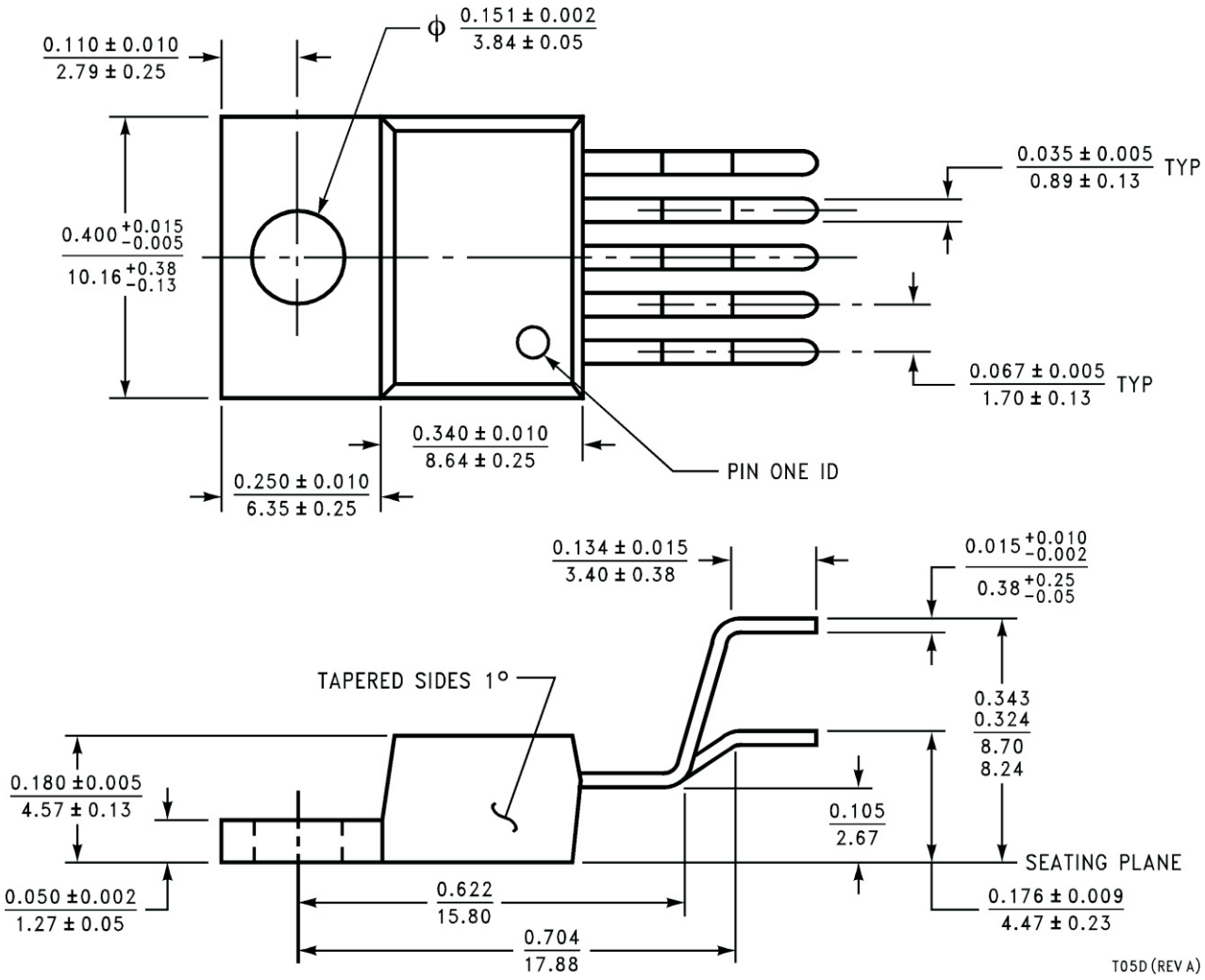
## TUBE



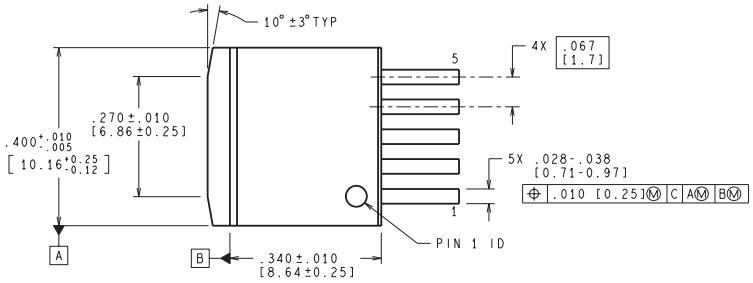

*All dimensions are nominal

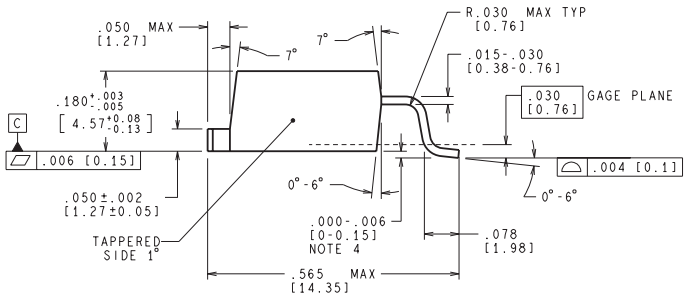
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| LP38855S-1.2/NOPB | KTT | TO-263 | 5 | 45 | 502 | 25 | 8204.2 | 9.19 |
| LP38855S-1.2/NOPB.A | KTT | TO-263 | 5 | 45 | 502 | 25 | 8204.2 | 9.19 |
| LP38855T-0.8/NOPB | NDH | TO-220 | 5 | 45 | 502 | 30 | 30048.2 | 10.74 |
| LP38855T-0.8/NOPB.A | NDH | TO-220 | 5 | 45 | 502 | 30 | 30048.2 | 10.74 |
| LP38855T-1.2/NOPB | NDH | TO-220 | 5 | 45 | 502 | 30 | 30048.2 | 10.74 |
| LP38855T-1.2/NOPB.A | NDH | TO-220 | 5 | 45 | 502 | 30 | 30048.2 | 10.74 |

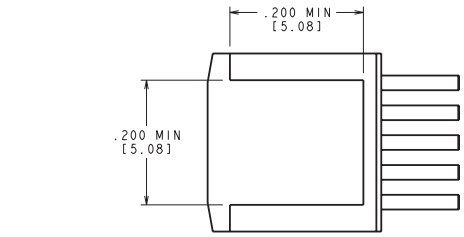
NDH0005D


0.110 ± 0.010
2.79 ± 0.25
ϕ 0.151 ± 0.002
3.84 ± 0.05
0.035 ± 0.005
0.89 ± 0.13
TYP
0.400 +0.015 −0.005
10.16 +0.38 −0.13
0.067 ± 0.005
1.70 ± 0.13
TYP
0.340 ± 0.010
8.64 ± 0.25
PIN ONE ID
0.250 ± 0.010
6.35 ± 0.25
0.134 ± 0.015
3.40 ± 0.38
0.015 +0.010 −0.002
0.38 +0.25 −0.05
TAPERED SIDES 1°
0.343
0.324
8.70
8.24
0.180 ±0.005
4.57 ± 0.13
0.105
2.67
SEATING PLANE
0.050 ±0.002
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0.704
17.88
T05D (REV A)

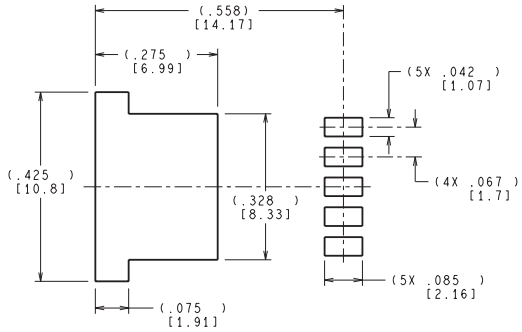
# KTT0005B




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