MIC37150/1/2/3

1.5A, Low Voltage µCap LDO Regulators

Features

- 1.5A Minimum Guaranteed Output Current
- 500 mV Maximum Dropout Voltage over Temperature
  - Ideal for 3.0V to 2.5V Conversion
  - Ideal for 2.5V to 1.8V, 1.65V, or 1.5V Conversion
- Stable with Ceramic or Tantalum Capacitor
- Wide Input Voltage Range
  - V_{IN}: 2.25V to 6.0V
- ±1.0% Initial Output Tolerance
- Fixed and Adjustable Output Voltages
  - MIC37150: 3-Lead S-Pak Fixed Voltages
  - MIC37151: 5-Lead S-Pak Fixed Voltages with Flag
  - MIC37152: 5-Lead S-Pak or 8-Lead SOIC Adjustable Voltage
  - MIC37153: 8-Lead ePad SOIC Adjustable Voltage with Flag
- Excellent Line and Load Regulation Specifications
- Logic Controlled Shutdown
- Thermal Shutdown and Current-Limit Protection
- Reverse-Leakage Protection
- Low Profile 3- or 5-Lead S-Pak Packages or 8-Lead ePad SOIC

Applications

- LDO Linear Regulator for Low-Voltage Digital IC
- PC Add-In Cards
- High Efficiency Linear Power Supplies
- SMPS Post Regulator
- Battery Charger

General Description

The MIC37150, MIC37151, MIC37152, and MIC37153 are 1.5A low-dropout linear voltage regulators that provide low voltage and high current output with a minimum of external components. They offer high precision, ultra-low dropout (500 mV over temperature), and low ground current.

The MIC37150/1/2/3 operate from an input of 2.25V to 6.0V. They are designed to drive digital circuits that require low voltage at high currents (i.e., PLDs, DSPs, microcontrollers, etc.). They are available in fixed and adjustable output voltages. Fixed voltages include 1.5V, 1.65V, 1.8V, 2.5V, and 3.3V. The adjustable version is capable of supplying output voltages from 1.24V to 5.5V.

Features of the MIC37150/1/2/3 LDOs include thermal and current-limit protection, reverse current protection, and reverse battery protection. Logic enable and error flag pins are available.

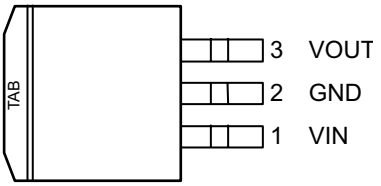
Junction temperature range of the MIC37150/1/2/3 is from –40°C to +125°C.

For applications that require input voltage greater than 6.0V, see MIC3910x, MIC3915x, MIC3930x, and MIC3950x LDOs.

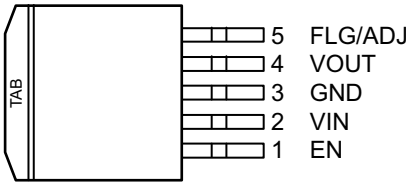
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Package Types

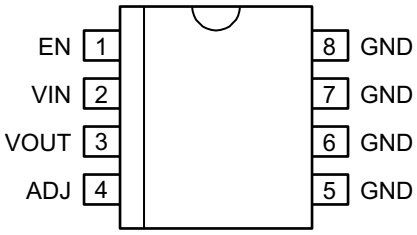
MIC37150
3-Lead S-Pak (WR)
(Top View)



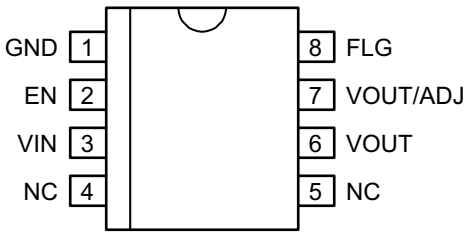
MIC37151/2
5-Lead S-Pak (WR)
(Top View)



MIC37152
8-Lead SOIC (YM)
(Top View)

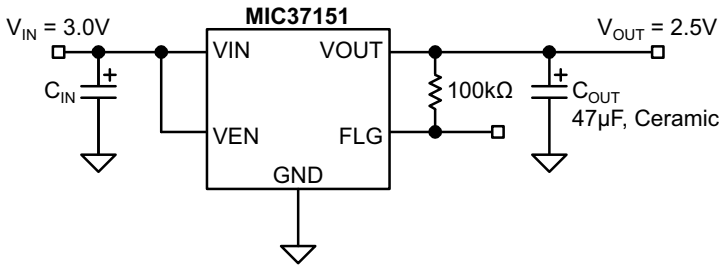


MIC37153
8-Lead EP SOIC (YME)
(Top View)

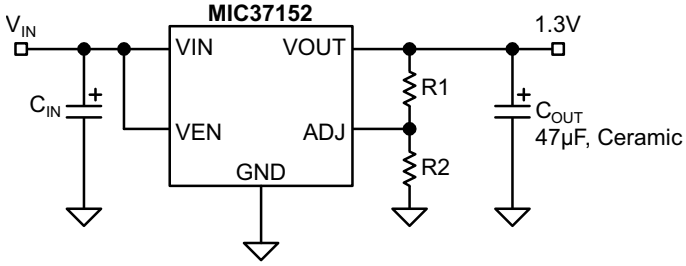


Typical Application Circuits

Fixed 2.5V Regulator with Error Flag



Adjustable Regulator



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{IN}) ..... +6.5V
Enable Input Voltage (V_{EN}) ..... +6.5V
Power Dissipation ..... Internally Limited
ESD Rating ..... Note 1

Operating Ratings ‡

Supply Voltage (V_{IN}) ..... +2.25V to +6.0V
Enable Input Voltage (V_{EN}) ..... 0V to +6.0V
Maximum Power Dissipation ..... Note 2

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ Notice: The device is not guaranteed to function outside its operating ratings.

Note 1: Devices are ESD sensitive. Handling precautions are recommended.

2: $P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA}$, where θ_{JA}, depends upon the printed circuit layout. See "Applications Information."

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: T_A = +25°C with $V_{IN} = V_{OUT}$ + 1V; $V_{EN} = V_{IN}$; **bold** values valid for –40°C < T_J < +125°C, unless otherwise noted. Note 1

Parameter	Min.	Typ.	Max.	Units	Condition
Output Voltage Accuracy	–1	—	1	%	I_L = 10 mA
	–2	—	**2**		10 mA < I_{OUT} < $I_{L(MAX)}$, V_{OUT} + 1 ≤ V_{IN} ≤ 6V
Output Voltage Line Regulation	—	0.06	0.5	%	$V_{IN} = V_{OUT}$ +1.0V to 6.0V
Output Voltage Load Regulation	—	0.2	1	%	I_L = 10 mA to 1.5A
$V_{IN} - V_{OUT}$; Dropout Voltage Note 2	—	—	**350**	mV	I_L = 750 mA
	—	—	**500**		I_L = 1.5A
Ground Pin Current, Note 3	—	17	**30**	mA	I_L = 1.5A
Ground Pin Current in Shutdown	—	1.0	—	µA	V_{IL} ≤ 0.5V, $V_{IN} = V_{OUT}$ + 1V
Current Limit	—	2.25	**4.0**	A	V_{OUT} = 0V

Note 1: Specification for packaged product only.

2: $V_{DO} = V_{IN} - V_{OUT}$ when V_{OUT} decreased to 98% of its nominal output voltage with $V_{IN} = V_{OUT}$ +1V. For output voltages below 1.75V, dropout voltage specification does not apply due to a minimum input operating voltage of 2.25V.

3: I_{IN} is the quiescent current. $I_{IN} = I_{IN} + I_{OUT}$.

4: For a 2.5V device, V_{IN} = 2.250V (device is in dropout).

5: $V_{REF} \le V_{OUT} \le (V_{IN} - 1.0V)$, 2.25V ≤ V_{IN} ≤ 6.0V, 10 mA ≤ I_L ≤ 1.5A, $T_J = T_{MAX}$.

6: Thermal regulation is defined as the change in output voltage at a time t after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a 200 mA load pulse at V_{IN} = 6V for t = 10 ms.

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ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: T_A = +25°C with $V_{IN} = V_{OUT}$ + 1V; $V_{EN} = V_{IN}$; **bold** values valid for –40°C < T_J < +125°C, unless otherwise noted. Note 1

Parameter	Min.	Typ.	Max.	Units	Condition
Start-Up Time	—	170	**500**	µs	$V_{EN} = V_{IN}$, I_{OUT} = 10 mA, C_{OUT} = 22 µF
Enable Input					
Enable Input Threshold	**2.25**	—	—	V	Regulator enable
	—	—	**0.8**		Regulator shutdown
Enable Pin Input Current	—	—	**4**	µA	V_{IL} ≤ 0.8V (regulator shutdown)
	1	15	—		V_{IH} ≥ 2.25V (regulator enabled)
	—	—	**75**		
Flag Output					
$I_{FLG(LEAK)}$	—	—	1	µA	V_{OH} = 6V
	—	—	**2**		
$V_{FLG(LO)}$	—	210	300	mV	V_{IN} = 2.25V, I_{OL} = 250 µA, Note 4
	—	—	**400**		
V_{FLG}	93	—	—	%	Low threshold, % of V_{OUT} below nominal
	—	2	—		Hysteresis
	—	—	99.2		High threshold, % of V_{OUT} below nominal
Reference Voltage	1.228	1.240	1.252	V	—
	1.215	—	**1.265**		Note 5
Reference Voltage Temp. Coefficient	—	**20**	—	ppm/°C	Note 6
Adjust Pin Bias Current	—	40	80	nA	—
	—	—	**120**		
Adjust Pin Bias Current Temp. Coefficient	—	0.1	—	nA/°C	—

Note 1: Specification for packaged product only.

2: $V_{DO} = V_{IN} - V_{OUT}$ when V_{OUT} decreased to 98% of its nominal output voltage with $V_{IN} = V_{OUT}$ +1V. For output voltages below 1.75V, dropout voltage specification does not apply due to a minimum input operating voltage of 2.25V.

3: I_{IN} is the quiescent current. $I_{IN} = I_{IN} + I_{OUT}$.

4: For a 2.5V device, V_{IN} = 2.250V (device is in dropout).

5: $V_{REF} \le V_{OUT} \le (V_{IN} - 1.0V)$, 2.25V ≤ V_{IN} ≤ 6.0V, 10 mA ≤ I_L ≤ 1.5A, $T_J = T_{MAX}$.

6: Thermal regulation is defined as the change in output voltage at a time t after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a 200 mA load pulse at V_{IN} = 6V for t = 10 ms.

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TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Maximum Junction Temperature Range	T_J	–40	—	+125	°C	Note 1
Operating Junction Temperature Range	T_J	–40	—	+125	°C	—
Storage Temperature Range	T_S	–65	—	+150	°C	—
Lead Temperature	—	—	—	+260	°C	Soldering, 5 sec.
Package Thermal Resistances						
S-Pak, 3-Ld or 5-Ld	θ_{JC}	—	2	—	°C/W	—
Power SOIC 8-Ld	θ_{JA}	—	63	—	°C/W	—
ePad SOIC 8-Ld	θ_{JC}	—	10	—	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

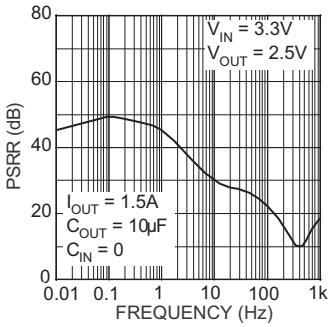


FIGURE 2-1: *Power Supply Rejection Ratio.*

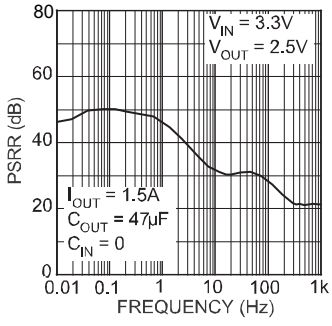


FIGURE 2-2: *Power Supply Rejection Ratio.*

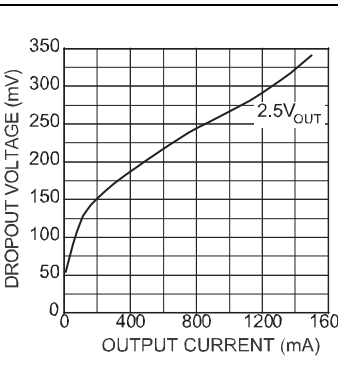


FIGURE 2-3: *Dropout Voltage vs. Output Current.*

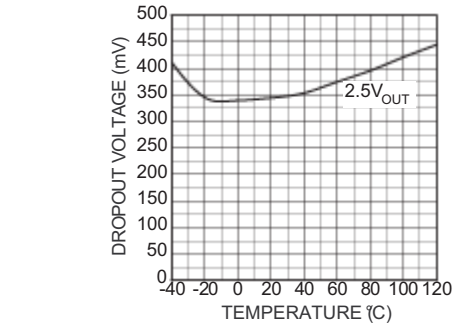


FIGURE 2-4: *Dropout Voltage vs. Temperature.*

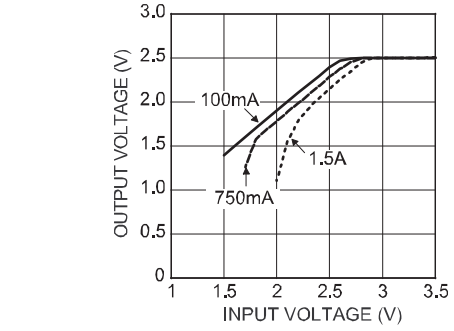


FIGURE 2-5: *Dropout Characteristics.*

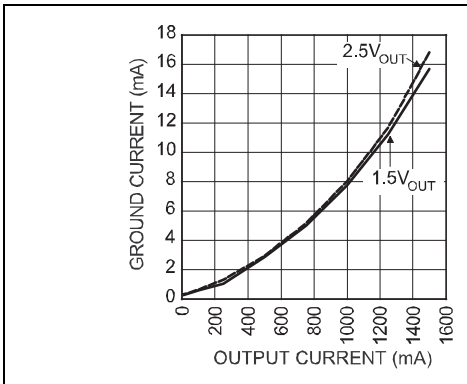


FIGURE 2-6: *Ground Current vs. Output Current.*

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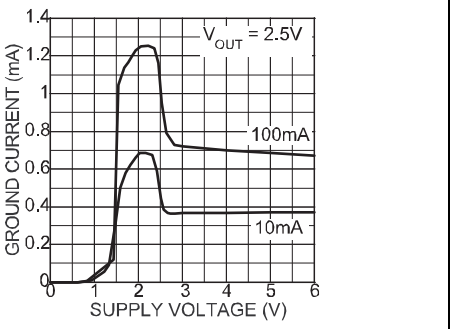


FIGURE 2-7: *Ground Current vs. Supply Voltage.*

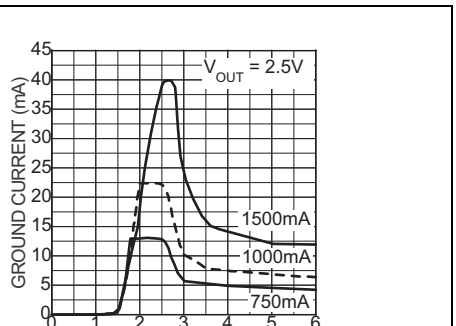


FIGURE 2-8: *Ground Current vs. Supply Voltage.*

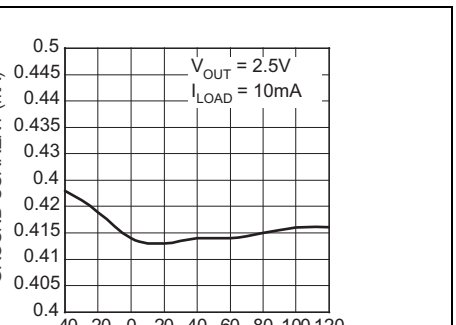


FIGURE 2-9: *Ground Current vs. Temperature.*

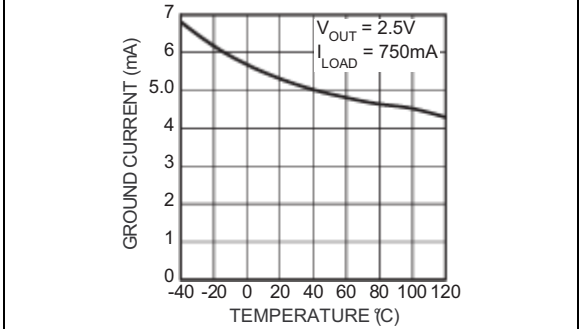


FIGURE 2-10: *Ground Current vs. Temperature.*

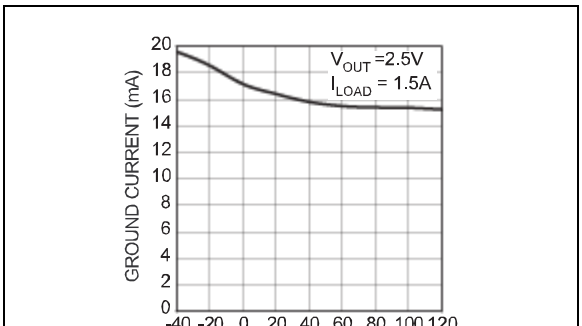


FIGURE 2-11: *Ground Current vs. Temperature.*

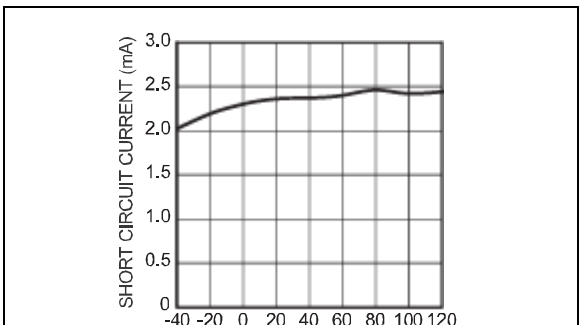


FIGURE 2-12: *Short-Circuit Current vs. Temperature.*

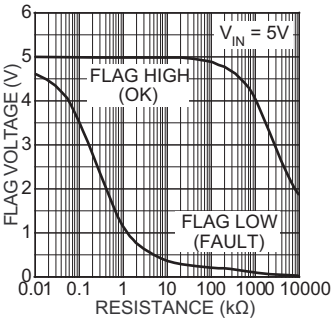


FIGURE 2-13: *Error Flag Pull-Up Resistor.*

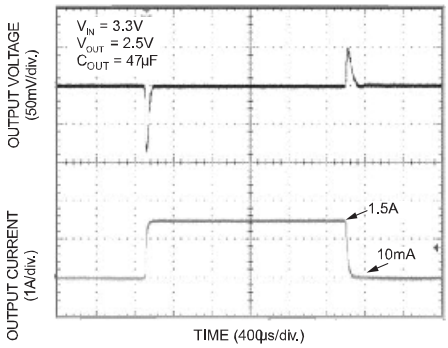


FIGURE 2-16: *Load Transient Response.*

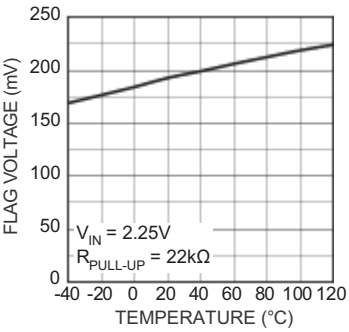


FIGURE 2-14: *Flag-Low Voltage vs. Temperature.*

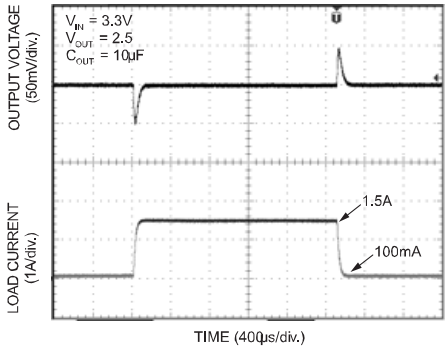


FIGURE 2-17: *Load Transient Response.*

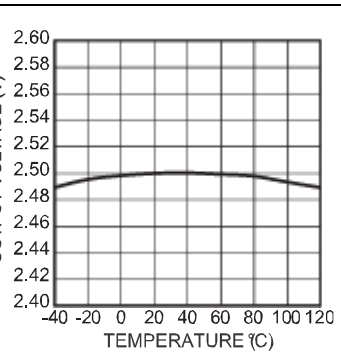


FIGURE 2-15: *Output Voltage vs. Temperature.*

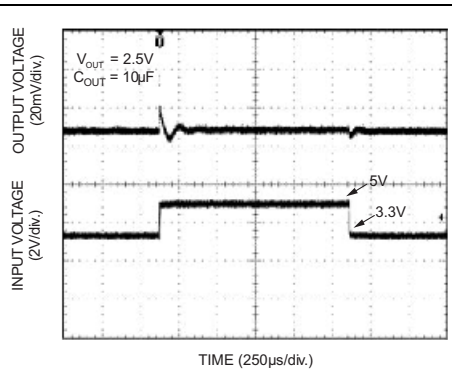


FIGURE 2-18: *Line Transient Response.*

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3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number S-Pak-3	Pin Number S-Pak-5	Pin Number SOIC-8	Pin Number EP SOIC-8	Pin Name	Description
—	1	1	2	EN	Enable (Input): CMOS compatible input. Logic high = enable, logic low = shut-down.
1	2	2	3	VIN	Input voltage that supplies current to the output power device.
2	3	5, 6, 7, 8	1	GND	Ground (TAB is connected to ground on S-Pak)
3	4	3	6, 7 (Fixed) 6 (Adj.)	VOUT	Regulator Output
—	5	—	8	FLG	Error Flag (Output): Open collector out-put. Active-low indicates an output fault condition.
—		4	7	ADJ	Adjustable regulator feedback input. Connect to resistor voltage divider.
—	—	—	4, 5	NC	Not internally connected.

4.0 APPLICATION INFORMATION

The MIC37150/1/2/3 are high-performance, low dropout voltage regulators suitable for moderate-to-high current regulator applications. Its 500 mV dropout voltage at full load and over temperature makes them especially valuable in battery-powered systems and as high efficiency noise filters in post-regulator applications. Unlike older NPN-pass transistor designs, the minimum dropout voltage is limited by the based-to-emitter voltage drop and collector-to-emitter saturation voltage, dropout performance of the PNP output of these devices is limited only by the low V_{CE} saturation voltage.

A trade-off for the low dropout voltage is a varying base drive requirement. The Super ßeta PNP process reduces this drive requirement to only 2% to 5% of the load current.

The MIC37150/1/2/3 regulators are fully protected from damage due to fault conditions. Current limiting is provided. This limiting is linear; output current during overload conditions is constant. Thermal shutdown disables the device when the die temperature exceeds the maximum safe operating temperature. Transient protection allows device (and load) survival even when the input voltage spikes above and below nominal. The output structure of these regulators allows voltages in excess of the desired output voltage to be applied without reverse current flow.

4.1 Thermal Design

Linear regulators are simple to use. The most complicated design parameters to consider are thermal characteristics. Thermal design requires the following application-specific parameters:

- Maximum ambient temperature (T_A)
- Output current (I_{OUT})
- Output voltage (V_{OUT})
- Input voltage (V_{IN})
- Ground current (I_{GND})

First, calculate the power dissipation of the regulator from these numbers and the device parameters from this data sheet.

EQUATION 4-1:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND}$$

The ground current is approximated by using numbers from the “Electrical Characteristics” or “Typical Characteristics.” Then, the heat sink thermal resistance is determined with the formula in Equation 4-2.

EQUATION 4-2:

$$\theta_{SA} = ((T_{J(MAX)} - T_A)/P_D) - (\theta_{JC} + \theta_{CS})$$

Where:
$T_{J(MAX)} \leq 125°C$
θ_{CS} = Between 0°C/W and 2°C/W.

The heat sink may be significantly reduced in applications where the minimum input voltage is known and is large compared with the dropout voltage. Use a series input resistor to drop excessive voltage and distribute the heat between this resistor and the regulator. The low dropout properties of the Super ßeta PNP regulators allow significant reductions in regulator power dissipation and the associated heat sink without compromising performance. When this technique is employed, a capacitor of at least 1.0 µF is needed directly between the input and regulator ground.

Refer to “Application Note 9” for further details and examples on thermal design and heat sink applications.

4.2 Output Capacitor

The MIC37150/1/2/3 require an output capacitor for stable operation. As µCap LDOs, the MIC37150/1/2/3 can operate with ceramic output capacitors as long as the amount of capacitance is 47 µF or greater. For values of output capacitance lower than 47 µF, the recommended ESR range is 200 mΩ to 2Ω. The minimum value of output capacitance recommended for the MIC37151 is 10 µF.

For 47 µF or greater, the ESR range recommended is less than 1Ω. Ultra-low ESR ceramic capacitors are recommended for output capacitance of 47 µF or greater to help improve transient response and noise reduction at high frequency. X7R/X5R dielectric-type ceramic capacitors are recommended because of their temperature performance. X7R-type capacitors change capacitance by 15% over their operating temperature range and are the most stable type of ceramic capacitors. Z5U and Y5V dielectric capacitors change value by as much as 50% and 60% respectively over their operating temperature ranges. To use a ceramic chip capacitor with Y5V dielectric, the value must be much higher than an X7R ceramic capacitor to ensure the same minimum capacitance over the equivalent operating temperature range. The MIC37150/1/2/3 has excellent transient response to variations in input voltage and load current. The device has been designed to respond quickly to load current variations and input voltage variations. Large output capacitors are not required to obtain this performance.

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A standard 47 µF output capacitor, is all that is required. Larger values help to improve performance even further.

4.3 Input Capacitor

An input capacitor of 1.0 µF or greater is recommended when the device is more than 4 inches away from the bulk and supply capacitance, or when the supply is a battery. Small, surface-mount chip capacitors can be used for the bypassing. The capacitor should be place within 1" of the device for optimal performance. Larger values will help to improve ripple rejection by bypassing the input to the regulator, further improving the integrity of the output voltage.

4.4 Transient Response and 3.3V to 2.5V, 2.5V to 1.8V or 1.65V, or 2.5V to 1.5V Conversions

The MIC37150/1/2/3 have excellent transient response to variations in input voltage and load current. The device has been designed to respond quickly to load current variations and input voltage variations. Large output capacitors are not required to obtain this performance. A standard 10 µF output capacitor, preferably tantalum, is all that is required. Larger values help to improve performance even further.

By virtue of their low dropout voltage, these devices do not saturate into dropout as readily as similar NPN-based designs. When converting from 3.3V to 2.5V, 2.5V to 1.8V or 1.65V, or 2.5V to 1.5V, the NPN-based regulators are already operating in dropout, with typical dropout requirements of 1.2V or greater. To convert down to 2.5V without operating in dropout, NPN-based regulators require an input voltage of 3.7V at the very least. The MIC37150/1/2/3 regulators will provide excellent performance with an input as low as 3.0V or 2.25V, respectively. This gives the PNP-based regulators a distinct advantage over older, NPN-based linear regulators.

4.5 Minimum Load Current

The MIC37150/1/2/3 regulators are specified between finite loads. If the output current is too small, leakage currents dominate and the output voltage rises. A 10 mA minimum load current is necessary for proper operation.

4.6 Error Flag

The MIC37151 and MIC37153 feature an error flag circuit that monitors the output voltage and signals an error condition when the voltage 5% below the nominal output voltage. The error flag is an open-collector output that can sink 10 mA during a fault condition.

Low output voltage can be caused by a number of problems, including an overcurrent fault (device in current limit) or low input voltage. The flag is inoperative during overtemperature shutdown.

4.7 Enable Input

The MIC37151, MIC37152, and MIC37153 also feature an enable input for on/off control of the device. Its shutdown state draws "zero" current (only microamperes of leakage). The enable input is TTL/CMOS compatible for simple logic interface, but can be connected to up to V_{IN}. When enabled, it draws approximately 15 µA.

4.8 Adjustable Regulator Deisgn

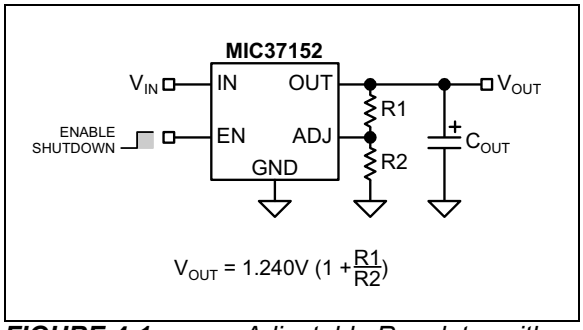


FIGURE 4-1: *Adjustable Regulator with Resistors.*

The MIC37152 and MIC37153 allow programming the output voltage anywhere between 1.24V and the 5.5V maximum operating rating of the family. Two resistors are used. Resistors can be quite large, up to 1 MΩ, because of the very high input impedance and low bias current of the sense comparator: The resistor values are calculated by:

EQUATION 4-3:

$$R1 = R2 \times \left(\frac{V_{OUT}}{1.240} - 1\right)$$

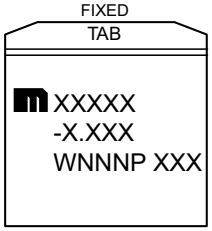
Where:
V_{OUT} = The desired output voltage.

Figure 4-1 shows component definition. Applications with widely varying load currents may scale the resistors to draw the minimum load current required for proper operation.

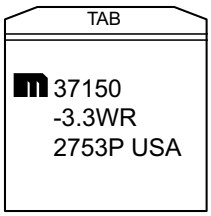
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

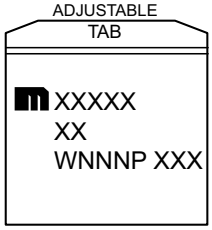
3- or 5-Lead S-Pak*
FIXED



Example



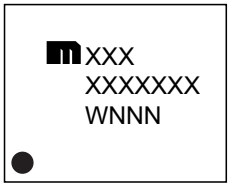
5-Lead S-Pak*
ADJUSTABLE



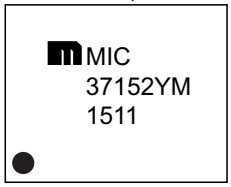
Example



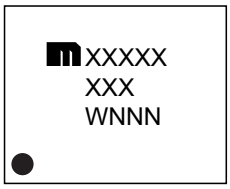
8-Lead SOIC*



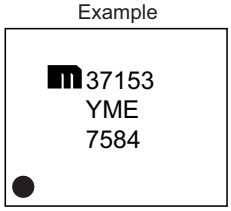
Example



8-Lead EP SOIC*



Example



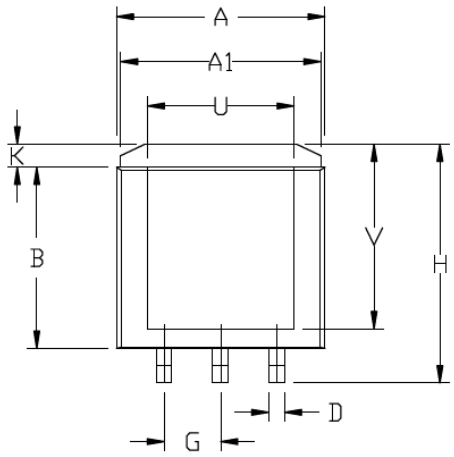
Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

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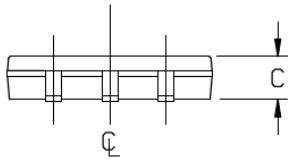
3-Lead S-Pak Package Outline and Recommended Land Pattern

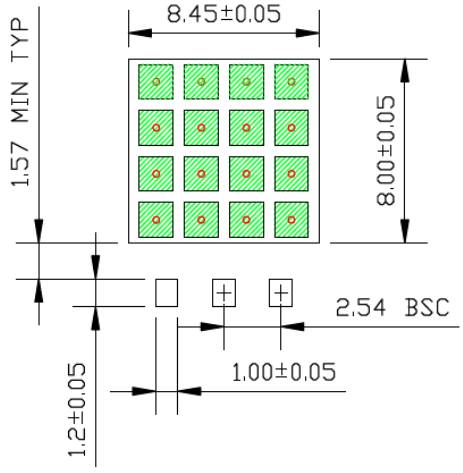
TITLE
3 LEAD SPAK PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	SPAK-3LD-PL-1	**UNIT**	INCH/MM



	INCHES		MILLIMETERS	
A	0.365	0.375	9.27	9.52
A1	0.350	0.360	8.89	9.14
B	0.310	0.320	7.87	8.13
C	0.070	0.080	1.78	2.03
D	0.025	0.031	0.63	0.79
E	0.010	BSC	0.25	BSC
G	0.100	BSC	2.54	BSC
H	0.410	0.420	10.41	10.67
K	0.030	0.050	0.76	1.27
L	0.001	0.005	0.03	0.13
M	0.035	0.045	0.89	1.14
N	0.010	BSC	0.25	BSC
P	0.031	0.041	0.79	1.04
R	0°	6°	0°	6°
U	0.256	BSC	6.50	BSC
V	0.316	BSC	8.03	BSC





RECOMMENDED LAND PATTERN (UNIT: MM)

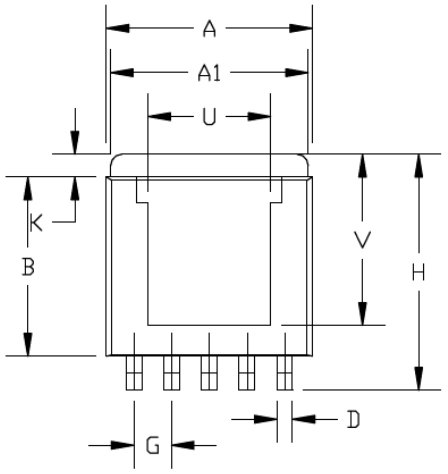
NOTE:
1. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. DIMENSION INCLUDES PLATING THICKNESS. SOLDER MASK OPENING
3. RED CIRCLES IN LAND PATTERN REPRESENT THERMAL VIA, 0.30MM IN DIAMETER & SHOULD BE CONNECTED TO GND FOR MAXIMUM PERFORMANCE
4. GREEN RECTANGLES IN LAND PATTERN REPRESENT SOLDER STENCIL OPENING (OPTIONAL), 1.50X1.50MM.

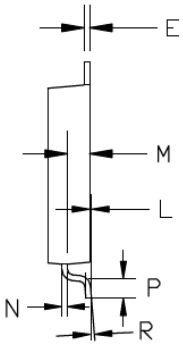
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

5-Lead S-Pak Package Outline and Recommended Land Pattern

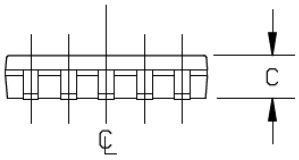
TITLE
5 LEAD SPAK PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	SPAK-5LD-PL-1	UNIT	MM

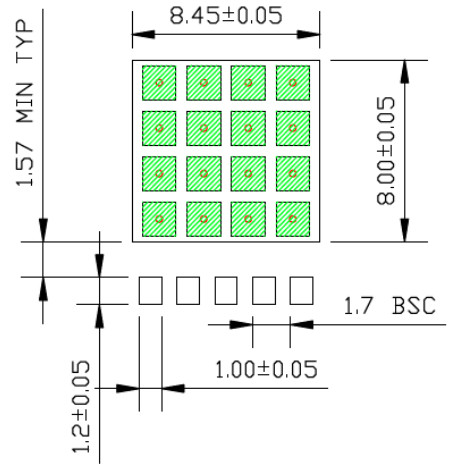




	INCHES		MILLIMETERS	
A	0.365	0.375	9.27	9.52
A1	0.350	0.360	8.89	9.14
B	0.310	0.320	7.87	8.13
C	0.070	0.080	1.78	2.03
D	0.025	0.031	0.63	0.79
E	0.010	BSC	0.25	BSC
G	0.067	BSC	1.70	BSC
H	0.410	0.420	10.41	10.67
K	0.030	0.050	0.76	1.27
L	0.001	0.005	0.03	0.13
M	0.035	0.045	0.89	1.14
N	0.010	BSC	0.25	BSC
P	0.031	0.041	0.79	1.04
R	0°	6°	0°	6°
U	0.220	BSC	5.58	BSC
V	0.296	BSC	7.52	BSC



NOTE:
1. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. DIMENSION INCLUDES PLATING THICKNESS. SOLDER MASK OPENING
3. RED CIRCLES IN LAND PATTERN REPRESENT THERMAL VIA, 0.30MM IN DIAMETER & SHOULD BE CONNECTED TO GND FOR MAXIMUM PERFORMANCE
4. GREEN RECTANGLES IN LAND PATTERN REPRESENT SOLDER STENCIL OPENING (OPTIONAL), 1.50X1.50MM.



RECOMMENDED LAND PATTERN

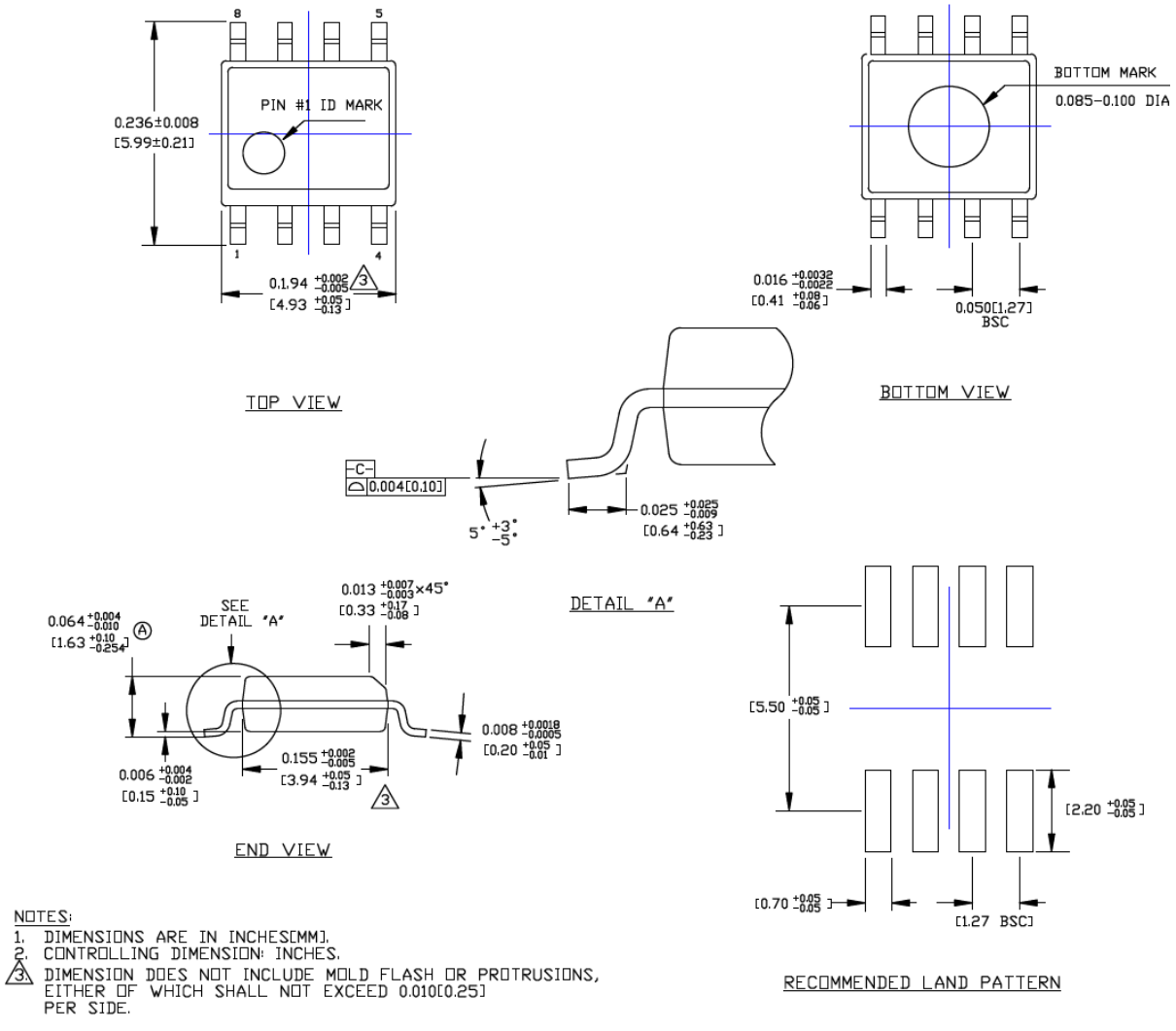
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

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8-Lead SOIC Package Outline and Recommended Land Pattern

TITLE
8 LEAD SOICN PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	SOICN-8LD-PL-1	UNIT	INCH [MM]



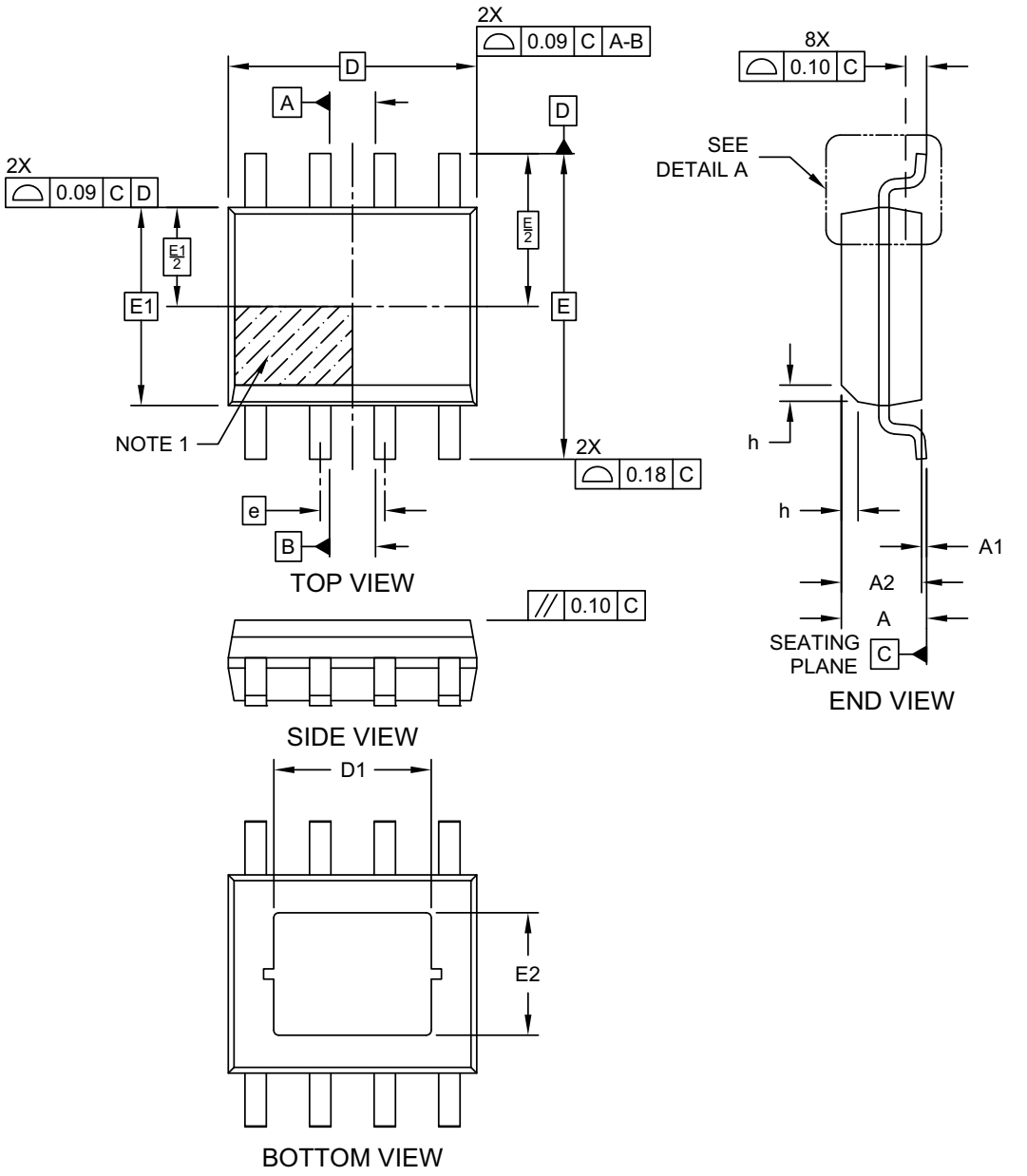
NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.010[0.25] PER SIDE.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

8-Lead EP SOIC Package Outline and Recommended Land Pattern

8-Lead Small Outline Integrated Circuit Package (EQA) - 3.90 mm (1.50 In) Body [SOIC] With 3.10x2.41 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

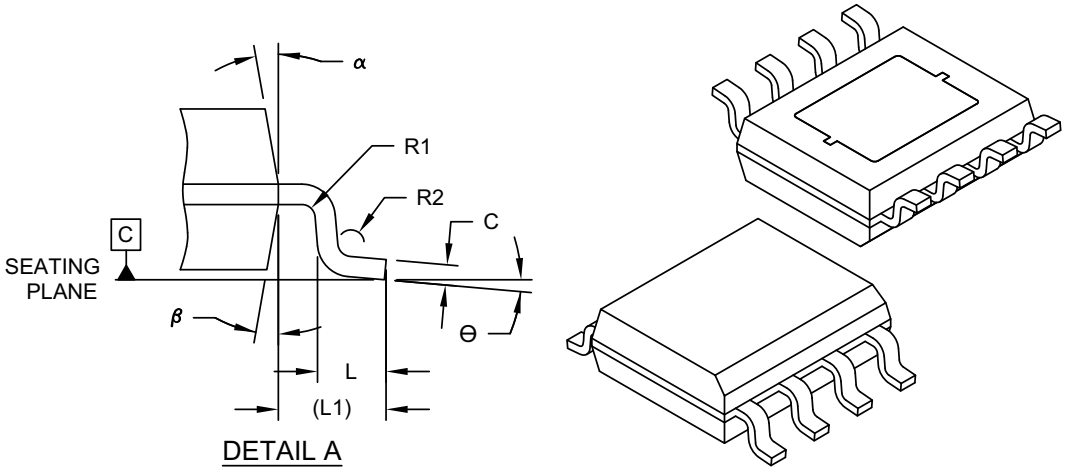


Microchip Technology Drawing C04-1136 Rev A Sheet 1 of 2

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8-Lead Small Outline Integrated Circuit Package (EQA) - 3.90 mm (1.50 In) Body [SOIC] With 3.10x2.41 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	1.43	1.55	1.68
Standoff	A1	0.00	0.05	0.10
Molded Package Thickness	A2	1.25	-	-
Overall Length	D		4.89 BSC	
Exposed Pad Length	D1	-	3.10	-
Overall Width	E		6.02 BSC	
Molded Package Width	E1		3.90 BSC	
Exposed Pad Width	E2	-	2.41	-
Terminal Width	b	0.35	0.41	0.49
Lead Thickness	c	0.19	0.20	0.25
Terminal Length	L	0.41	0.64	0.89
Terminal-to-Exposed-Pad	L1		1.04 REF	
Foot Angle	Θ	0°	5°	8°
Lead Bend Radius	R1	0.07	-	-
Terminal Length	R2	0.07	-	-
Mold Draft Angle	α	5°	-	15°
Mold Draft Angle	β	5°	-	15°

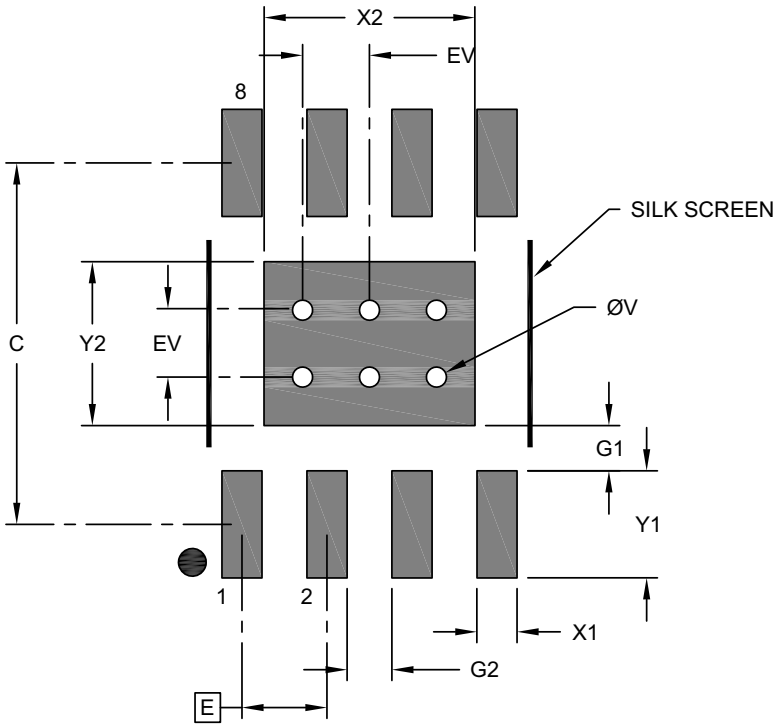
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1136 Rev A Sheet 2 of 2

8-Lead Small Outline Integrated Circuit Package (EQA) - 3.90 mm (1.50 In) Body [SOIC] With 3.10x2.41 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Optional Center Pad Width	X2			3.15
Optional Center Pad Length	Y2			2.45
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.60
Contact Pad to Center Pad (X8)	G1	0.68		
Contact Pad to Contact Pad (X6)	G2	0.67		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-1136 Rev A

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APPENDIX A: REVISION HISTORY

Revision A (January 2021)

- Converted Micrel document MIC37150/1/2/3 to Microchip data sheet template DS20006491A.
- Minor grammatical text changes throughout.

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Device	-X.XX	XXX	-XX
Part No.	Output Voltage	Package	Media Type

Device:	MIC37150:	1.5A Low Voltage µCap LDO Regulator
	MIC37151:	1.5A Low Voltage µCap LDO Regulator
	MIC37152:	1.5A Low Voltage µCap LDO Regulator
	MIC37153:	1.5A Low Voltage µCap LDO Regulator
Output Voltage:	-1.5 =	1.5V
	-1.65 =	1.65V
	-1.8 =	1.8V
	-2.5 =	2.5V
	-3.3 =	3.3V
	<blank>=	Adjustable
Package:	WR =	3-Lead or 5-Lead S-Pak
	YM =	8-Lead SOIC
	YME =	8-Lead EP SOIC
Media Type:	<blank>=	48/Tube (WR Package Option)
	<blank>=	95/Tube (YM Package Option)
	TR =	750/Reel (WR Package Option)
	TR =	2500/Reel (YM & YME Package Options)

Examples:

a) MIC37150-1.5WR: MIC37150, 1.5V Output Voltage, 3-Lead S-Pak, –40°C to +125°C Range, 48/Tube

b) MIC37151-3.3WR-TR: MIC37151, 3.3V Output Voltage, 5-Lead S-Pak, –40°C to +125°C Range, 750/Reel

c) MIC37152YM: MIC37152, Adjustable Output Voltage, 8-Lead SOIC, –40°C to +125°C Range, 95/Tube

d) MIC37153YME-TR: MIC37153, Adjustable Output Voltage, 8-Lead EP SOIC, –40°C to +125°C Range, 2500/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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