Document Number: MMRF1020-04N
Rev. 0, 2/2014

RoHS

RF Power LDMOS Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

These 100 W symmetrical Doherty RF power LDMOS transistors are designed for cellular base station applications covering the frequency range of 720 to 960 MHz. The transistors are also suitable for wideband power amplifier applications from 600 to 1000 MHz and saturated power levels up to 500 watts.

- Typical Doherty Single-Carrier W-CDMA Performance: V_{DD} = 48 Vdc, I_{DQA} = 860 mA, V_{GSB} = 0.9 Vdc, P_{out} = 100 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

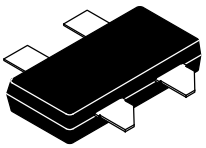
Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
920 MHz	19.5	48.5	7.2	–29.2
940 MHz	19.5	49.5	7.1	–32.0
960 MHz	19.2	48.0	7.0	–35.7

Features

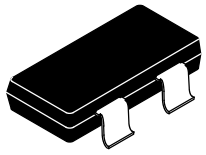
- Production Tested in a Symmetrical Doherty Configuration
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems
- In Tape and Reel. R3 Suffix = 250 Units, 32 mm Tape Width, 13-inch Reel.

MMRF1020-04NR3
MMRF1020-04GNR3

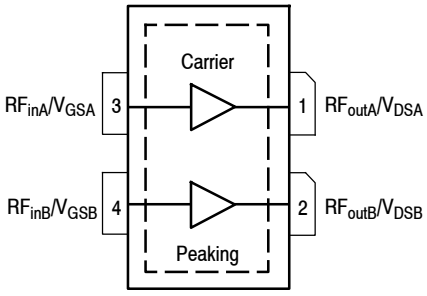
720–960 MHz, 100 W AVG., 48 V
RF POWER LDMOS
TRANSISTORS



OM-780-4L
PLASTIC
MMRF1020-04NR3



OM-780G-4L
PLASTIC
MMRF1020-04GNR3



(Top View)

Note: Exposed backside of the package is the source terminal for the transistors.

Figure 1. Pin Connections

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freescale Airfast

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	–0.5, +105	Vdc
Gate-Source Voltage	V_{GS}	–6.0, +10	Vdc
Operating Voltage	V_{DD}	55, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +150	°C
Operating Junction Temperature Range (1,2)	T_J	–40 to +225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 86°C, 102 W W-CDMA, 48 Vdc, I_{DQA} = 860 mA, V_{GSB} = 0.9 Vdc, 940 MHz	$R_{\theta JC}$	0.45	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1C
Machine Model (per EIA/JESD22-A115)	A
Charge Device Model (per JESD22-C101)	IV

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics (4)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 105 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 48 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics (4)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 460 μAdc)	$V_{GS(th)}$	1.3	1.8	2.3	Vdc
Gate Quiescent Voltage (V_{DD} = 48 Vdc, I_{DA} = 860 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	2.0	2.5	3.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 1.3 Adc)	$V_{DS(on)}$	0.1	0.21	0.3	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.
4. Each side of device measured separately.

(continued)

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (1,2,3) (In Freescale Doherty Test Fixture, 50 ohm system) V_{DD} = 48 Vdc, I_{DQA} = 860 mA, V_{GSB} = 0.9 Vdc, P_{out} = 100 W Avg., f = 920 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	18.5	19.5	21.5	dB
Drain Efficiency	η_D	45.0	48.5	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	6.6	7.2	—	dB
Adjacent Channel Power Ratio	ACPR	—	–29.2	–27.0	dBc
Load Mismatch (In Freescale Test Fixture, 50 ohm system) I_{DQA} = 860 mA, V_{GSB} = 0.9 Vdc, f = 940 MHz					
VSWR 10:1 at 52 Vdc, 500 W Pulsed Output Power (3 dB Input Overdrive from 200 W Pulsed Rated Power)		No Device Degradation			
Typical Performances (2) (In Freescale Doherty Test Fixture, 50 ohm system) V_{DD} = 48 Vdc, I_{DQA} = 860 mA, V_{GSB} = 0.9 Vdc, 920-960 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	200	—	W
P_{out} @ 3 dB Compression Point (4)	P3dB	—	500	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 920-960 MHz frequency range)	Φ	—	–21	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	43	—	MHz
Gain Flatness in 40 MHz Bandwidth @ P_{out} = 100 W Avg.	G_F	—	0.3	—	dB
Gain Variation over Temperature (-30°C to +85°C)	ΔG	—	0.01	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C)	ΔP1dB	—	0.0075	—	dB/°C

1. Part internally input matched.
2. Measurement made with device in a symmetrical Doherty configuration.
3. Measurement made with device in straight lead configuration before any lead forming operation is applied.
4. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.

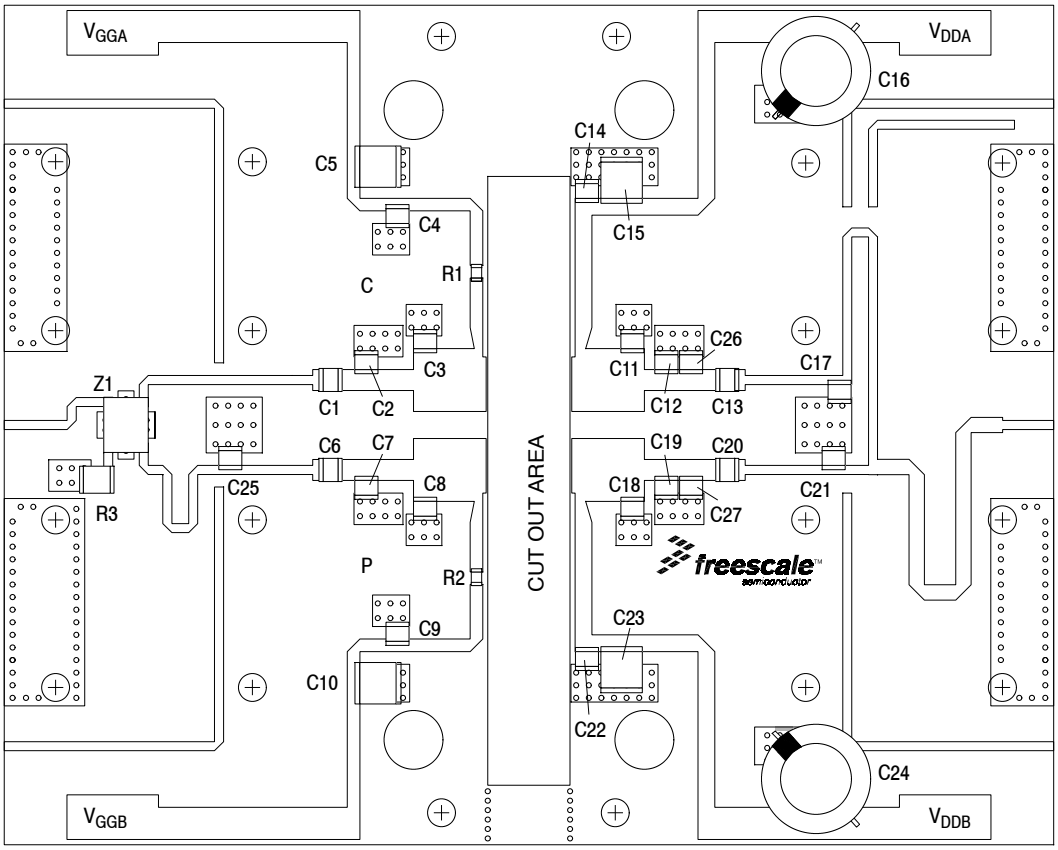


Figure 2. MMRF1020-04NR3 Test Circuit Component Layout

Table 6. MMRF1020-04NR3 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C6, C13, C20	33 pF Chip Capacitors	ATC100B330JT500XT	ATC
C2, C7, C17, C21	4.3 pF Chip Capacitors	ATC100B4R3CT500XT	ATC
C3, C8	6.8 pF Chip Capacitors	ATC100B6R8CT500XT	ATC
C4, C9. C14, C22	47 pF Chip Capacitors	ATC100B470JT500XT	ATC
C5, C10	2.2 μF Chip Capacitors	C3225X7R1H225K250AB	TDK
C11, C18	12 pF Chip Capacitors	ATC100B120JT500XT	ATC
C12, C19	8.2 pF Chip Capacitors	ATC100B8R2CT500XT	ATC
C15, C23	10 μF Chip Capacitors	C5750X7S2A106M230KB	TDK
C16, C24	220 μF, 100 V Electrolytic Capacitors	MCGPR100V227M16X26-RH	Multicomp
C25	0.5 pF Chip Capacitor	ATC100B0R5BT500XT	ATC
C26	0.3 pF Chip Capacitor	ATC100B0R3BT500XT	ATC
C27	0.8 pF Chip Capacitor	ATC100B0R8BT500XT	ATC
R1, R2	1.5 Ω, 1/4 W Chip Resistors	RC1206FR-071R5L	Yageo
R3	50 Ω , 30 W Termination	RFP-375375N6Z50-2	Anaren
Z1	800-1000 MHz Band, 90°, 3 dB Hybrid Coupler	X3C09P1-03S	Anaren
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	—	MTL

TYPICAL CHARACTERISTICS

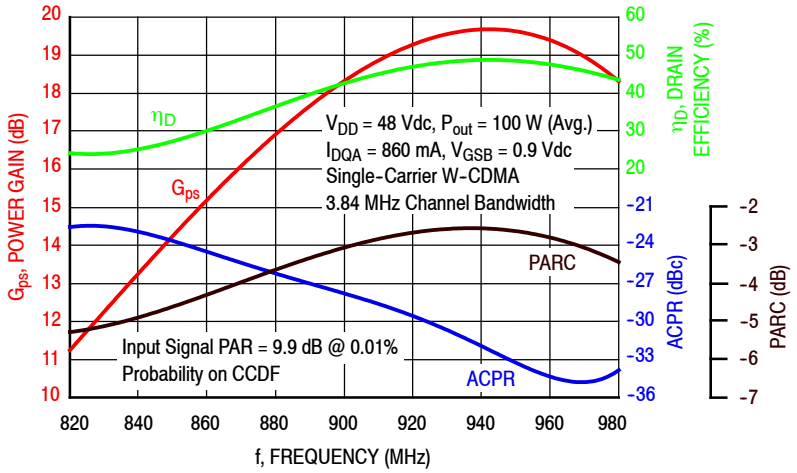


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 100 Watts Avg.

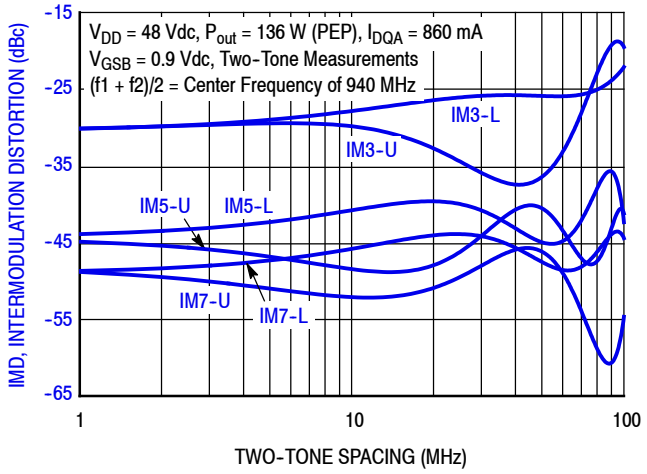


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

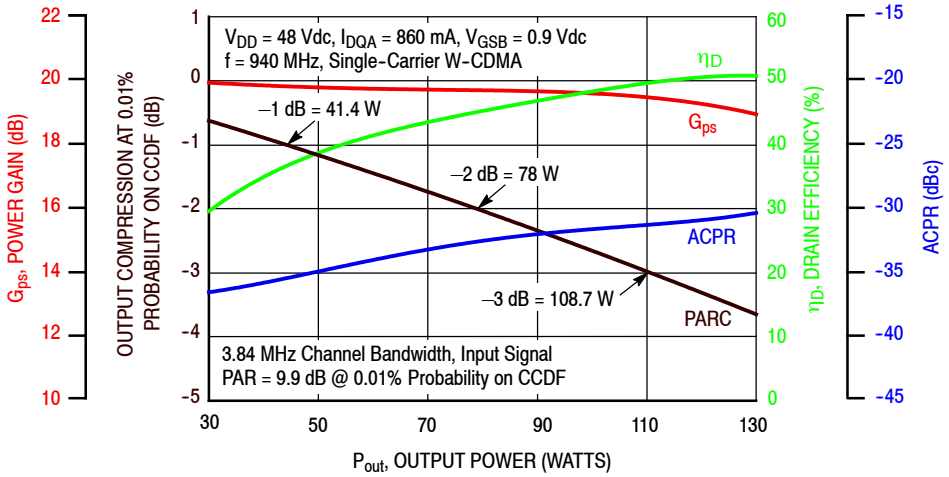


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS

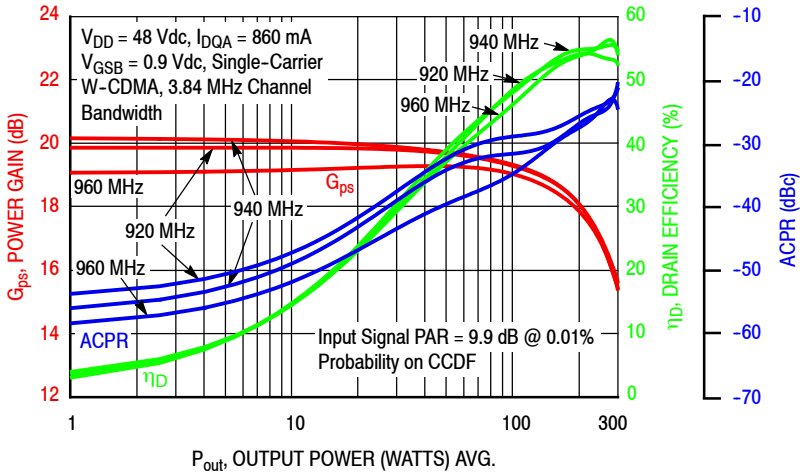


Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

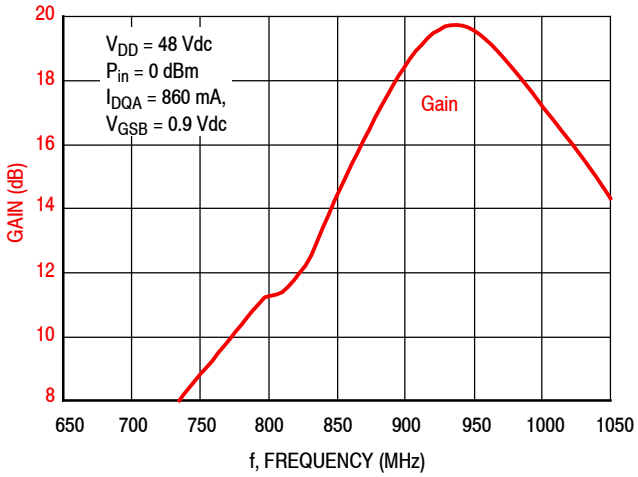


Figure 7. Broadband Frequency Response

Table 7. Carrier Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 48 Vdc, I_{DQ} = 862 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	2.39 – j3.65	2.32 + j3.41	1.84 + j0.12	21.3	54.1	260	59.9	–14
940	2.54 – j4.03	2.49 + j3.84	1.85 + j0.11	21.3	54.1	258	59.9	–14
960	2.90 – j4.64	2.76 + j4.31	1.77 + j0.13	21.2	54.1	259	59.8	–15

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	2.39 – j3.65	2.29 + j3.66	2.11 – j0.03	19.1	54.8	301	61.1	–19
940	2.54 – j4.03	2.45 + j4.12	2.04 – j0.03	19.2	54.8	299	60.8	–18
960	2.90 – j4.64	2.74 + j4.63	1.97 – j0.01	19.1	54.8	300	60.6	–19

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 8. Carrier Side Load Pull Performance — Maximum Drain Efficiency Tuning

V_{DD} = 48 Vdc, I_{DQ} = 862 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	2.39 – j3.65	2.11 + j3.81	1.51 + j1.85	24.3	51.5	140	71.8	–20
940	2.54 – j4.03	2.27 + j4.24	1.43 + j1.84	24.3	51.4	138	71.9	–21
960	2.90 – j4.64	2.60 + j4.68	1.46 + j1.61	23.8	52.2	164	71.6	–20

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	2.39 – j3.65	2.22 + j3.95	1.92 + j1.53	21.5	53.2	207	71.6	–25
940	2.54 – j4.03	2.38 + j4.45	1.74 + j1.57	21.7	52.9	197	71.8	–27
960	2.90 – j4.64	2.66 + j4.94	1.59 + j1.48	21.5	53.1	206	72.0	–27

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

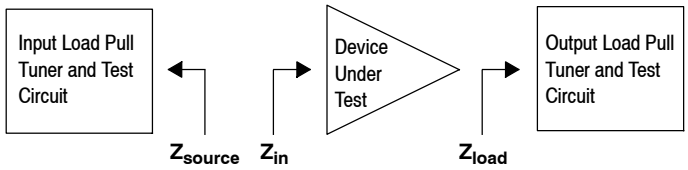


Table 9. Peaking Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 48 Vdc, V_{GSB} = 0.9 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	2.39 – j3.65	2.33 + j3.43	1.52 + j0.07	16.8	54.7	294	66.5	–25
940	2.54 – j4.03	2.44 + j3.87	1.44 + j0.21	16.9	54.6	291	66.9	–25
960	2.90 – j4.64	2.64 + j4.34	1.58 + j0.24	17.0	54.5	283	66.5	–25

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	2.39 – j3.65	2.28 + j3.69	1.68 – j0.06	14.7	55.3	335	66.8	–29
940	2.54 – j4.03	2.40 + j4.15	1.60 + j0.13	14.9	55.2	332	68.0	–30
960	2.90 – j4.64	2.61 + j4.66	1.71 + j0.14	14.9	55.1	325	66.8	–30

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

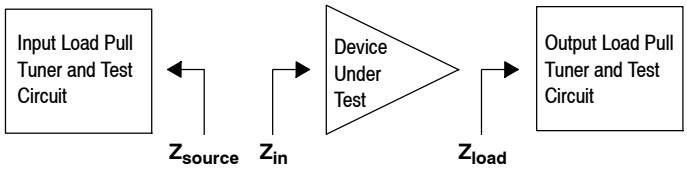
Table 10. Peaking Side Load Pull Performance — Maximum Drain Efficiency Tuning

V_{DD} = 48 Vdc, V_{GSB} = 0.9 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	2.39 – j3.65	2.22 + j3.39	1.81 + j1.79	17.5	52.4	174	78.9	–29
940	2.54 – j4.03	2.27 + j3.80	1.35 + j2.23	17.6	51.2	131	81.4	–35
960	2.90 – j4.64	2.43 + j4.27	1.24 + j2.22	17.6	51.2	131	81.6	–36

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	2.39 – j3.65	2.20 + j3.66	2.07 + j1.45	15.5	53.6	231	77.1	–33
940	2.54 – j4.03	2.31 + j4.12	1.86 + j1.49	15.7	53.6	231	78.9	–36
960	2.90 – j4.64	2.50 + j4.62	1.70 + j1.64	15.8	53.4	218	78.7	–37

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB - TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 940 MHz

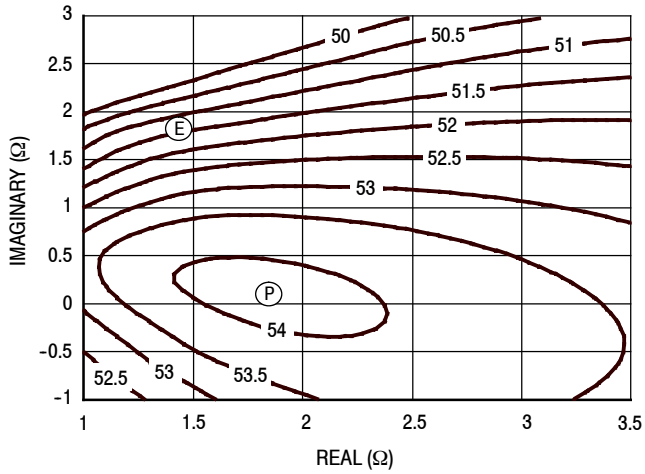


Figure 8. P1dB Load Pull Output Power Contours (dBm)

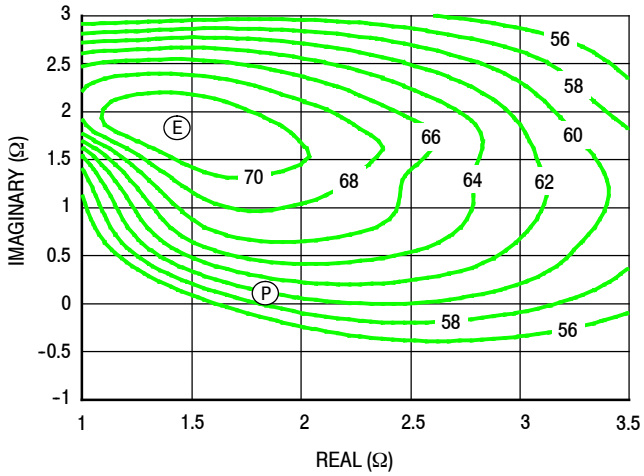


Figure 9. P1dB Load Pull Efficiency Contours (%)

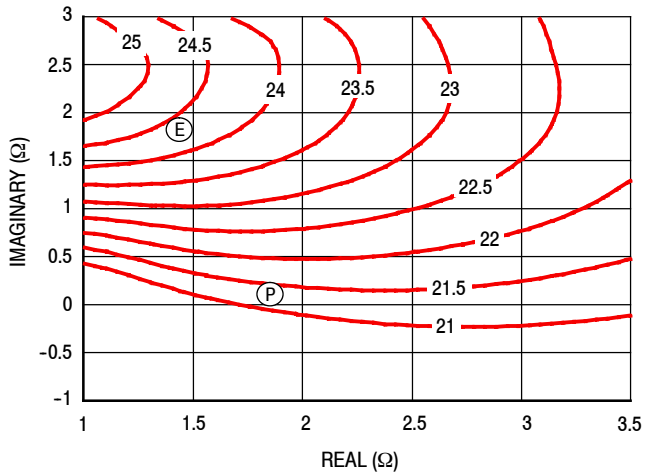


Figure 10. P1dB Load Pull Gain Contours (dB)

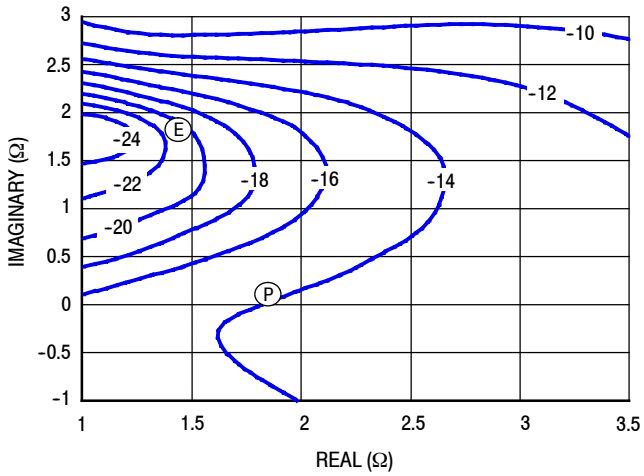


Figure 11. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB - TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 940 MHz

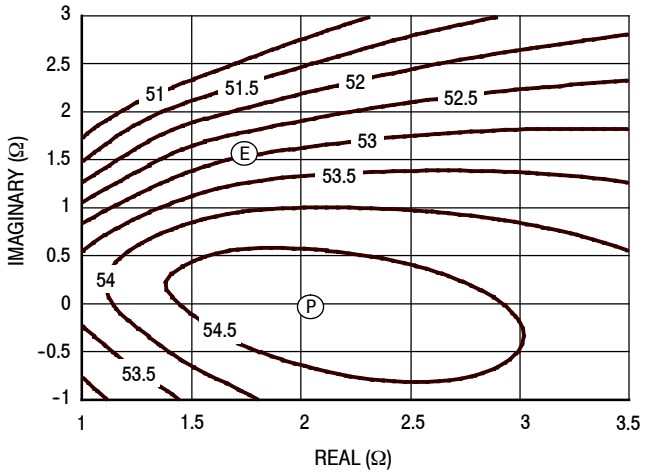


Figure 12. P3dB Load Pull Output Power Contours (dBm)

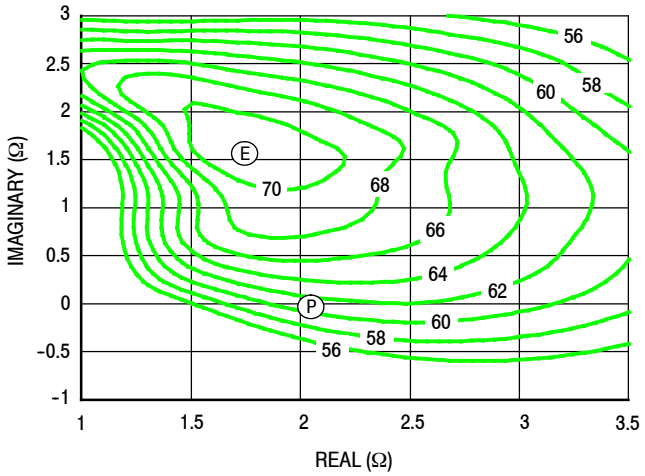


Figure 13. P3dB Load Pull Efficiency Contours (%)

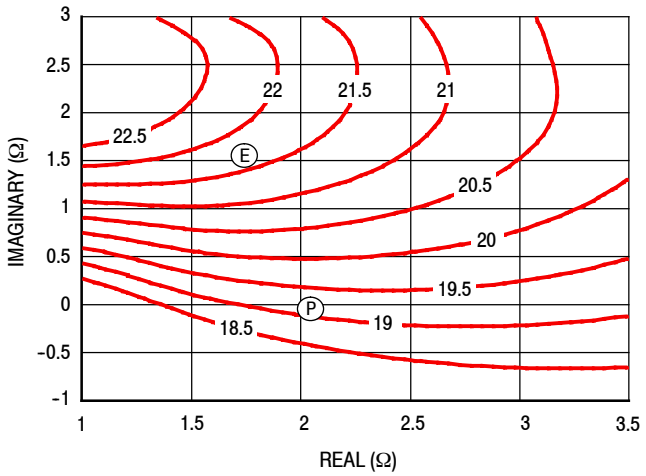


Figure 14. P3dB Load Pull Gain Contours (dB)

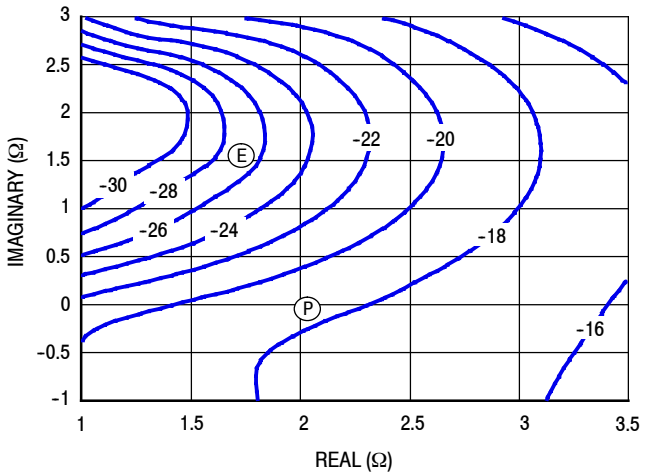


Figure 15. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P1dB - TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 940 MHz

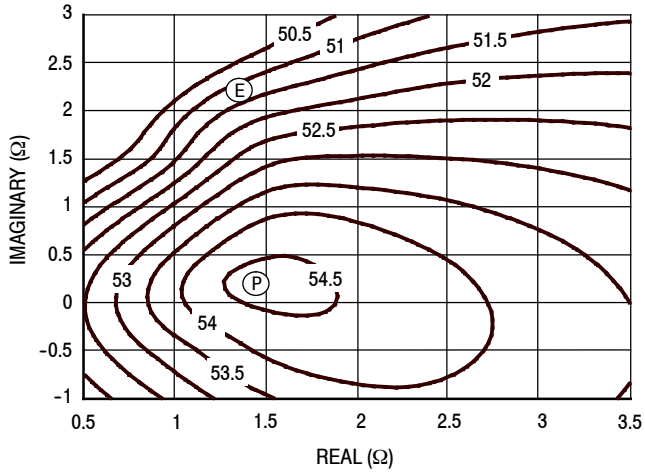


Figure 16. P1dB Load Pull Output Power Contours (dBm)

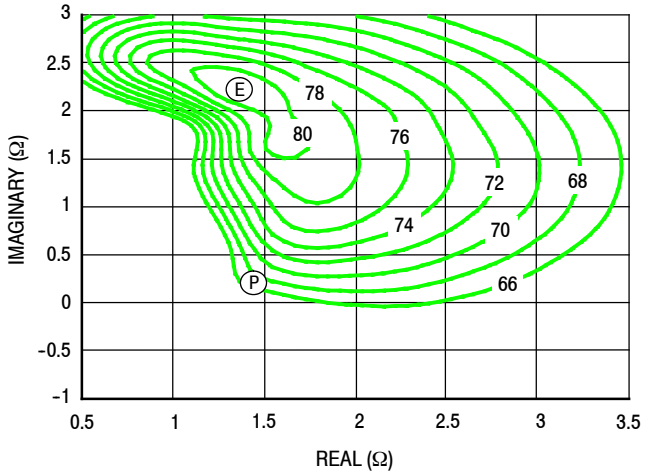


Figure 17. P1dB Load Pull Efficiency Contours (%)

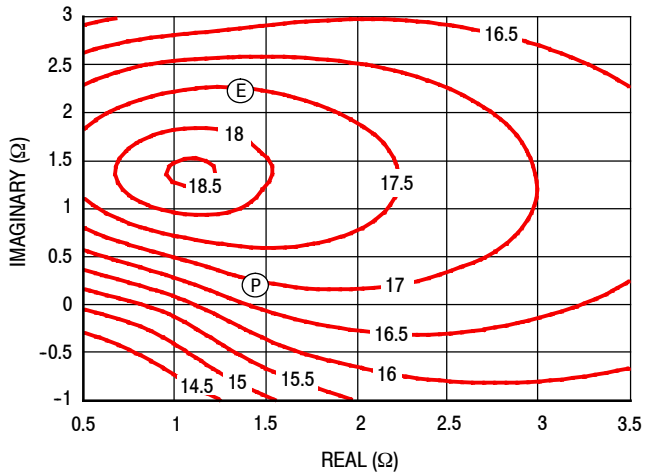


Figure 18. P1dB Load Pull Gain Contours (dB)

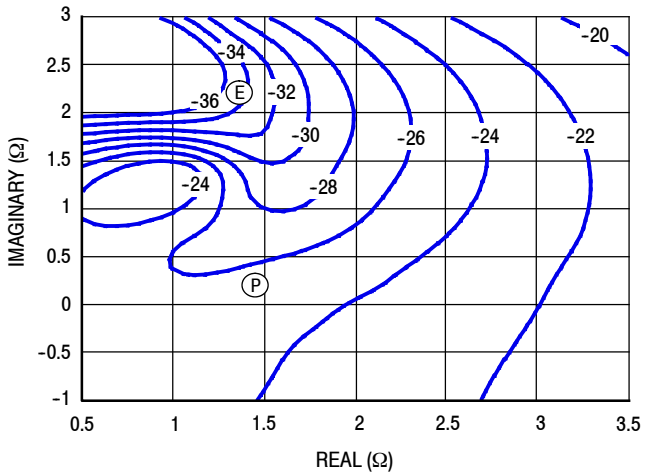


Figure 19. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB - TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 940 MHz

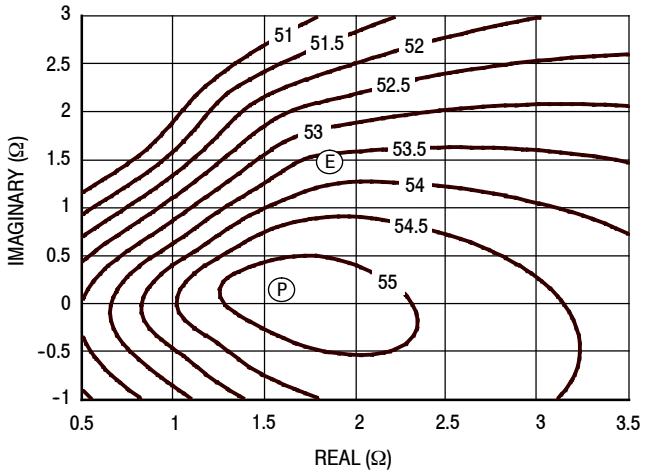


Figure 20. P3dB Load Pull Output Power Contours (dBm)

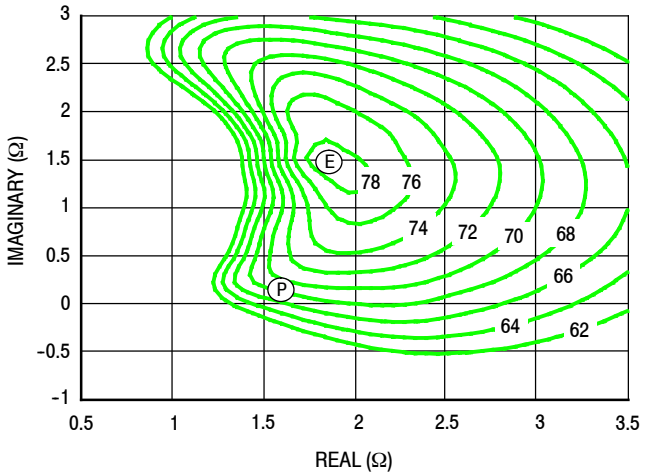


Figure 21. P3dB Load Pull Efficiency Contours (%)

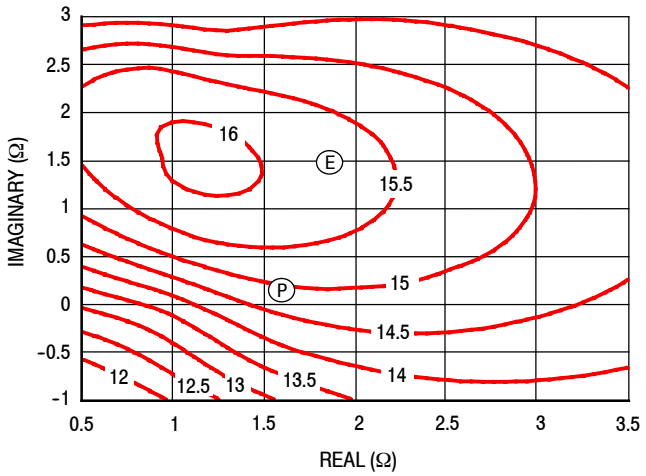


Figure 22. P3dB Load Pull Gain Contours (dB)

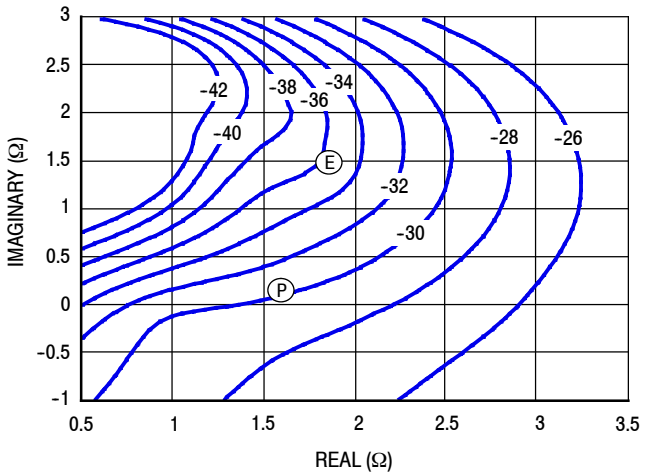


Figure 23. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

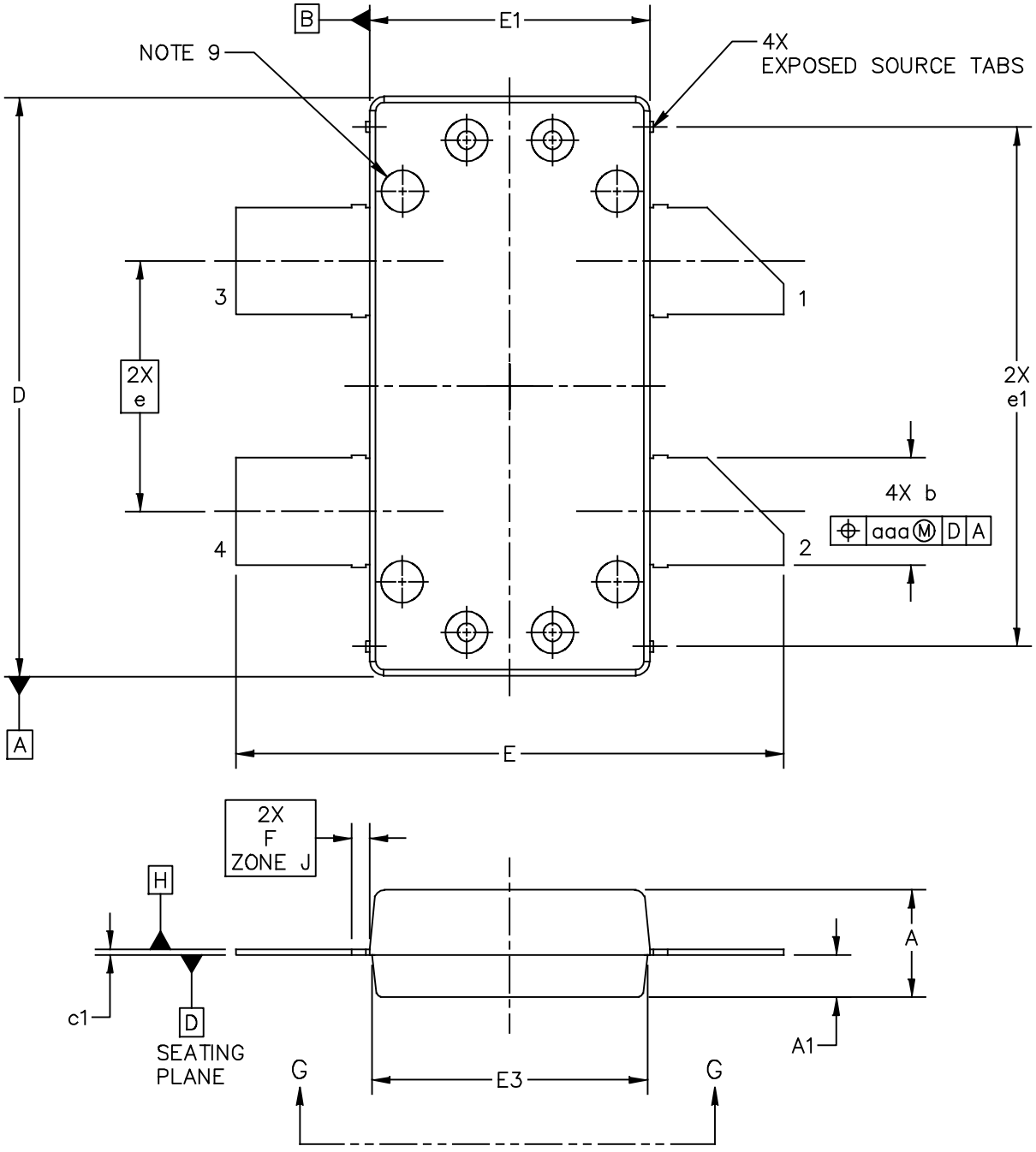
Gain

Drain Efficiency

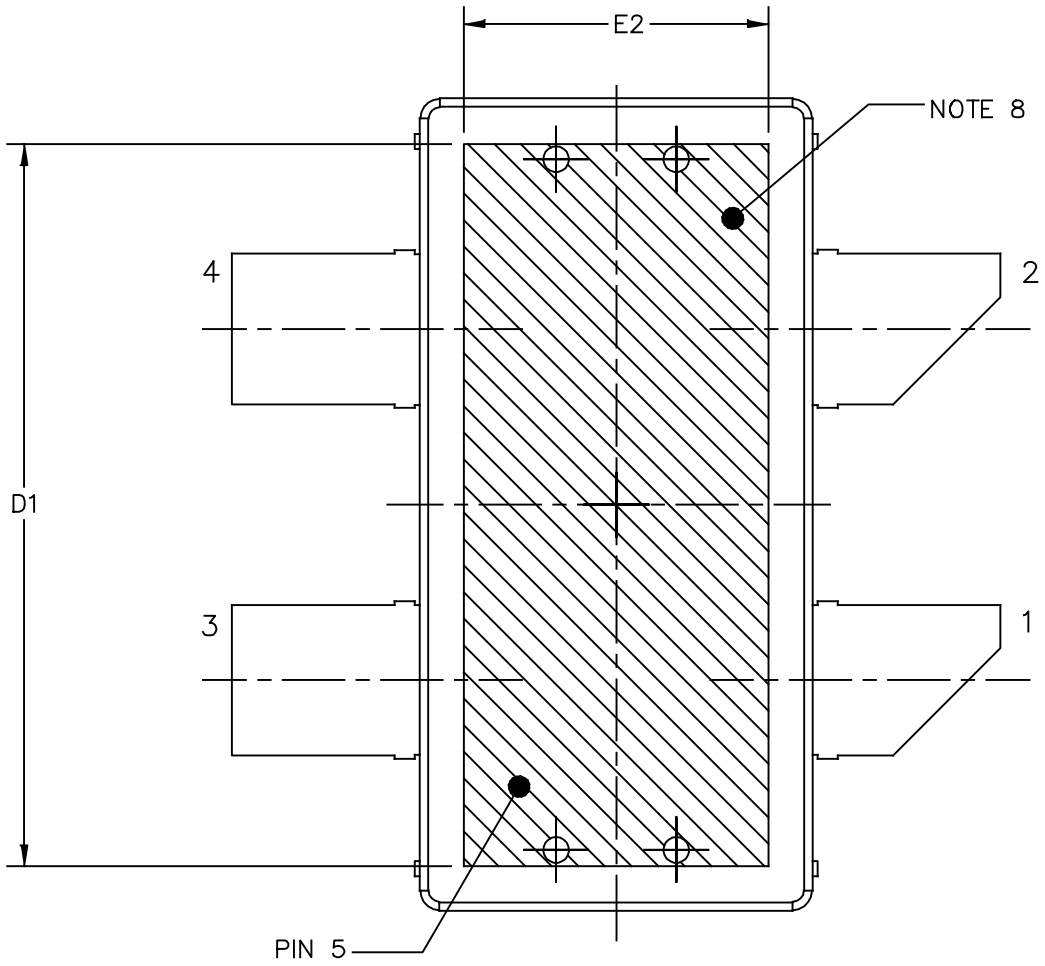
Linearity

Output Power

PACKAGE DIMENSIONS



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BOTTOM VIEW
VIEW G–G

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	CASE NUMBER: 2023–02	10 FEB 2010
	STANDARD: NON–JEDEC	

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE –H– IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.

5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. DATUMS –A– AND –B– TO BE DETERMINED AT DATUM PLANE –H–.

7. DIMENSION A1 APPLIES WITHIN ZONE "J" ONLY.

8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG. THE DIMENSIONS D1 AND E2 REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF HEAT SLUG.

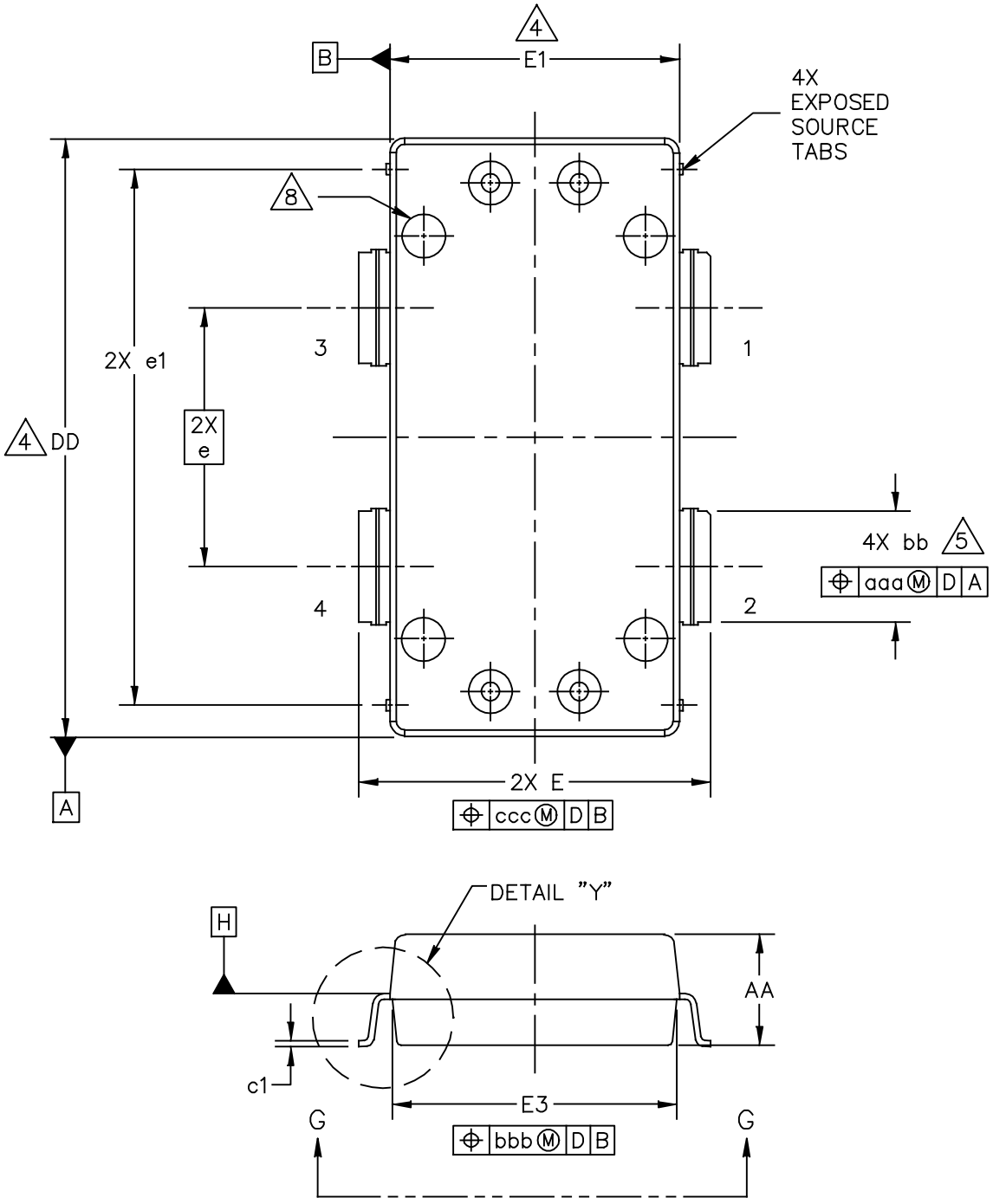
9. DIMPLED HOLE REPRESENTS INPUT SIDE.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	0.148	.152	3.76	3.86	b	.147	.153	3.73	3.89
A1	.059	.065	1.50	1.65	c1	.007	.011	0.18	0.28
D	.808	.812	20.52	20.62	e	.350 BSC		8.89 BSC	
D1	.720	----	18.29	----	e1	.721	.729	18.31	18.52
E	.762	.770	19.36	19.56					
E1	.390	.394	9.91	10.01	aaa	.004		0.10	
E2	.306	----	7.77	----					
E3	.383	.387	9.72	9.83					
F	.025 BSC		0.635 BSC						

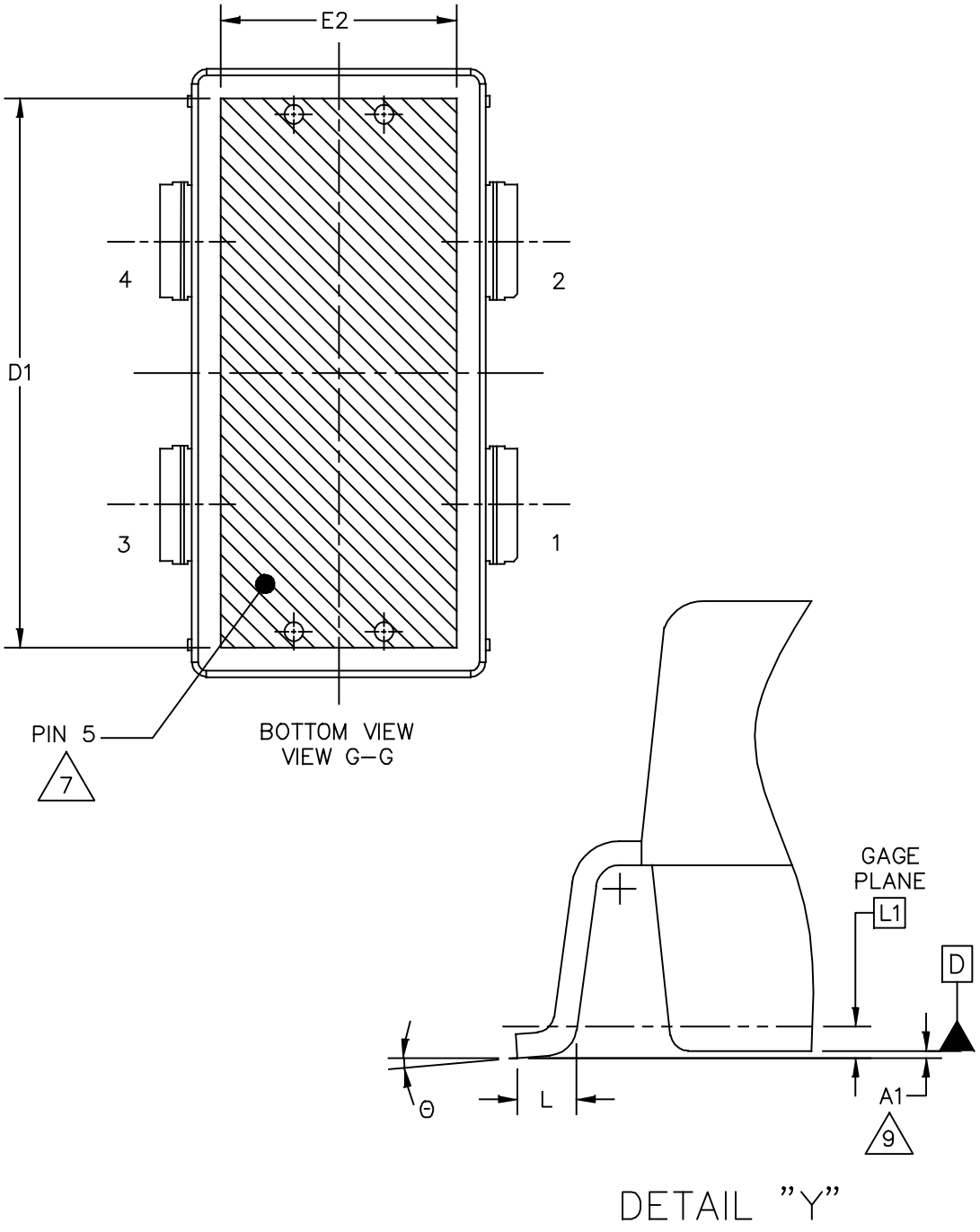
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OM780–4 STRAIGHT LEAD	CASE NUMBER: 2023–02	10 FEB 2010
	STANDARD: NON–JEDEC	



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	STANDARD: NON–JEDEC	
	14 NOV 2013	

NOTES:
1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE H IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS DD AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS DD AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

5. DIMENSION bb DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE bb DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

7. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG. THE DIMENSIONS D1 AND E2 REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF HEAT SLUG.

8. DIMPLED HOLE REPRESENTS INPUT SIDE.

9. DIMENSION A1 IS MEASURED WITH REFERENCE TO DATUM D. THE POSITIVE VALUE IMPLIES THAT THE BOTTOM OF PACKAGE IS HIGHER THAN THE BOTTOM OF THE LEAD.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
AA	.148	.152	3.76	3.86	bb	.147	.153	3.73	3.89
A1	–.002	.002	–0.05	0.05	c1	.007	.011	0.18	0.28
DD	.808	.812	20.52	20.62	e	0.350 BSC		8.89 BSC	
D1	.720	----	18.29	----	e1	.721	.729	18.31	18.52
E	.470	.482	11.94	12.24	Θ	0°	8°	0°	8°
E1	.390	.394	9.91	10.01	aaa	.004		0.10	
E2	.306	----	7.77	----	bbb	.006		0.15	
E3	.383	.387	9.73	9.83	ccc	.010		0.25	
L	.018	.024	0.46	0.61					
L1	.010 BSC		0.25 BSC						

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TITLE:	DOCUMENT NO: 98ASA10834D	REV: D
OM–780G–4L	STANDARD: NON–JEDEC	
	14 NOV 2013	

PRODUCT DOCUMENTATION AND SOFTWARE

Refer to the following documents, software and tools to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator

For Software and Tools, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Feb. 2014	• Initial Release of Data Sheet

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Rev. 0, 2/2014

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