Document Number: MMRF1305H
Rev. 0, 12/2013

RoHS

RF Power LDMOS Transistors

High Ruggedness N-Channel Enhancement-Mode Lateral MOSFETs

MMRF1305HR5
MMRF1305HSR5

RF power transistors suitable for both narrowband and broadband CW or pulse applications operating at frequencies from 1.8 to 2000 MHz, such as military and radio communications and radar. These devices are fabricated using Freescale's enhanced ruggedness platform and are suitable for use in applications where high VSWRs are encountered.

1.8-2000 MHz, 100 W, 50 V
BROADBAND
RF POWER LDMOS TRANSISTORS

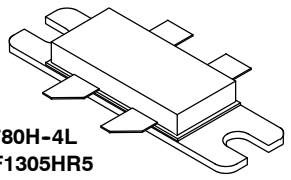
Typical Performance: V_{DD} = 50 Vdc

Frequency (MHz)	Signal Type	P_{out} (W)	G_{ps} (dB)	η_D (%)	IMD (dBc)
30-512 (1,3)	Two-Tone (100 kHz spacing)	100 PEP	19.0	30.0	-30
512 (2)	CW	100	27.2	70.0	—
512 (2)	Pulse (200 μsec, 20% Duty Cycle)	100 Peak	26.0	70.0	—

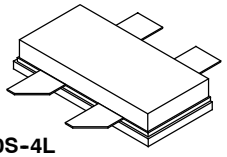
Load Mismatch/Ruggedness

Frequency (MHz)	Signal Type	VSWR	P_{out} (W)	Test Voltage	Result
512 (2)	Pulse (100 μsec, 20% Duty Cycle)	>65:1 at all Phase Angles	130 (3 dB Overdrive)	50	No Device Degradation
512 (2)	CW		126 (3 dB Overdrive)		

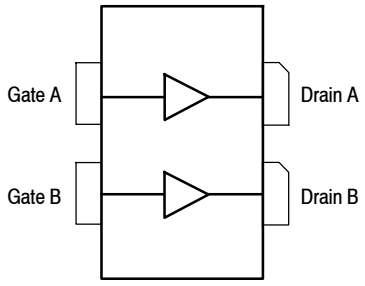
1. Measured in 30-512 MHz broadband reference circuit.
2. Measured in 512 MHz narrowband test circuit.
3. The values shown are the minimum measured performance numbers across the indicated frequency range.



NI-780H-4L
MMRF1305HR5



NI-780S-4L
MMRF1305HSR5



(Top View)

Note: The backside of the package is the source terminal for the transistors.

Figure 1. Pin Connections

Features

- Wide Operating Frequency Range
- Extremely Rugged
- Unmatched, Capable of Very Broadband Operation
- Integrated Stability Enhancements
- Low Thermal Resistance
- Integrated ESD Protection Circuitry
- In Tape and Reel. R5 Suffix = 50 Units, 56 mm Tape Width, 13-inch Reel.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +133	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	-40 to +150	°C
Operating Junction Temperature (4)	T_J	-40 to +225	°C

4. Continuous use at maximum temperature will affect MTTF.

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Table 2. Thermal Characteristics

Characteristic	Symbol	Value (1)	Unit
Thermal Resistance, Junction to Case CW: Case Temperature 81°C, 100 W CW, 50 Vdc, $I_{DQ(A+B)}$ = 100 mA, 512 MHz	$R_{\theta JC}$	0.38	°C/W
Thermal Impedance, Junction to Case Pulse: Case Temperature 73°C, 100 W Peak, 100 μsec Pulse Width, 20% Duty Cycle, 50 Vdc, $I_{DQ(A+B)}$ = 100 mA, 512 MHz	$Z_{\theta JC}$	0.12	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2, passes 2500 V
Machine Model (per EIA/JESD22-A115)	B, passes 250 V
Charge Device Model (per JESD22-C101)	IV, passes 2000 V

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted)

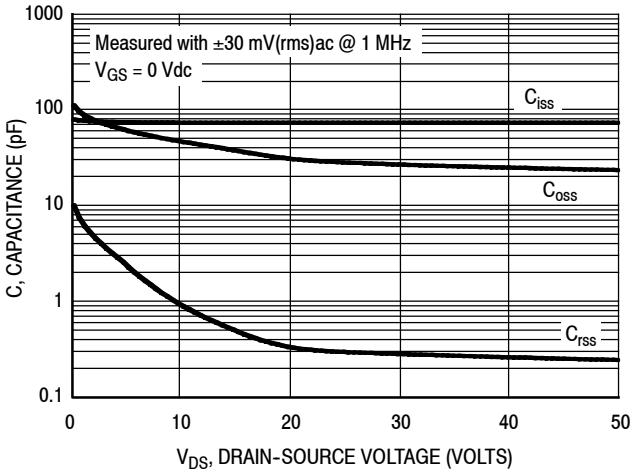
Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics (2)					
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	400	nAdc
Drain-Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 50 mA)	$V_{(BR)DSS}$	133	141	—	Vdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	3	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 100 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
On Characteristics					
Gate Threshold Voltage (2) (V_{DS} = 10 Vdc, I_D = 170 μAdc)	$V_{GS(th)}$	1.6	2.1	2.6	Vdc
Gate Quiescent Voltage (V_{DD} = 50 Vdc, I_D = 100 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	2.1	2.6	3.1	Vdc
Drain-Source On-Voltage (2) (V_{GS} = 10 Vdc, I_D = 1 Adc)	$V_{DS(on)}$	—	0.23	—	Vdc
Dynamic Characteristics (2)					
Reverse Transfer Capacitance (V_{DS} = 50 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	0.24	—	pF
Output Capacitance (V_{DS} = 50 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	23.9	—	pF
Input Capacitance (V_{DS} = 50 Vdc, V_{GS} = 0 Vdc ± 30 mV(rms)ac @ 1 MHz)	C_{iss}	—	73.6	—	pF
Functional Tests (In Freescale Test Fixture, 50 ohm system) V_{DD} = 50 Vdc, $I_{DQ(A+B)}$ = 100 mA, P_{out} = 100 W Peak (20 W Avg.), f = 512 MHz, 200 μsec Pulse Width, 20% Duty Cycle					
Power Gain	G_{ps}	25.0	26.0	27.0	dB
Drain Efficiency	η_D	68.0	70.0	—	%
Input Return Loss	IRL	—	-14	-9	dB

Load Mismatch/Ruggedness (In Freescale Test Fixture, 50 ohm system, $I_{DQ(A+B)}$ = 100 mA)

Frequency (MHz)	Signal Type	VSWR	P_{out} (W)	Test Voltage, V_{DD}	Result
512	Pulse (100 μsec, 20% Duty Cycle)	>65:1 at all Phase Angles	130 Peak (3 dB Overdrive)	50	No Device Degradation
	CW		126 (3 dB Overdrive)		

1. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.
2. Each side of device measured separately.

TYPICAL CHARACTERISTICS



Note: Each side of device measured separately.

Figure 2. Capacitance versus Drain-Source Voltage

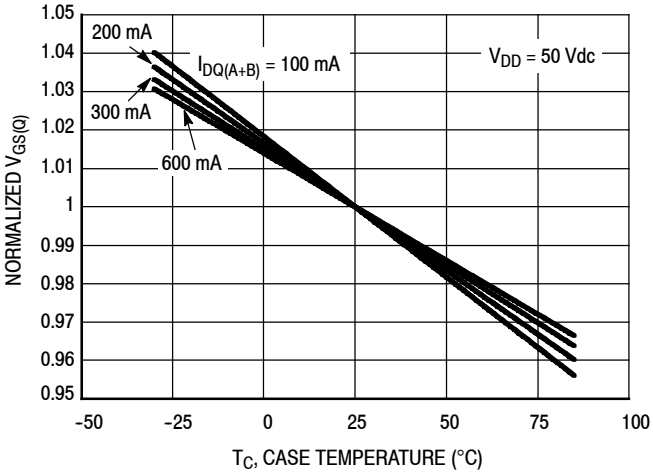
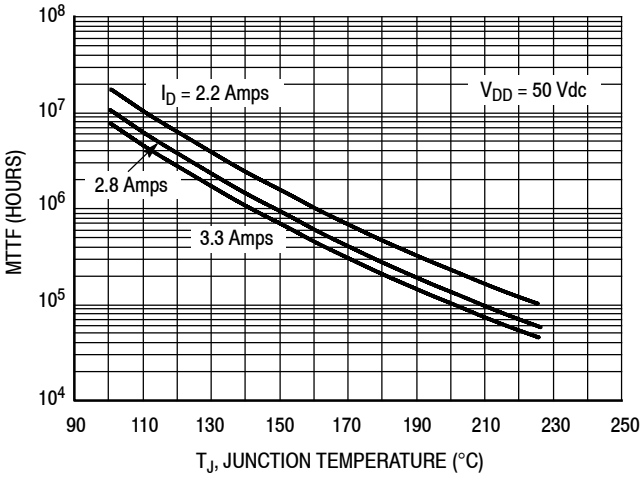


Figure 3. Normalized V_{GS} versus Quiescent Current and Case Temperature

I_{DQ} (mA)	Slope (mV/°C)
100	-1.945
200	-1.826
300	-1.700
600	-1.648



Note: MTTF value represents the total cumulative operating time under indicated test conditions.

MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

Figure 4. MTTF versus Junction Temperature - CW

512 MHz NARROWBAND PRODUCTION TEST FIXTURE

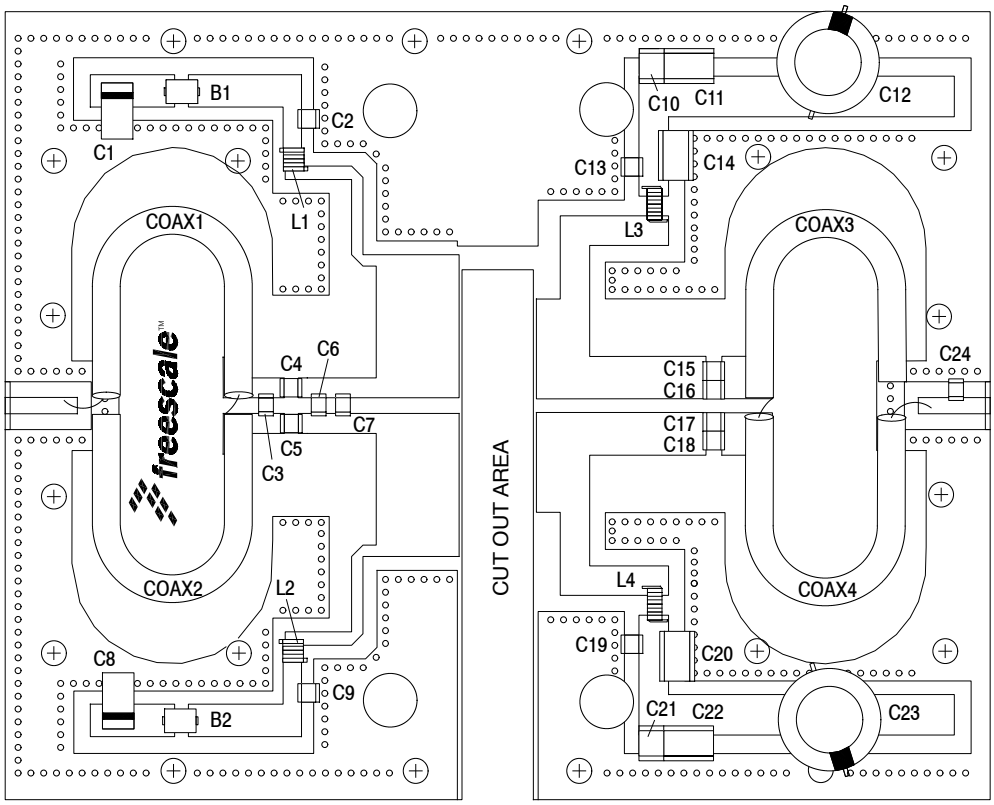


Figure 5. MMRF1305HR5(HSR5) Narrowband Test Circuit Component Layout — 512 MHz

Table 5. MMRF1305HR5(HSR5) Narrowband Test Circuit Component Designations and Values — 512 MHz

Part	Description	Part Number	Manufacturer
B1, B2	Small Ferrite Beads, Surface Mount	2743019447	Fair-Rite
C1, C8	22 μF, 35 V Tantalum Capacitors	T491X226K035AT	Kemet
C2, C9	120 pF Chip Capacitors	ATC100B121JT500XT	ATC
C3	4.3 pF Chip Capacitor	ATC100B4R3CT500XT	ATC
C4, C5	56 pF Chip Capacitors	ATC100B560CT500XT	ATC
C6, C7, C15, C16, C17, C18	27 pF Chip Capacitors	ATC100B270JT500XT	ATC
C10, C21	0.1 μF Chip Capacitors	C1812F104K1RACTU	Kemet
C11, C22	0.01 μF Chip Capacitors	C1825C103K1GACTU	Kemet
C12, C23	470 μF, 63 V Electrolytic Capacitors	MCGPR63V477M13X26-RH	Multicomp
C13, C19	240 pF Chip Capacitors	ATC100B241JT200XT	ATC
C14, C20	2.2 μF Chip Capacitors	G2225X7R225KT3AB	ATC
C24	7.5 pF Chip Capacitor	ATC100B7R5CT500XT	ATC
Coax1, 2	25 Ω Semi Rigid Coax, 2.2″ Shield Length	UT-141C-25	Micro-Coax
Coax3, 4	25 Ω Semi Rigid Coax, 2.0″ Shield Length	UT-141C-25	Micro-Coax
L1, L2	5 Turns, 18.5 nH Inductors, Wire Wound	A05TKLC	Coilcraft
L3, L4	7 Turns, 22 nH Inductors, Wire Wound	B07TJLC	Coilcraft
PCB	0.030″, ε_r = 2.55	AD255D	Arlon

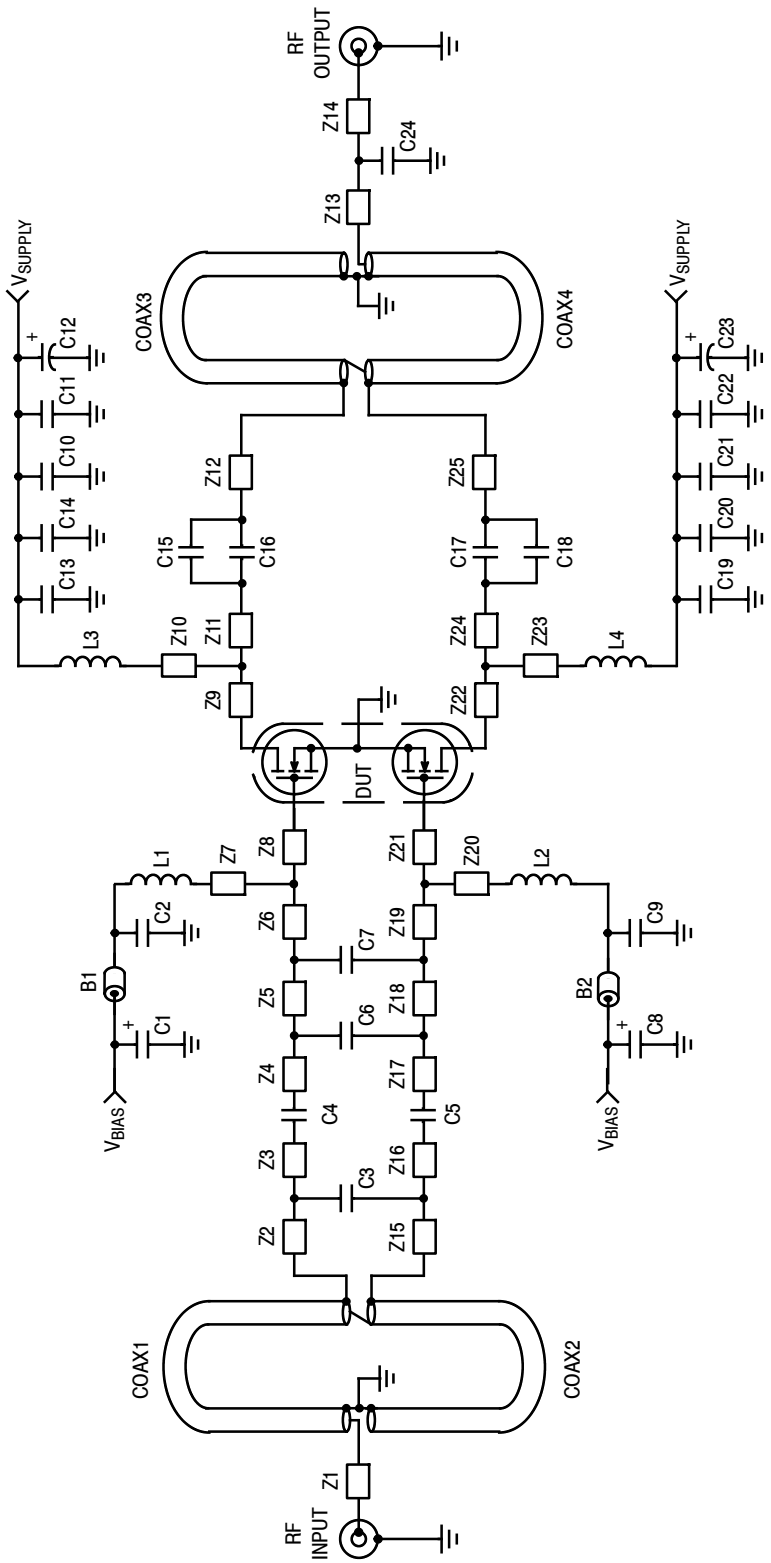


Figure 6. MMRF1305HR5(HSR5) Narrowband Test Circuit Schematic — 512 MHz

Table 6. MMRF1305HR5(HSR5) Narrowband Test Circuit Microstrips — 512 MHz

Microstrip	Description
Z1	0.366″ × 0.082″ Microstrip
Z2, Z15	0.070″ × 0.102″ Microstrip
Z3, Z16	0.094″ × 0.102″ Microstrip
Z4, Z17	0.103″ × 0.102″ Microstrip
Z5, Z18	0.125″ × 0.102″ Microstrip
Z6, Z19	0.168″ × 0.102″ Microstrip
Z7*, Z20*	0.912″ × 0.058″ Microstrip
Z8, Z21	0.420″ × 0.726″ Microstrip
Z9, Z22	0.271″ × 0.507″ Microstrip
Z10*, Z23*	0.822″ × 0.150″ Microstrip
Z11, Z24	0.590″ × 0.216″ Microstrip
Z12, Z25	0.257″ × 0.216″ Microstrip
Z13	0.192″ × 0.082″ Microstrip
Z14	0.173″ × 0.082″ Microstrip

* Line length includes microstrip bends

TYPICAL CHARACTERISTICS — 512 MHz

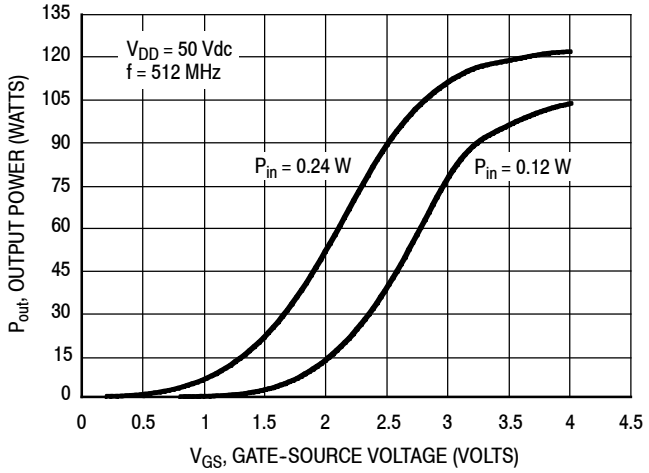
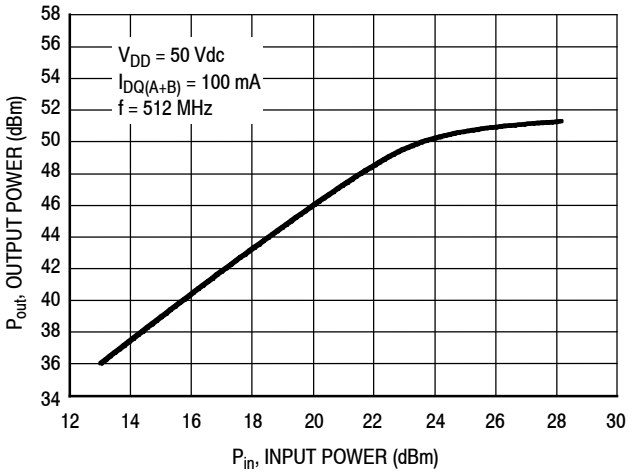


Figure 7. CW Output Power versus Gate-Source Voltage at a Constant Input Power



f (MHz)	P1dB (W)	P3dB (W)
512	117	132

Figure 8. CW Output Power versus Input Power

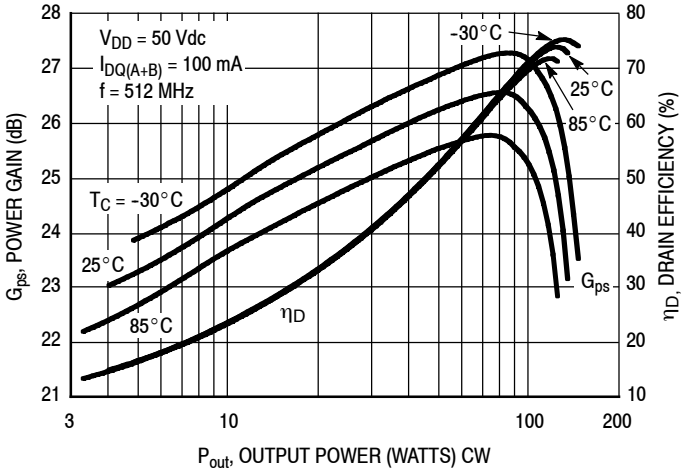


Figure 9. Power Gain and Drain Efficiency versus CW Output Power

512 MHz NARROWBAND PRODUCTION TEST FIXTURE

V_{DD} = 50 Vdc, $I_{DQ(A+B)}$ = 100 mA, P_{out} = 100 W Peak

f MHz	Z_{source} Ω	Z_{load} Ω
512	1.50 + j8.90	12.2 + j18.0

Z_{source} = Test circuit impedance as measured from gate to gate, balanced configuration.

Z_{load} = Test circuit impedance as measured from drain to drain, balanced configuration.

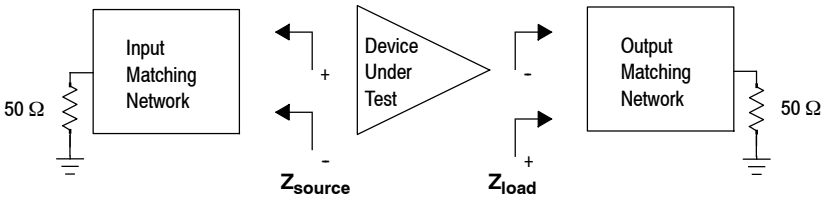


Figure 10. Narrowband Series Equivalent Source and Load Impedance — 512 MHz

Table 7. 30–512 MHz Broadband Performance (In Freescale Reference Circuit, 50 ohm system)
V_{DD} = 50 Volts, $I_{DQ(A+B)}$ = 400 mA

Signal Type	P_{out} (W)	f (MHz)	G_{ps} (dB)	η_D (%)	IMD (dBc)
Two-Tone (200 kHz spacing)	25 PEP	30	24.5	25.3	-37.8
		100	19.6	19.9	-35.7
		512	21.3	20.3	-42.8
	50 PEP	30	24.5	36.7	-29.1
		100	19.9	28.9	-32.9
		512	21.7	29.6	-43.7
	75 PEP	30	23.9	44.6	-24.1
		100	19.4	35.1	-25.1
		512	21.7	36.8	-37.4
	100 PEP	30	23.2	50.7	-20.1
		100	18.8	39.8	-20.4
		512	21.6	42.2	-28.6

30–512 MHz BROADBAND REFERENCE CIRCUIT

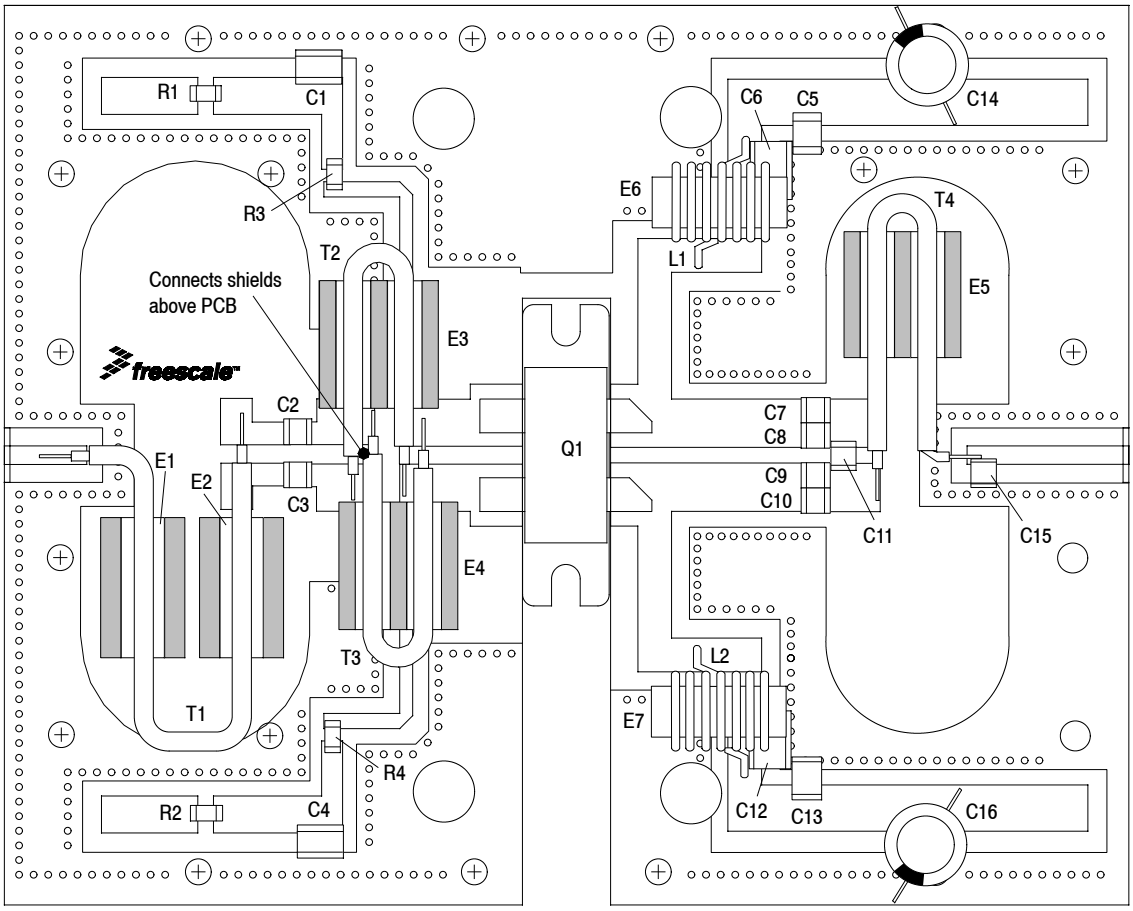


Figure 11. MMRF1305HR5(HSR5) Broadband Reference Circuit Component Layout — 30–512 MHz

Table 8. MMRF1305HR5(HSR5) Broadband Reference Circuit Component Designations and Values — 30–512 MHz

Part	Description	Part Number	Manufacturer
C1, C4	2.2 μF Chip Capacitors	C1825C225J5RAC	Kemet
C2, C3, C7, C8, C9, C10	20K pF Chip Capacitors	ATC200B203KT50XT	ATC
C5, C13	200 nF Chip Capacitors	C1812C224K5RAC-TU	Kemet
C6, C12	2.2 μF Chip Capacitors	G2225X7R225KT3AB	ATC
C11	2.7 pF Chip Capacitor	ATC100B2R7BT500XT	ATC
C14, C16	470 μF, 63 V Electrolytic Capacitors	MCGPR63V477M13X26-RH	Multicomp
C15	2.0 pF Chip Capacitor	ATC100B2R0BT500XT	ATC
E1, E2	#43 Ferrite Beads	2643023402	Fair-Rite
E3, E4, E5	Binocular Toroid K Material	12-365-K	Ferronics
E6, E7	Toroid Ferrite K Material	11–750–K	Ferronics
L1, L2	10 Turns, #18 AWG, Toroid Transformer with Ferrites E6, E7	8075 Copper Magnetic Wire	Belden
Q1	RF Power LDMOS Transistor	MRFE6VP100HR5	Freescale
R1, R2	10 Ω, 1/4 W Chip Resistors	CRCW120610ROJNEA	Vishay
R3, R4	56 Ω, 1/4 W Chip Resistors	CRCW120656ROJNEA	Vishay
T1	50 Ω Flex Cable, 4″	Sucoform 141	Hubert+Suhner
T2, T3	22 Ω Flex Cable, 3.25″	M27500-16RC1509	Whitmor-Wirenetics
T4	25 Ω Semi Rigid, 2.75″	UT-90-25	Micro-Coax
PCB	0.030″, ε_r = 2.55	AD255A	Arlon

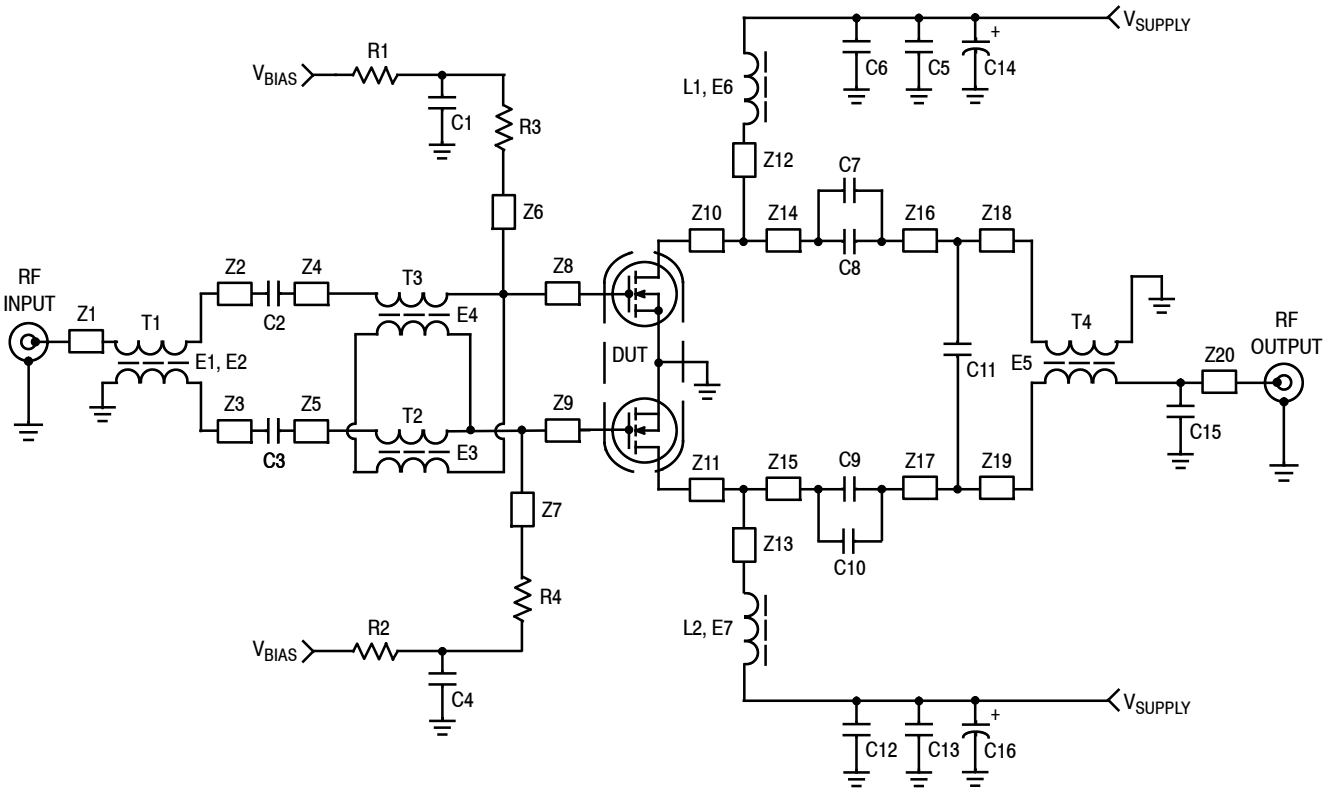


Figure 12. MMRF1305HR5(HSR5) Broadband Test Circuit Schematic — 30–512 MHz

Table 9. MMRF1305HR5(HSR5) Narrowband Test Circuit Microstrips — 30–512 MHz

Microstrip	Description
Z1	0.366″ × 0.082″ Microstrip
Z2, Z3	0.070″ × 0.102″ Microstrip
Z4,Z5	0.094″ × 0.102″ Microstrip
Z6*, Z7*	1.375″ × 0.063″ Microstrip
Z8, Z9	0.561″ × 0.219″ Microstrip
Z10, Z11	0.250″ × 0.219″ Microstrip

Microstrip	Description
Z12*, Z13*	1.125″ × 0.150″ Microstrip
Z14, Z15	0.563″ × 0.219″ Microstrip
Z16, Z17	0.094″ × 0.219″ Microstrip
Z18, Z19	0.156″ × 0.219″ Microstrip
Z20	0.359″ × 0.078″ Microstrip

* Line length includes microstrip bends

TYPICAL CHARACTERISTICS — 30–512 MHz BROADBAND REFERENCE CIRCUIT

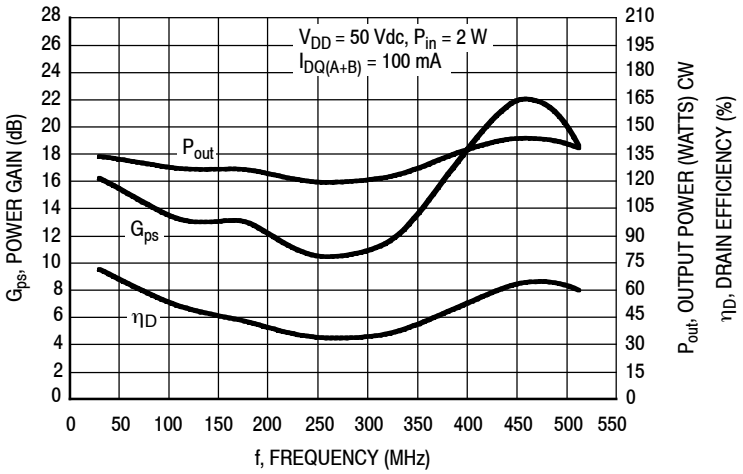


Figure 13. Power Gain, CW Output Power and Drain Efficiency versus Frequency at a Constant Input Power

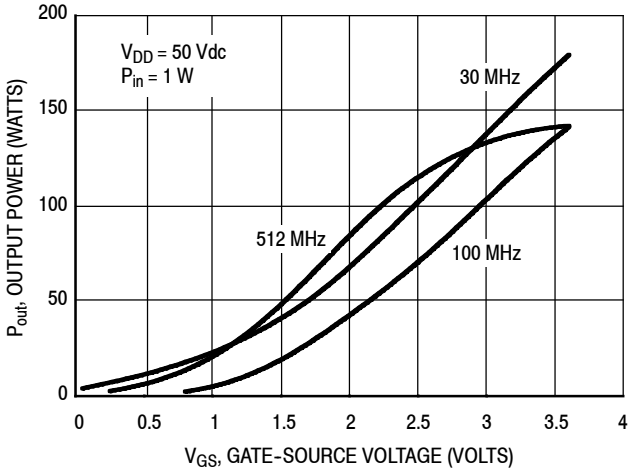


Figure 14. CW Output Power versus Gate-Source Voltage at a Constant Input Power

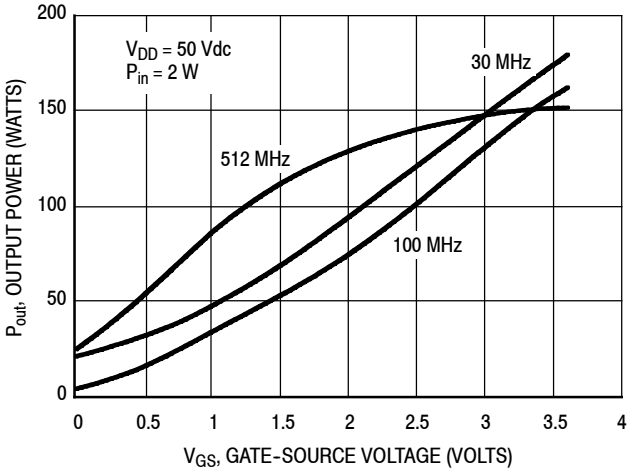
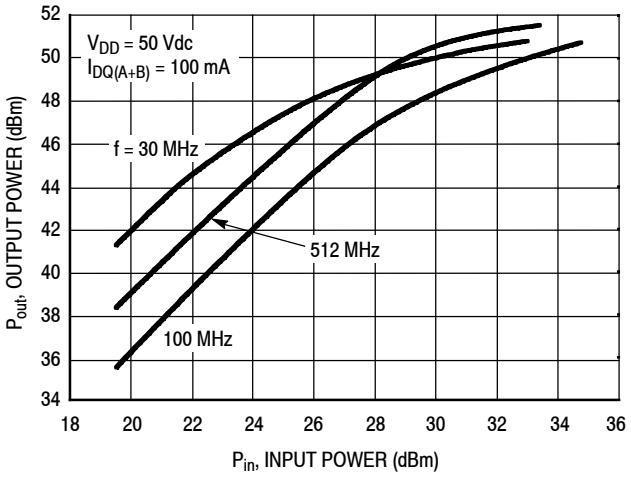


Figure 15. CW Output Power versus Gate-Source Voltage at a Constant Input Power

TYPICAL CHARACTERISTICS — 30–512 MHz BROADBAND REFERENCE CIRCUIT



f (MHz)	P1dB (W)	P3dB (W)
30	78	107
100	81	118
512	123	142

Figure 16. CW Output Power versus Input Power

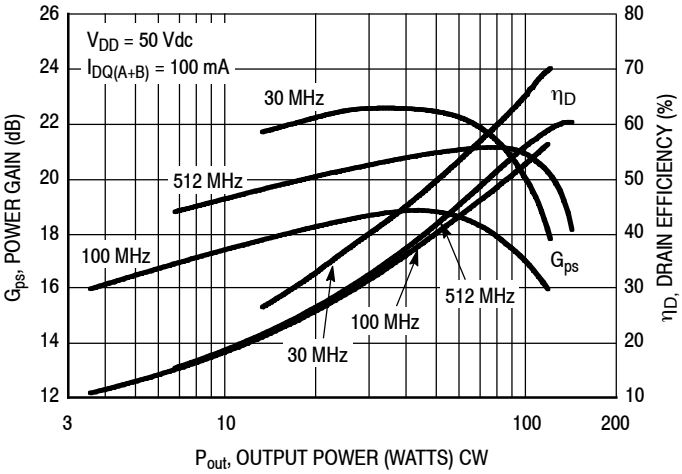


Figure 17. Power Gain and Drain Efficiency versus CW Output Power

TYPICAL CHARACTERISTICS — 30–512 MHz BROADBAND REFERENCE CIRCUIT — TWO-TONE (1)

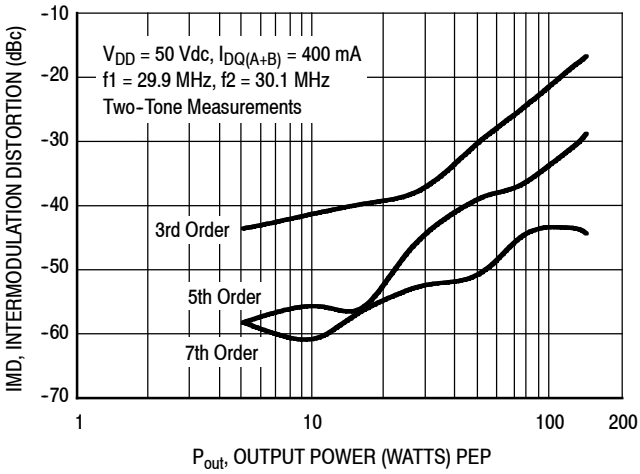


Figure 18. Intermodulation Distortion Products versus Output Power — 30 MHz

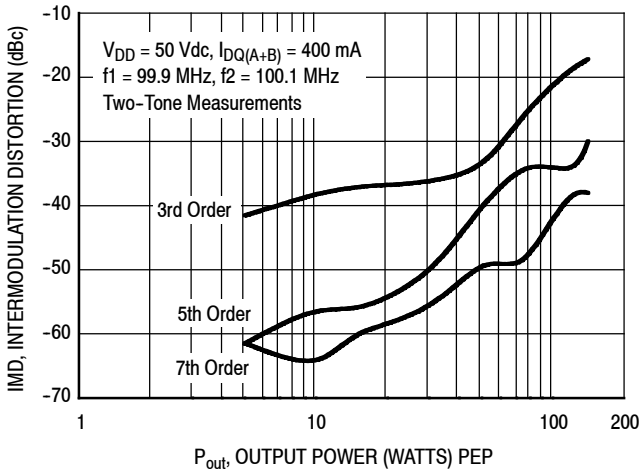


Figure 19. Intermodulation Distortion Products versus Output Power — 100 MHz

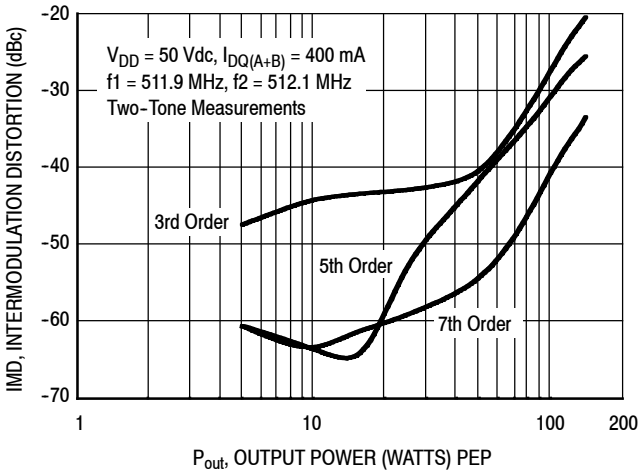
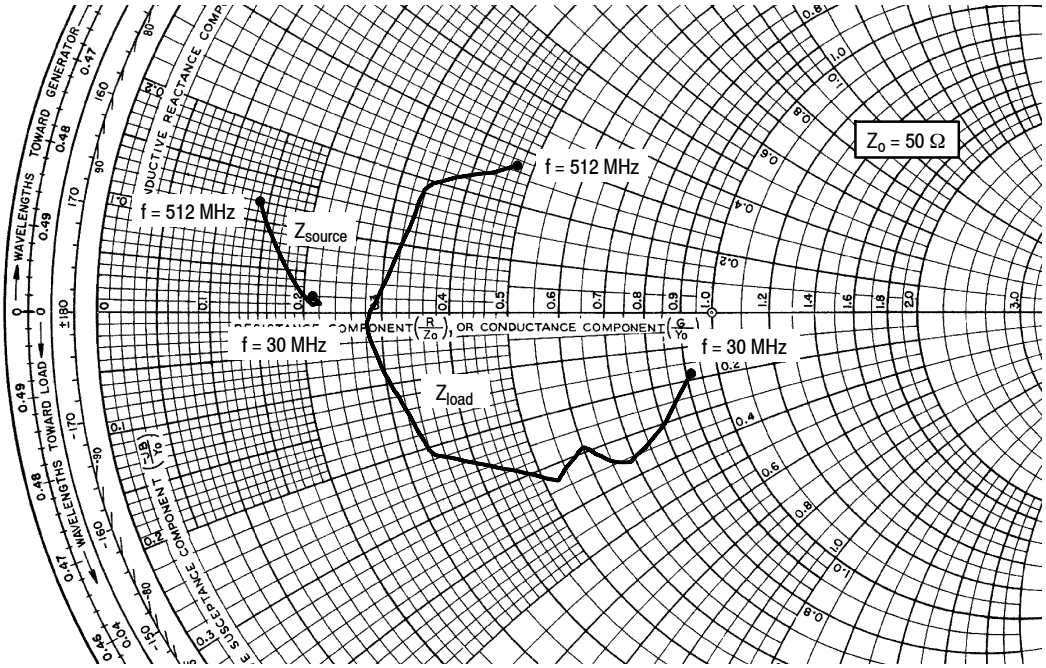


Figure 20. Intermodulation Distortion Products versus Output Power — 520 MHz

1. The distortion products are referenced to one of the two tones and the peak envelope power (PEP) is 6 dB above the power in a single tone.

30–512 MHz BROADBAND REFERENCE CIRCUIT



V_{DD} = 50 Vdc, P_{out} = 100 W CW

f MHz	Z_{source} Ω	Z_{load} Ω
30	10.7 + j1.20	45.8 – j9.00
64	10.9 + j0.70	39.7 – j15.4
88	10.9 + j0.50	33.9 – j18.1
108	10.3 + j0.70	30.0 – j14.4
144	11.0 + j0.70	26.0 – j16.7
170	10.4 + j0.60	21.8 – j13.4
230	9.90 + j0.90	17.0 – j10.7
352	8.90 + j2.30	13.8 – j0.60
450	7.60 + j4.80	16.9 + j9.50
512	7.20 + j6.00	23.7 + j13.5

Z_{source} = Test circuit impedance as measured from gate to gate, balanced configuration.

Z_{load} = Test circuit impedance as measured from drain to drain, balanced configuration.

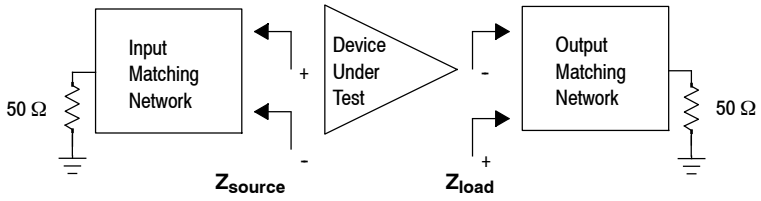
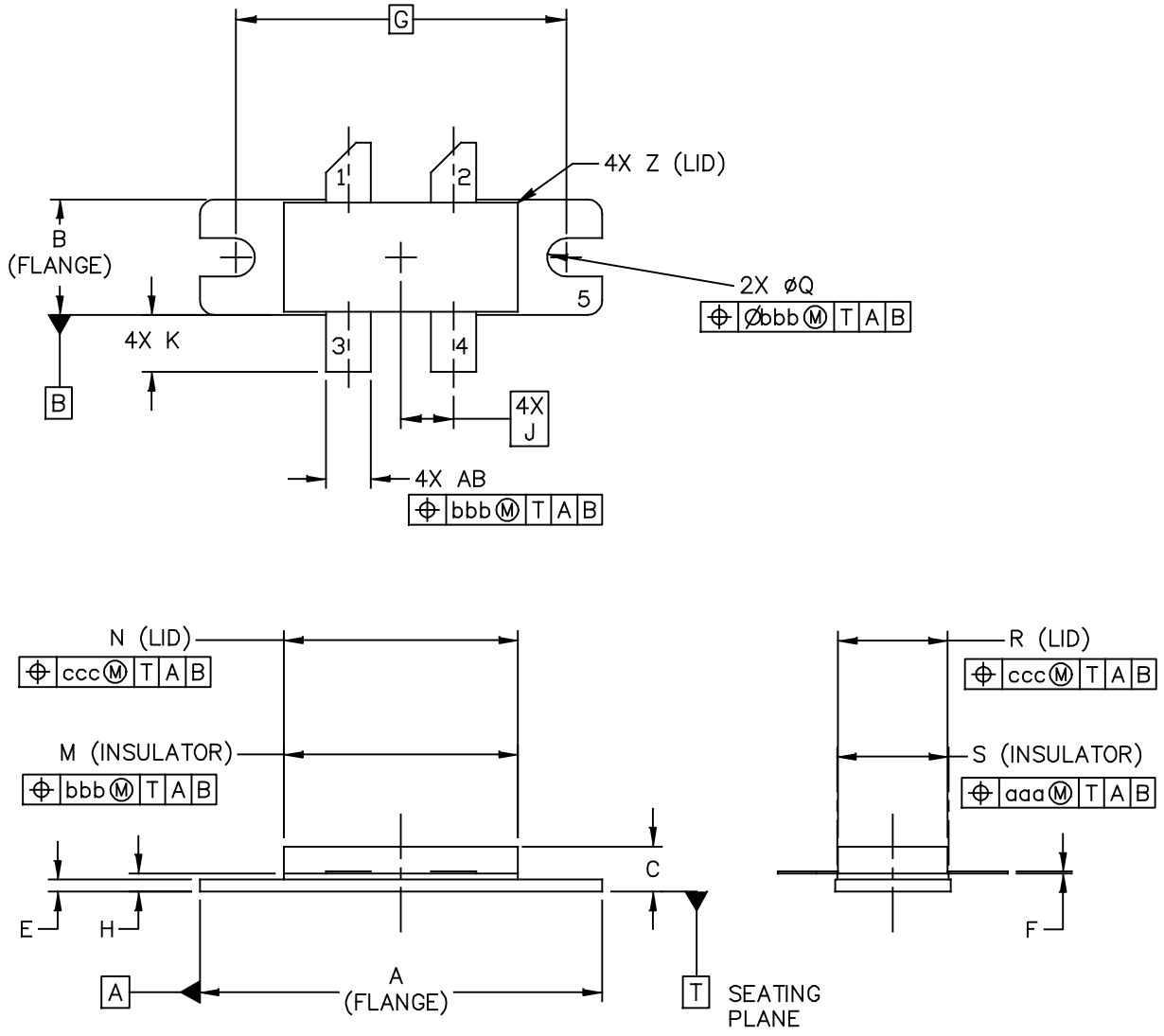


Figure 21. Broadband Series Equivalent Source and Load Impedance — 30–512 MHz

PACKAGE DIMENSIONS



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	CASE NUMBER: 465M-01	27 MAR 2007
	STANDARD: NON-JEDEC	

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1994.

2. CONTROLLING DIMENSION: INCH.

3. DIMENSION H IS MEASURED .030 (0.762) AWAY FROM PACKAGE BODY.

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. GATE
5. SOURCE

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	1.335	1.345	33.91	34.16	R	.365	.375	9.27	9.53
B	.380	.390	9.65	9.91	S	.365	.375	9.27	9.52
C	.125	.170	3.18	4.32	U		.040		1.02
E	.035	.045	0.89	1.14	Z		.030		0.76
F	.003	.006	0.08	0.15	AB	.145	.155	3.68	3.94
G	1.100 BSC		27.94 BSC						
H	.057	.067	1.45	1.7	aaa		.005		0.127
J	.175 BSC		4.44 BSC		bbb		.010		0.254
K	.170	.210	4.32	5.33	ccc		.015		0.381
M	.774	.786	19.61	20.02					
N	.772	.788	19.61	20.02					
Q	ø.118	ø.138	ø3	ø3.51					

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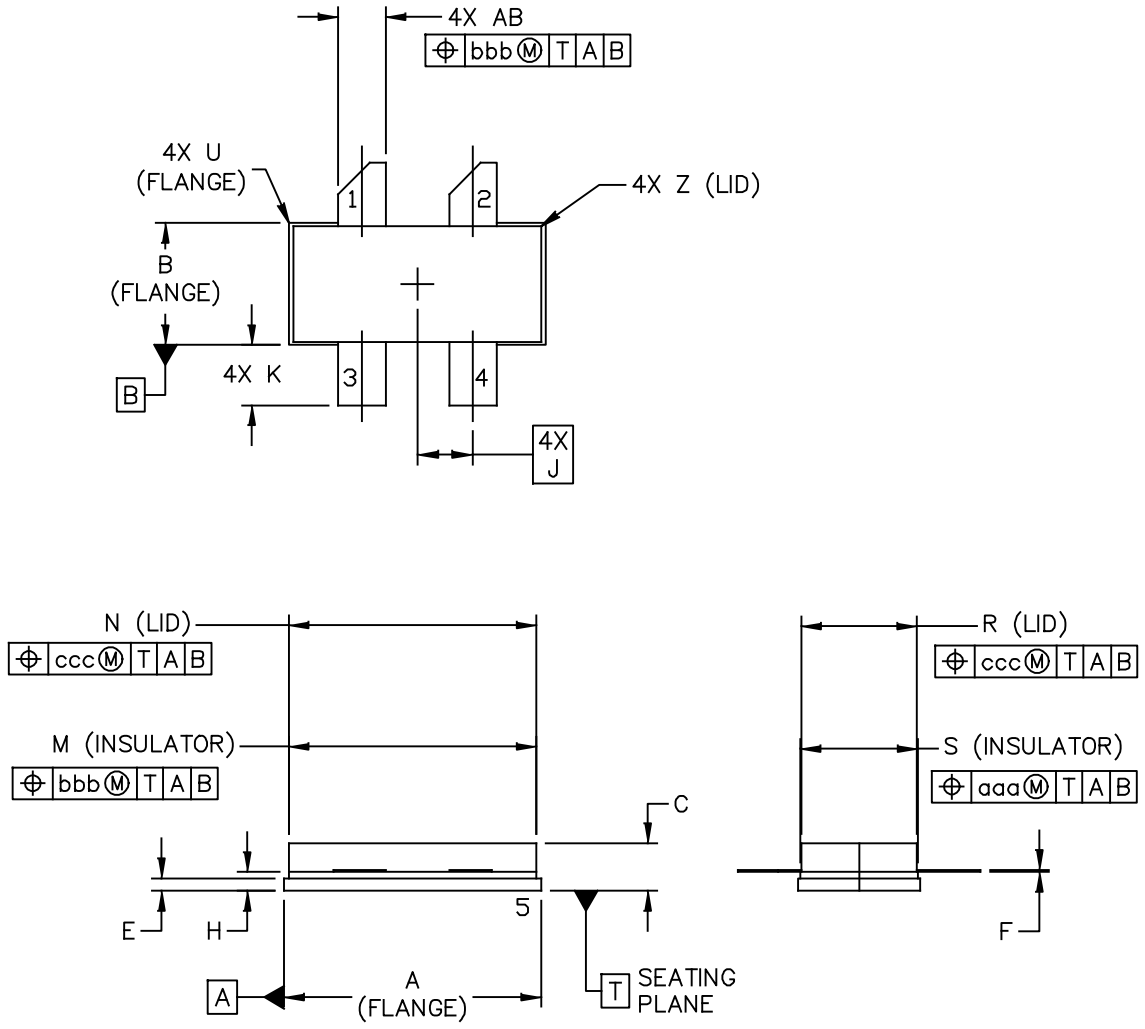
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	STANDARD: NON-JEDEC	

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH.
3. DELETED
4. DIMENSION H IS MEASURED .030 (0.762) AWAY FROM PACKAGE BODY.

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. GATE
5. SOURCE

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	.805	.815	20.45	20.7	U		.040		1.02
B	.380	.390	9.65	9.91	Z		.030		0.76
C	.125	.170	3.18	4.32	AB	.145	.155	3.68	3.94
E	.035	.045	0.89	1.14					
F	.003	.006	0.08	0.15	aaa		.005		0.127
H	.057	.067	1.45	1.7	bbb		.010		0.254
J	.175 BSC		4.44 BSC		ccc		.015		0.381
K	.170	.210	4.32	5.33					
M	.774	.786	19.61	20.02					
N	.772	.788	19.61	20.02					
R	.365	.375	9.27	9.53					
S	.365	.375	9.27	9.52					

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MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE

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NI 780S–4	CASE NUMBER: 465H–02	27 MAR 2007
	STANDARD: NON–JEDEC	

PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Dec. 2013	• Initial Release of Data Sheet

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