Document Number: MRFE6VP5150N
Rev. 1, 7/2014

RoHS

# RF Power LDMOS Transistors

## High Ruggedness N–Channel Enhancement–Mode Lateral MOSFETs

**MRFE6VP5150NR1**
**MRFE6VP5150GNR1**

**1.8–600 MHz, 150 W CW, 50 V WIDEBAND RF POWER LDMOS TRANSISTORS**

These high ruggedness devices are designed for use in high VSWR industrial (including laser and plasma exciters), broadcast (analog and digital), aerospace and radio/land mobile applications. They are unmatched input and output designs allowing wide frequency range utilization, between 1.8 and 600 MHz.

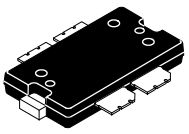
**Typical Performance:** $V_{DD}$ = 50 Vdc

| Frequency (MHz) | Signal Type | $P_{out}$ (W) | $G_{ps}$ (dB) | $\eta_D$ (%) |
|---|---|---|---|---|
| 87.5–108 (1,3) | CW | 179 | 22.5 | 74.6 |
| 230 (2) | CW | 150 | 26.3 | 72.0 |
| 230 (2) | Pulse (100 μsec, 20% Duty Cycle) | 150 Peak | 26.1 | 70.3 |

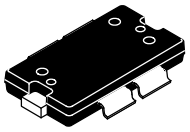
**Load Mismatch/Ruggedness**

| Frequency (MHz) | Signal Type | VSWR | $P_{in}$ (W) | Test Voltage | Result |
|---|---|---|---|---|---|
| 98 (1) | CW | > 65:1 at all Phase Angles | 3.0 (3 dB Overdrive) | 50 | No Device Degradation |
| 230 (2) | Pulse (100 μsec, 20% Duty Cycle) | | 0.62 Peak (3 dB Overdrive) | | |

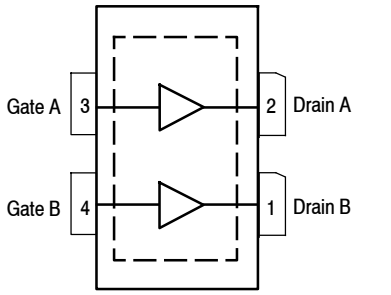
1. Measured in 87.5–108 MHz broadband reference circuit.
2. Measured in 230 MHz narrowband test circuit.
3. The values shown are the minimum measured performance numbers across the indicated frequency range.



**TO-270WB-4**
**PLASTIC**
**MRFE6VP5150NR1**



**TO-270WBG-4**
**PLASTIC**
**MRFE6VP5150GNR1**




(Top View)

Note: Exposed backside of the package is the source terminal for the transistors.

**Figure 1. Pin Connections**

### Features

- Wide Operating Frequency Range
- Extreme Ruggedness
- Unmatched Input and Output Allowing Wide Frequency Range Utilization
- Integrated Stability Enhancements
- Low Thermal Resistance
- Integrated ESD Protection Circuitry
- In Tape and Reel. R1 Suffix = 500 Units, 44 mm Tape Width, 13–inch Reel.

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**Table 1. Maximum Ratings**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain-Source Voltage | $V_{DSS}$ | –0.5, +133 | Vdc |
| Gate-Source Voltage | $V_{GS}$ | –6.0, +10 | Vdc |
| Storage Temperature Range | $T_{stg}$ | –65 to +150 | °C |
| Case Operating Temperature Range | $T_C$ | –40 to +150 | °C |
| Operating Junction Temperature Range (1,2) | $T_J$ | –40 to +225 | °C |
| Total Device Dissipation @ $T_C$ = 25°C<br>Derate above 25°C | $P_D$ | 952<br>4.76 | W<br>W/°C |

**Table 2. Thermal Characteristics**

| Characteristic | Symbol | Value (2,3) | Unit |
|---|---|---|---|
| Thermal Resistance, Junction to Case<br>CW: Case Temperature 80°C, 150 W CW, 50 Vdc, $I_{DQ(A+B)}$ = 100 mA, 230 MHz | $R_{\theta JC}$ | 0.21 | °C/W |
| Thermal Impedance, Junction to Case<br>Pulse: Case Temperature 66°C, 150 W Peak, 100 μsec Pulse Width,<br>20% Duty Cycle, 50 Vdc, $I_{DQ(A+B)}$ = 100 mA, 230 MHz | $Z_{\theta JC}$ | 0.04 | °C/W |

**Table 3. ESD Protection Characteristics**

| Test Methodology | Class |
|---|---|
| Human Body Model (per JESD22-A114) | 2, passes 2500 V |
| Machine Model (per EIA/JESD22-A115) | B, passes 250 V |
| Charge Device Model (per JESD22-C101) | IV, passes 1200 V |

**Table 4. Moisture Sensitivity Level**

| Test Methodology | Rating | Package Peak Temperature | Unit |
|---|---|---|---|
| Per JESD22-A113, IPC/JEDEC J-STD-020 | 3 | 260 | °C |

**Table 5. Electrical Characteristics** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Off Characteristics (4)** | | | | | |
| Gate-Source Leakage Current<br>($V_{GS}$ = 5 Vdc, $V_{DS}$ = 0 Vdc) | $I_{GSS}$ | — | — | 1 | μAdc |
| Drain-Source Breakdown Voltage<br>($V_{GS}$ = 0 Vdc, $I_D$ = 50 mAdc) | $V_{(BR)DSS}$ | 133 | 139 | — | Vdc |
| Zero Gate Voltage Drain Leakage Current<br>($V_{DS}$ = 50 Vdc, $V_{GS}$ = 0 Vdc) | $I_{DSS}$ | — | — | 5 | μAdc |
| Zero Gate Voltage Drain Leakage Current<br>($V_{DS}$ = 100 Vdc, $V_{GS}$ = 0 Vdc) | $I_{DSS}$ | — | — | 10 | μAdc |
| **On Characteristics** | | | | | |
| Gate Threshold Voltage (4)<br>($V_{DS}$ = 10 Vdc, $I_D$ = 480 μAdc) | $V_{GS(th)}$ | 1.8 | 2.4 | 2.8 | Vdc |
| Gate Quiescent Voltage<br>($V_{DD}$ = 50 Vdc, $I_D$ = 100 mAdc, Measured in Functional Test) | $V_{GS(Q)}$ | 2.3 | 2.8 | 3.3 | Vdc |
| Drain-Source On-Voltage (4)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 1 Adc) | $V_{DS(on)}$ | — | 0.26 | — | Vdc |

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.
4. Each side of device measured separately.

(continued)

**Table 5. Electrical Characteristics** ($T_A$ = 25°C unless otherwise noted) **(continued)**

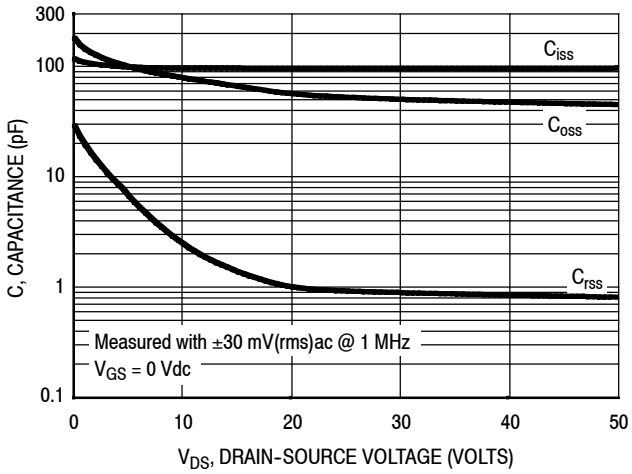
| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Dynamic Characteristics** (1) | | | | | |
| Reverse Transfer Capacitance ($V_{DS}$ = 50 Vdc ± 30 mV(rms)ac @ 1 MHz, $V_{GS}$ = 0 Vdc) | $C_{rss}$ | — | 0.8 | — | pF |
| Output Capacitance ($V_{DS}$ = 50 Vdc ± 30 mV(rms)ac @ 1 MHz, $V_{GS}$ = 0 Vdc) | $C_{oss}$ | — | 45.4 | — | pF |
| Input Capacitance ($V_{DS}$ = 50 Vdc, $V_{GS}$ = 0 Vdc ± 30 mV(rms)ac @ 1 MHz) | $C_{iss}$ | — | 96.7 | — | pF |
| **Functional Tests** (2) (In Freescale Test Fixture, 50 ohm system) $V_{DD}$ = 50 Vdc, $I_{DQ(A+B)}$ = 100 mA, $P_{out}$ = 150 W Peak (30 W Avg.), f = 230 MHz, 100 μsec Pulse Width, 20% Duty Cycle | | | | | |
| Power Gain | $G_{ps}$ | 25.0 | 26.1 | 27.5 | dB |
| Drain Efficiency | $\eta_D$ | 68.0 | 70.3 | — | % |
| Input Return Loss | IRL | — | –16 | –9 | dB |

**Load Mismatch/Ruggedness** (In Freescale Test Fixture) 50 ohm system, $I_{DQ(A+B)}$ = 100 mA

| Frequency (MHz) | Signal Type | VSWR | $P_{in}$ (W) | Test Voltage, $V_{DD}$ | Result |
|---|---|---|---|---|---|
| 230 | Pulse (100 μsec, 20% Duty Cycle) | > 65:1 at all Phase Angles | 0.62 Peak (3 dB Overdrive) | 50 | No Device Degradation |

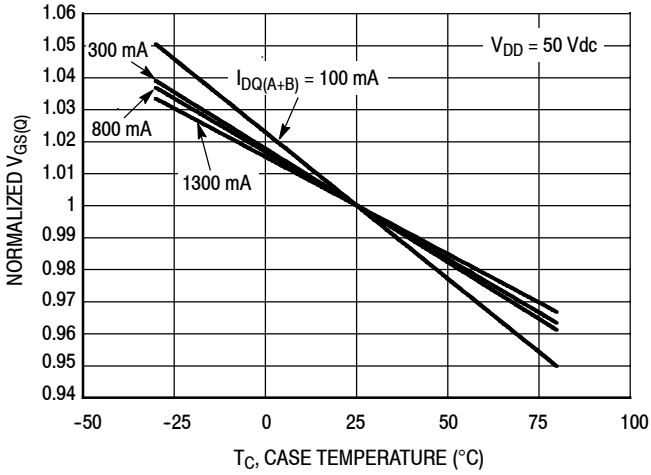
1. Each side of device measured separately.
2. Measurements made with device in straight lead configuration before any lead forming operation is applied. Lead forming is used for gull wing (GN) parts.

## TYPICAL CHARACTERISTICS



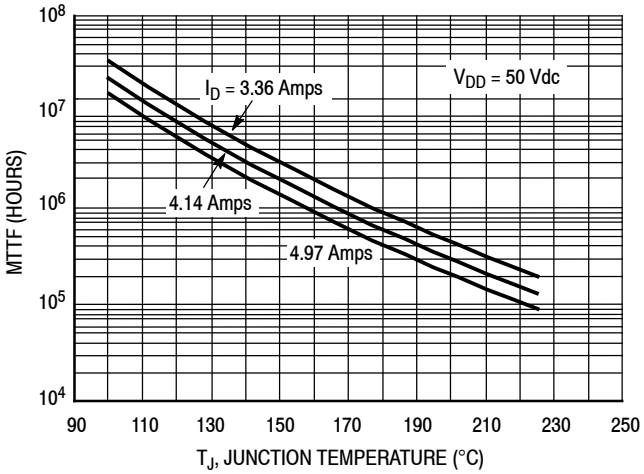

**Note:** Each side of device measured separately.

**Figure 2. Capacitance versus Drain-Source Voltage**




| $I_{DQ}$ (mA) | Slope (mV/°C) |
|---|---|
| 100 | –2.466 |
| 300 | –2.058 |
| 800 | –2.015 |
| 1300 | –1.877 |

**Figure 3. Normalized $V_{GS}$ versus Quiescent Current and Case Temperature**




**Note:** MTTF value represents the total cumulative operating time under indicated test conditions.

MTTF calculator available at http:/www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

**Figure 4. MTTF versus Junction Temperature – CW**

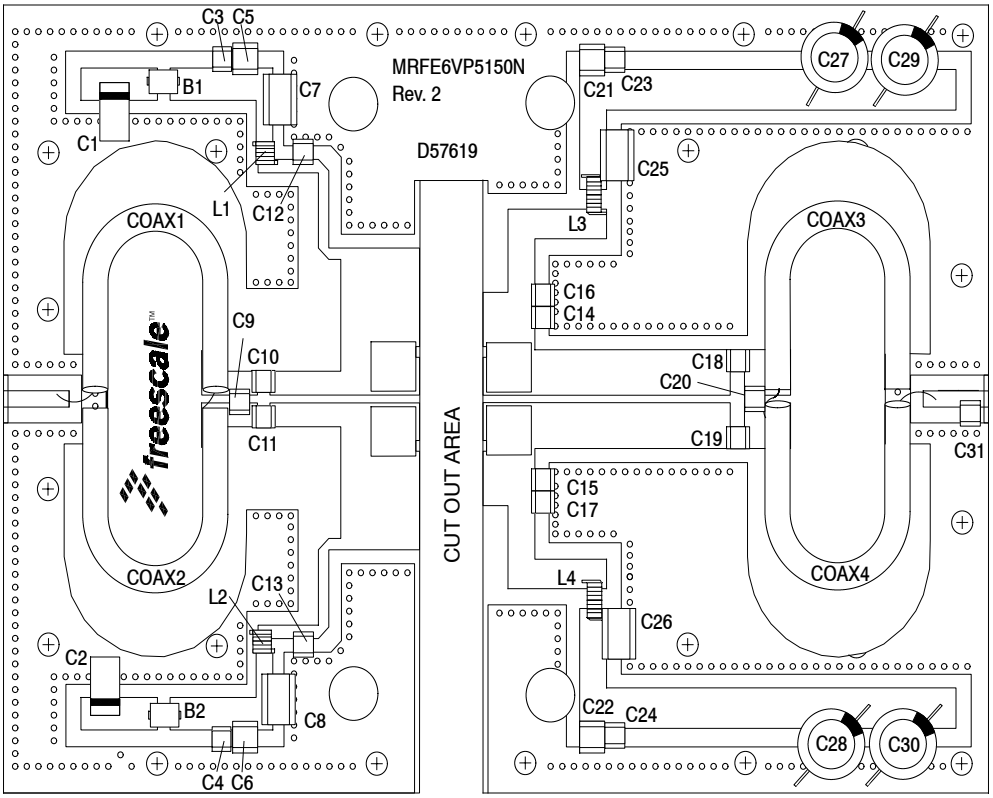



**Figure 5. MRFE6VP5150NR1 Narrowband Test Circuit Component Layout — 230 MHz**

**Table 6. MRFE6VP5150NR1 Narrowband Test Circuit Component Designations and Values — 230 MHz**

| Part | Description | Part Number | Manufacturer |
|---|---|---|---|
| B1, B2 | Small Ferrite Beads, Surface Mount | 2743019447 | Fair-Rite |
| C1, C2 | 22 μF, 35 V Tantalum Capacitors | T491X226K035AT | Kemet |
| C3, C4, C23, C24 | 0.1 μF Chip Capacitors | CDR33BX104AKWS | AVX |
| C5, C6 | 220 nF Chip Capacitors | C1812C224K5RACTU | Kemet |
| C7, C8 | 2.2 μF Chip Capacitors | C1825C225J5RACTU | Kemet |
| C9 | 2.2 pF Chip Capacitor | ATC100B2R2JT500XT | ATC |
| C10, C11 | 18 pF Chip Capacitors | ATC100B180JT500XT | ATC |
| C12, C13 | 330 pF Chip Capacitors | ATC100B331JT200XT | ATC |
| C14, C15 | 39 pF Chip Capacitors | ATC100B390JT500XT | ATC |
| C16, C17 | 15 pF Chip Capacitors | ATC100B150JT500XT | ATC |
| C18, C19 | 1000 pF Chip Capacitors | ATC100B102JT50XT | ATC |
| C20 | 82 pF Chip Capacitor | ATC100B820JT500XT | ATC |
| C21, C22 | 0.10 μF Chip Capacitors | C1812F104K1RACTU | Kemet |
| C25, C26 | 2.2 μF Chip Capacitors | 2225X7R225KT3AB | ATC |
| C27, C28, C29, C30 | 470 μF, 63 V Electrolytic Capacitors | MCGPR63V477M13X26-RH | Multicomp |
| C31 | 36 pF Chip Capacitor | ATC100B360JT500XT | ATC |
| Coax1, 2, 3, 4 | 25 Ω SemiRigid Coax, 2.4″ | UT-141C-25 | Micro-Coax |
| L1, L2 | 3 Turns, 12 nH Inductors | GA3094-ALC | Coilcraft |
| L3, L4 | 4 Turns, 17.5 nH Inductors | GA3095-ALC | Coilcraft |
| PCB | Arlon AD255A, 0.030″, $\varepsilon_r$ = 2.55 | D57619 | MTL |

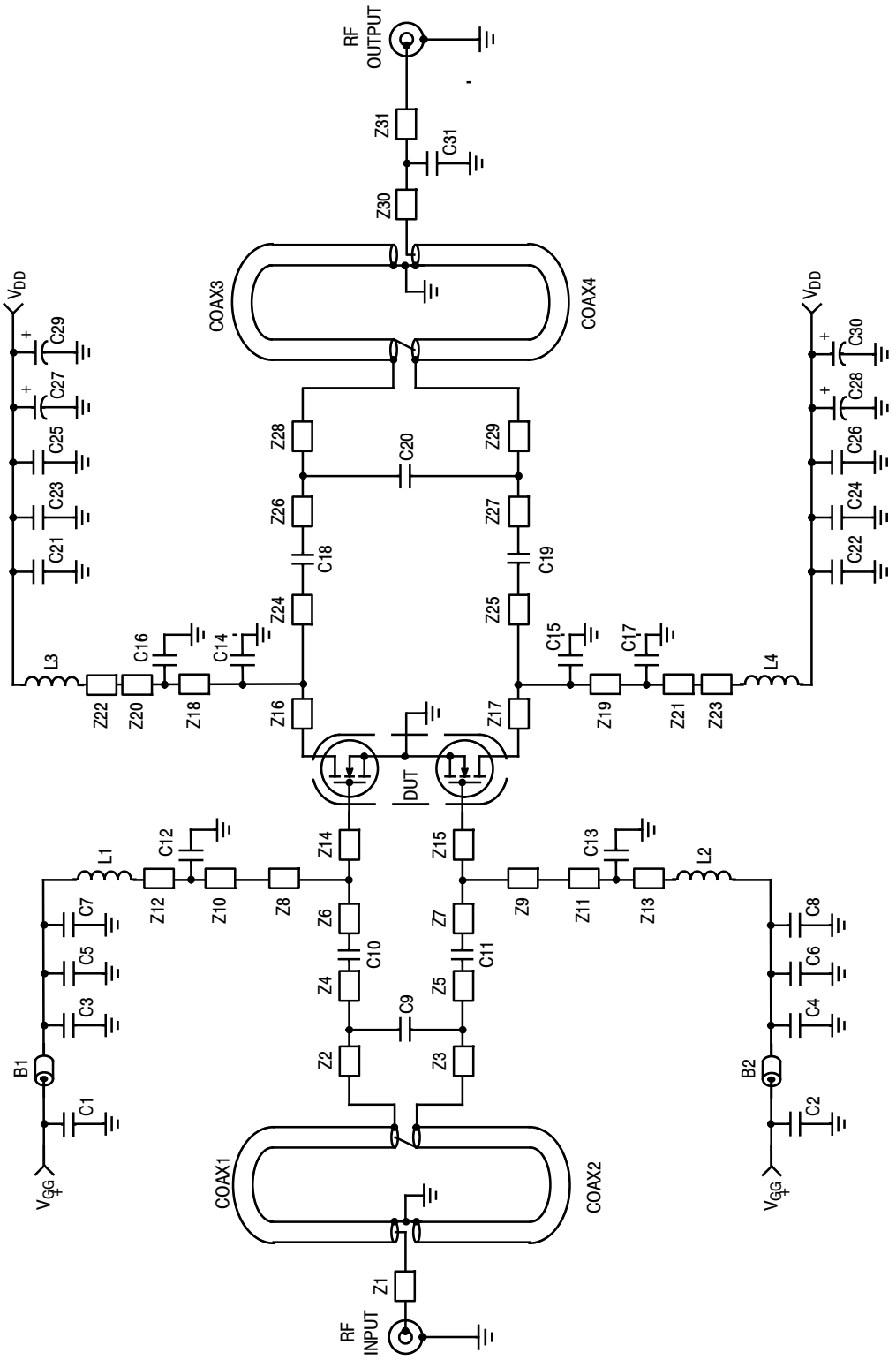



**Figure 6. MRFE6VP5150NR1 Narrowband Test Circuit Schematic — 230 MHz**

**Table 7. MRFE6VP5150NR1 Narrowband Test Circuit Microstrips — 230 MHz**

| Microstrip | Description | Microstrip | Description | Microstrip | Description |
|---|---|---|---|---|---|
| Z1 | 0.366″ × 0.082″ Microstrip | Z12, Z13 | 0.210″ × 0.068″ Microstrip | Z24, Z25 | 1.090″ × 0.230″ Microstrip |
| Z2, Z3 | 0.690″ × 0.120″ Microstrip | Z14, Z15 | 0.439″ × 0.746″ Microstrip | Z26, Z27 | 0.093″ × 0.230″ Microstrip |
| Z4, Z5 | 0.134″ × 0.120″ Microstrip | Z16, Z17 | 0.289″ × 0.393″ Microstrip | Z28, Z29 | 0.144″ × 0.230″ Microstrip |
| Z6, Z7 | 0.395″ × 0.120″ Microstrip | Z18, Z19 | 0.112″ × 0.289″ Microstrip | Z30 | 0.262″ × 0.082″ Microstrip |
| Z8*, Z9* | 0.125″ × 0.058″ Microstrip | Z20, Z21 | 0.422″ × 0.150″ Microstrip | Z31 | 0.102″ × 0.082″ Microstrip |
| Z10, Z11 | 0.450″ × 0.058″ Microstrip | Z22, Z23 | 0.400″ × 0.150″ Microstrip | | |

* Line length include microstrip bends

## TYPICAL CHARACTERISTICS — 230 MHz

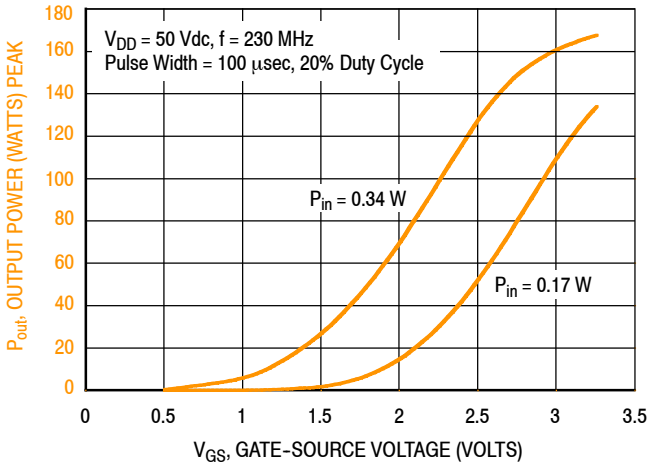
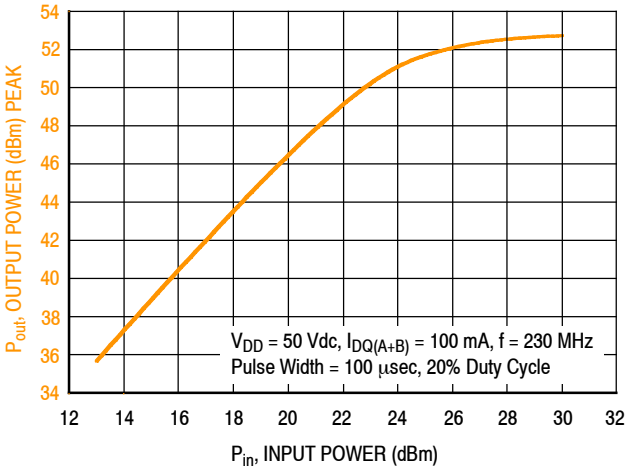



**Figure 7. Output Power versus Gate-Source Voltage at a Constant Input Power**




| f (MHz) | P1dB (W) | P3dB (W) |
|---|---|---|
| 230 | 159 | 182 |

**Figure 8. Output Power versus Input Power**

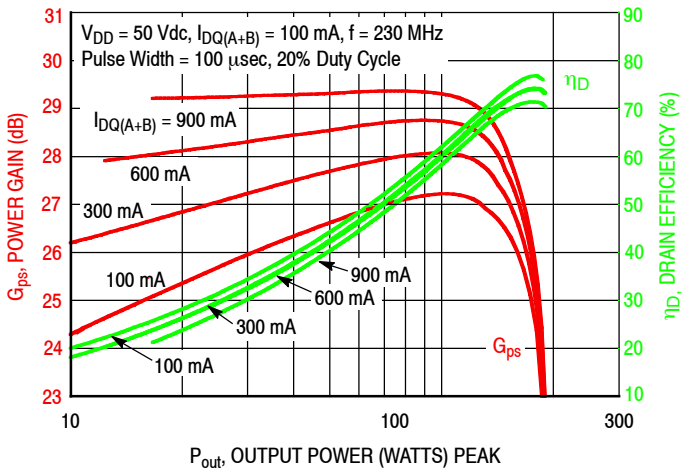



**Figure 9. Power Gain and Drain Efficiency versus Output Power and Quiescent Current**

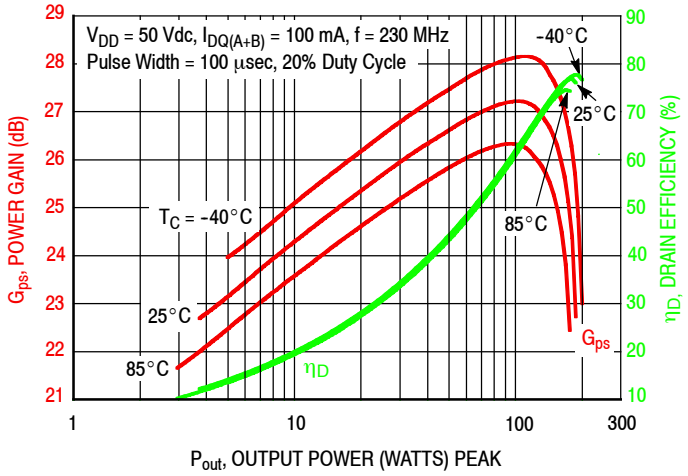



**Figure 10. Power Gain and Drain Efficiency versus Output Power**

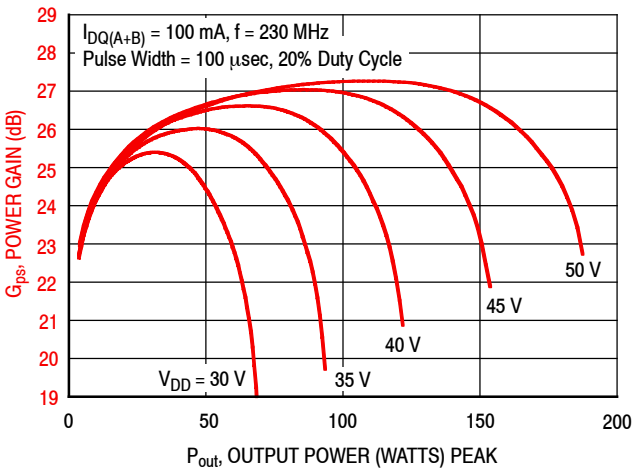



**Figure 11. Power Gain versus Output Power and Drain-Source Voltage**

$V_{DD}$ = 50 Vdc, $I_{DQ(A+B)}$ = 100 mA, $P_{out}$ = 150 W Peak

| f MHz | $Z_{source}$ Ω | $Z_{load}$ Ω |
|---|---|---|
| 230 | 6.2 + j17.7 | 12.1 + j12.5 |

$Z_{source}$ = Test circuit impedance as measured from gate to gate, balanced configuration.

$Z_{load}$ = Test circuit impedance as measured from drain to drain, balanced configuration.

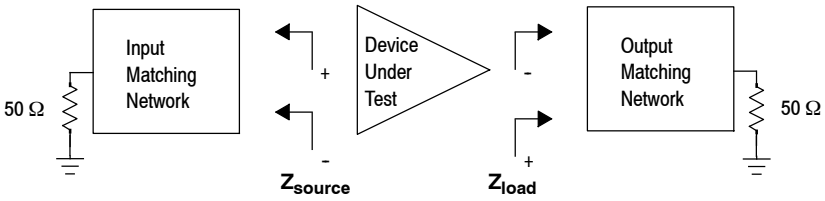



**Figure 12. Narrowband Series Equivalent Source and Load Impedance — 230 MHz**

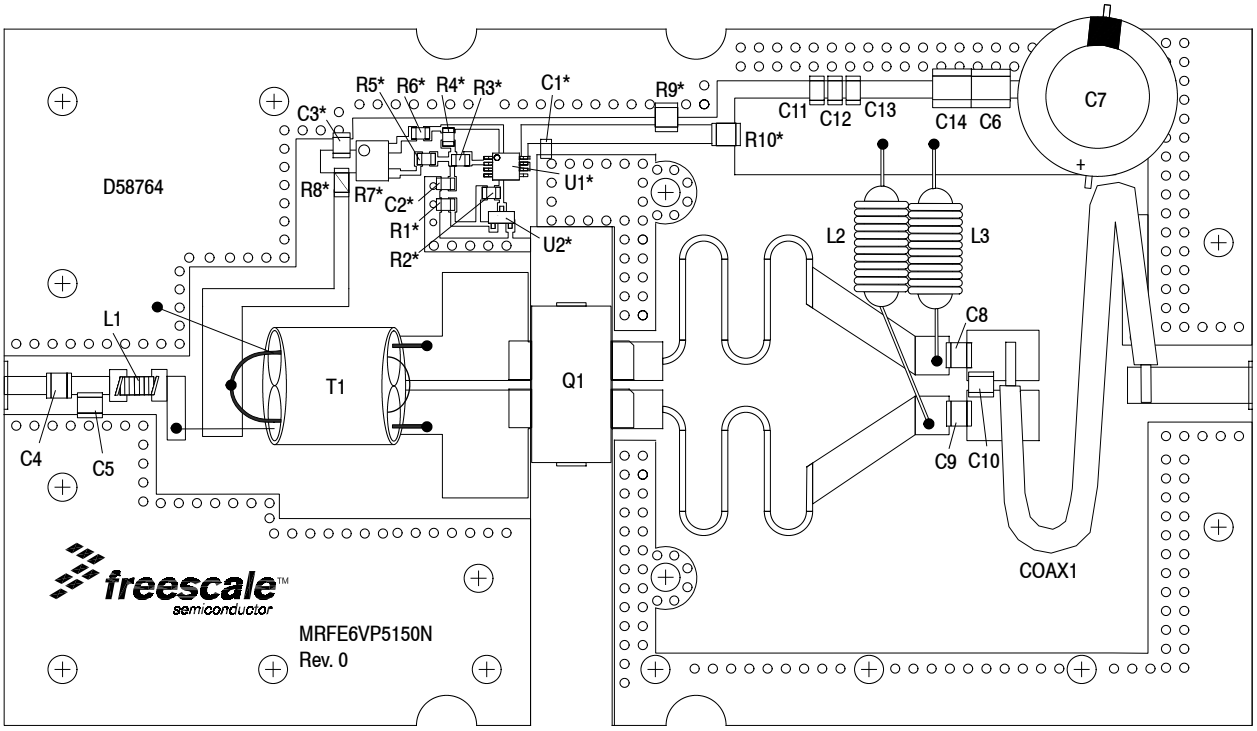
**Table 8. 87.5–108 MHz Broadband Performance** (In Freescale Reference Circuit, 50 ohm system)
$V_{DD}$ = 50 Vdc, $I_{DQ(A+B)}$ = 100 mA, $P_{in}$ = 1.5 W

| Signal Type | f (MHz) | $G_{ps}$ (dB) | $\eta_D$ (%) | $P_{out}$ (W) |
|---|---|---|---|---|
| CW | 87.5 | 22.7 | 74.6 | 187 |
| | 98 | 22.8 | 77.1 | 191 |
| | 108 | 22.5 | 77.8 | 179 |

**Table 9. Load Mismatch/Ruggedness** (In Freescale Reference Circuit, 50 ohm system) $I_{DQ(A+B)}$ = 100 mA

| Frequency (MHz) | Signal Type | VSWR | $P_{in}$ (W) | Test Voltage, $V_{DD}$ | Result |
|---|---|---|---|---|---|
| 98 | CW | > 65:1 at all Phase Angles | 3.0 (3 dB Overdrive) | 50 | No Device Degradation |

## 87.5–108 MHz BROADBAND REFERENCE CIRCUIT




*Bias Regulator and Temperature Compensation. Refer to AN1643, *RF LDMOS Power Modules for GSM Base Station Application: Optimum Biasing Circuit*. Go to http://www.freescale.com/rf. Select Documentation/Application Notes – AN1643.

**Figure 13. MRFE6VP5150NR1 Broadband Reference Circuit Component Layout — 87.5–108 MHz**

## 87.5–108 MHz BROADBAND REFERENCE CIRCUIT

**Table 10. MRFE6VP5150NR1 Broadband Reference Circuit Component Designations and Values — 87.5–108 MHz**

| Part | Description | Part Number | Manufacturer |
|---|---|---|---|
| C1, C2 | 1 μF Chip Capacitors | GRM21BR71H105KA12L | Murata |
| C3 | 10 nF Chip Capacitor | ATC200B103KT50XT | ATC |
| C4, C8, C9 | 1000 pF Chip Capacitors | ATC200B102KT50XT | ATC |
| C5 | 43 pF Chip Capacitor | ATC100B430JT500XT | ATC |
| C6, C14 | 10 μF Chip Capacitors | C5750X7S2A106M230KB | TDK |
| C7 | 470 μF, 63 V Electrolytic Capacitor | MCGPR63V477M13X26RH | Multicomp |
| C10 | 10 pF Chip Capacitor | ATC100B100JT500XT | ATC |
| C11 | 10 nF Chip Capacitor | GRM319R72A103KA01D | Murata |
| C12 | 47 nF Chip Capacitor | GRM31MR72A473KA01L | Murata |
| C13 | 470 nF Chip Capacitor | GRM31MR72A474KA35L | Murata |
| Coax1 | 35 Ω Flex Cable, 11.02″, 3 Turns | HSF-141C-35 | Hongsen Cable |
| L1 | 47 nH Inductor | 1812SMS47NJLC | Coilcraft |
| L2, L3 | Toroid Core, 10 Turns, 22 AWG Magnetic Wire | 11-750-K / 8077 | Ferronics/Beldon |
| Q1 | RF Power LDMOS Transistor | MRFE6VP5150NR1 | Freescale |
| R1 | 2.2 KΩ, 1/8 W Chip Resistor | CRCW08052K20FKEA | Vishay |
| R2 | 390 Ω, 1/8 W Chip Resistor | CRCW0805390RFKEA | Vishay |
| R3 | 10 Ω, 1/8 W Chip Resistor | RK73H2ATTD10R0F | KOA Speer |
| R4 | 1.0 KΩ, 1/8 W Chip Resistor | RR1220P-102-D | Susumu |
| R5 | 2.7 KΩ, 1/8 W Chip Resistor | CRCW08052K70FKEA | Vishay |
| R6 | 200 Ω, 1/8 W Chip Resistor | CRCW0805200RFKEA | Vishay |
| R7 | 5.0 KΩ Multi-turn Cermet Trimmer Potentiometer | 3224W-1-502E | Bourns |
| R8 | 10 Ω, 1/4 W Chip Resistor | CRCW120610R0FKEA | Vishay |
| R9, R10 | 5.1 KΩ, 1/2 W Chip Resistors | CRCW12105K10FKEA | Vishay |
| T1 | 61 Material Binocular Core Ferrite (1:1) with 24 AWG 1 Turn Primary, 24 AWG 1 Turn Secondary, Hand Wound | 2861000102 | Fair-Rite |
| U1 | Voltage Regulator 5 V, Micro8 | LP2951ACDMR2G | ON Semiconductor |
| U2 | NPN Bipolar Transistor | BC847ALT1G | ON Semiconductor |
| PCB | Rogers RO4350B, 0.030″, $\varepsilon_r$ = 3.66 | D58764 | MTL |

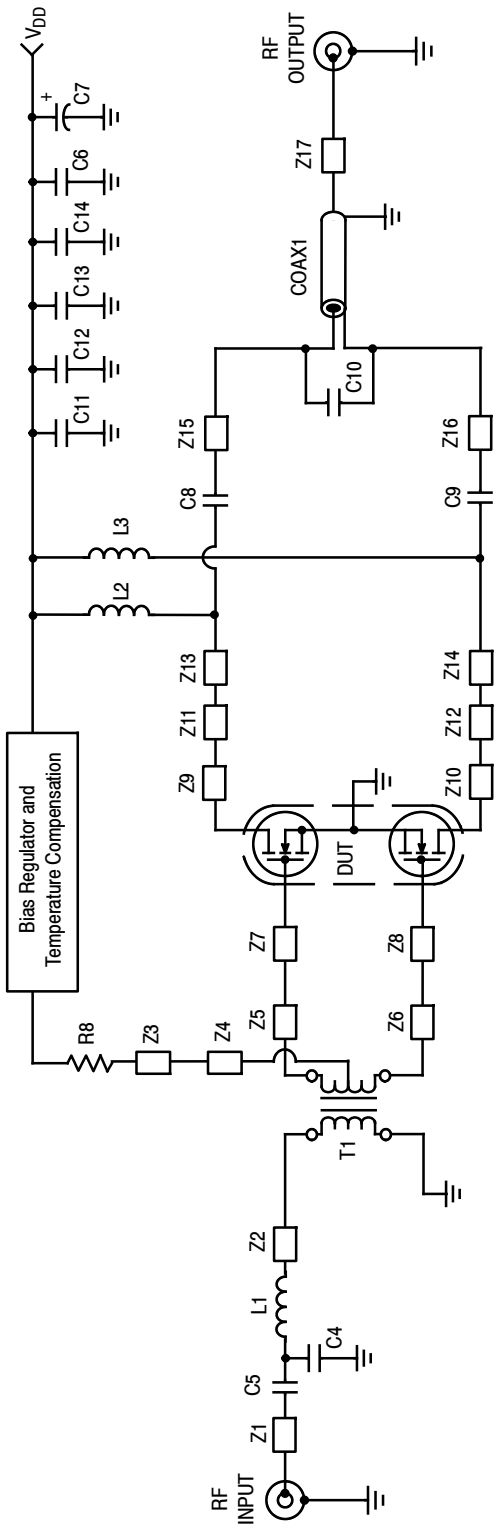



**Figure 14. MRFE6VP5150NR1 Broadband Reference Circuit Schematic — 87.5–108 MHz**

**Table 11. MRFE6VP51510NR1 Broadband Reference Circuit Microstrips — 87.5–108 MHz**

| Microstrip | Description |
|---|---|
| Z1 | 0.230″ × 0.080″ Microstrip |
| Z2* | 0.280″ × 0.080″ Microstrip |
| Z3* | 0.680″ × 0.080″ Microstrip |
| Z4 | 0.310″ × 0.170″ Microstrip |
| Z5, Z6 | 0.270″ × 0.200″ Microstrip |
| Z7, Z8 | 0.380″ × 0.630″ Microstrip |
| Z9, Z10 | 0.240″ × 0.180″ Microstrip |
| Z11*, Z12* | 2.060″ × 0.027″ Microstrip |
| Z13*, Z14* | 0.680″ × 0.150″ Microstrip |
| Z15, Z16 | 0.240″ × 0.210″ Microstrip |
| Z17 | 0.480″ × 0.150″ Microstrip |

* Line length includes microstrip bends

## TYPICAL CHARACTERISTICS — 87.5–108 MHz BROADBAND REFERENCE CIRCUIT

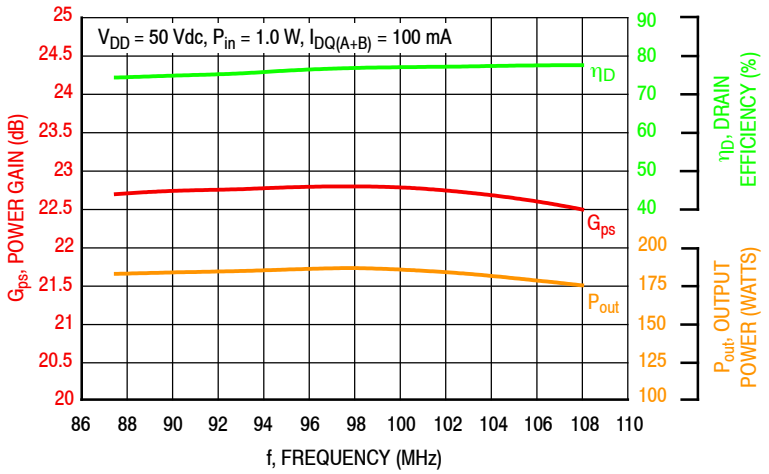



**Figure 15. Power Gain, Drain Efficiency and CW Output Power versus Frequency at a Constant Input Power**

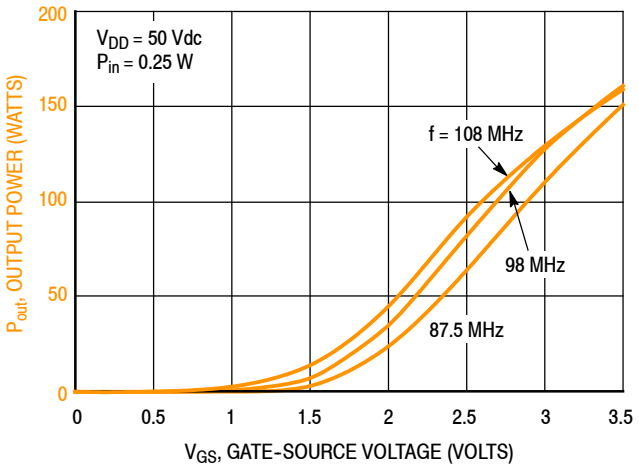



**Figure 16. CW Output Power versus Gate-Source Voltage at a Constant Input Power**

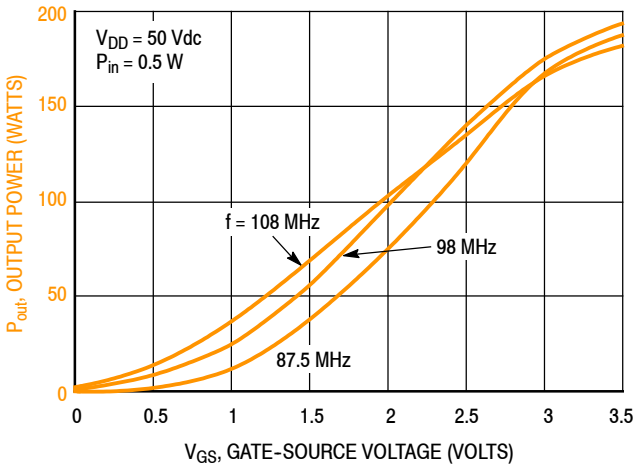
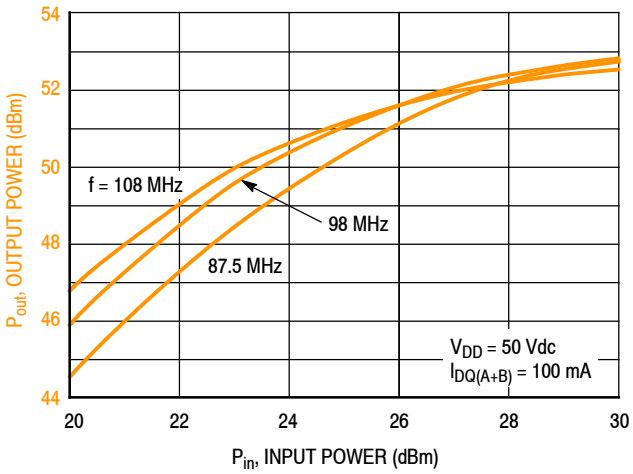



**Figure 17. CW Output Power versus Gate-Source Voltage at a Constant Input Power**

## TYPICAL CHARACTERISTICS — 87.5–108 MHz BROADBAND REFERENCE CIRCUIT




| f (MHz) | P1dB (W) | P3dB (W) |
|---|---|---|
| 87.5 | 164 | 189 |
| 98 | 145 | 183 |
| 108 | 130 | 165 |

**Figure 18. CW Output Power versus Input Power**

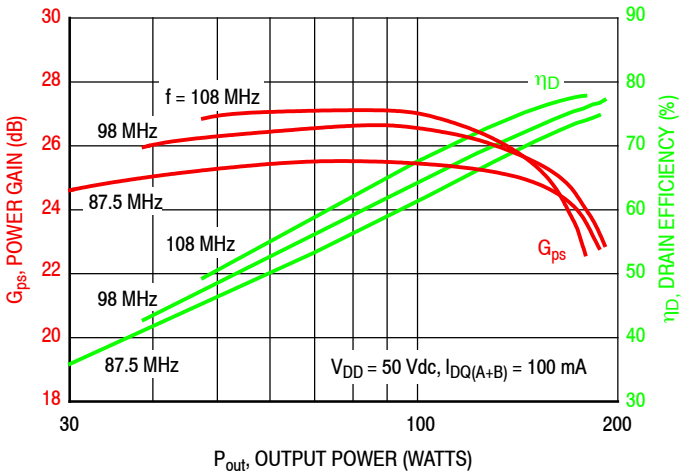
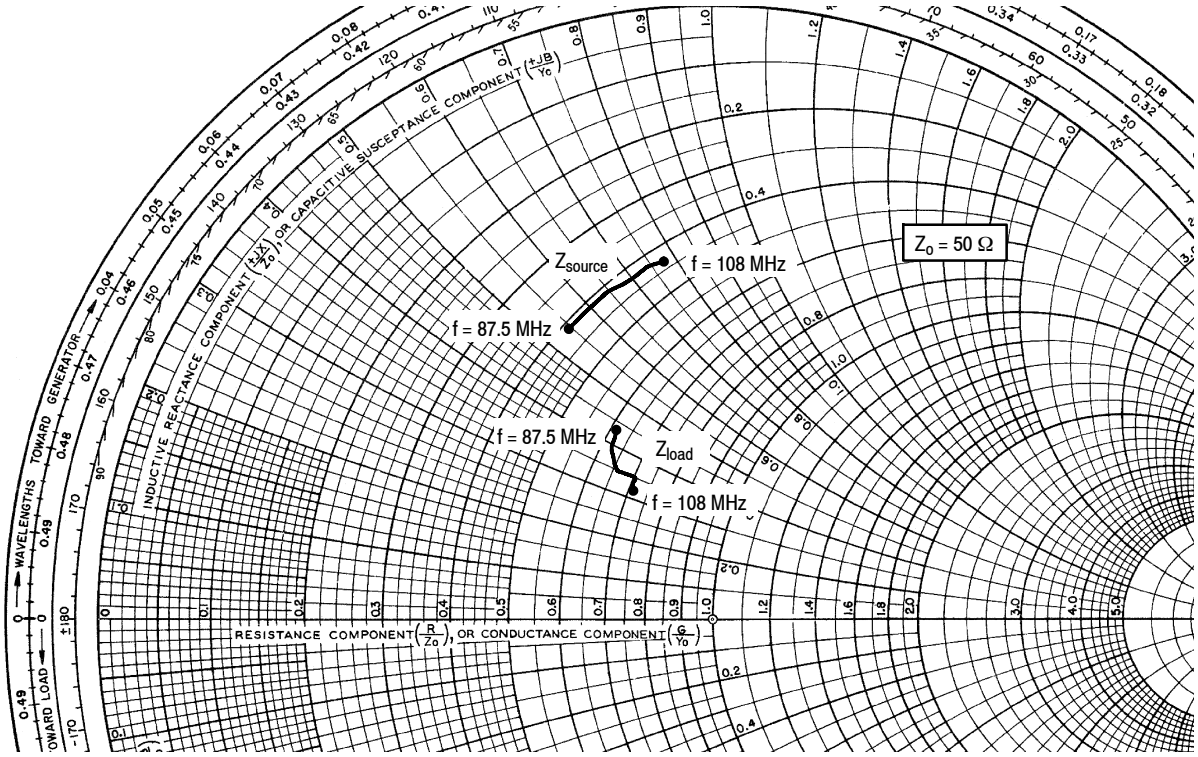



**Figure 19. Power Gain and Drain Efficiency versus CW Output Power**

## 87.5–108 MHz BROADBAND REFERENCE CIRCUIT




$V_{DD}$ = 50 Vdc, $I_{DQ(A+B)}$ = 100 mA, $P_{out}$ = 150 W CW

| f MHz | $Z_{source}$ Ω | $Z_{load}$ Ω |
|---|---|---|
| 87.5 | 20.3 + j26.9 | 35.3 + j15.9 |
| 92 | 20.4 + j29.6 | 35.2 + j17.1 |
| 96 | 20.6 + j31.9 | 35.1 + j17.3 |
| 100 | 20.8 + j34.1 | 33.2 + j17.4 |
| 104 | 21.0 + j36.5 | 31.7 + j19.5 |
| 108 | 21.4 + j38.6 | 30.6 + j21.4 |

$Z_{source}$ = Test circuit impedance as measured from gate to gate, balanced configuration.

$Z_{load}$ = Test circuit impedance as measured from drain to drain, balanced configuration.

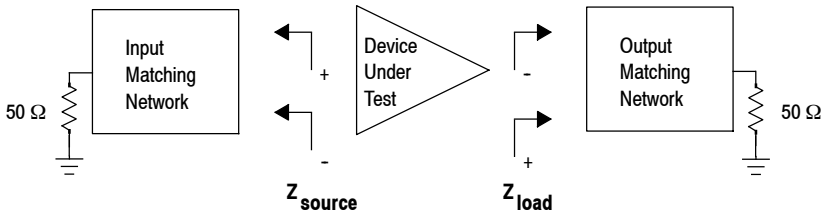
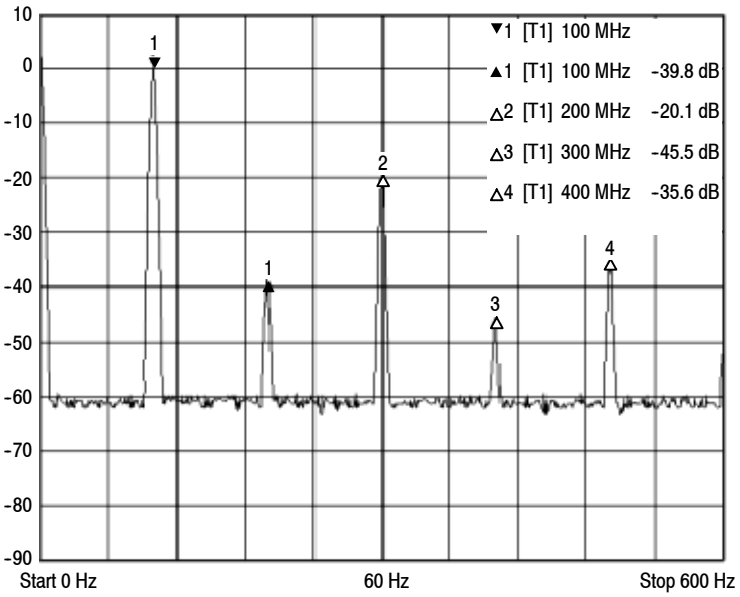



**Figure 20. Broadband Series Equivalent Source and Load Impedance — 87.5–108 MHz**

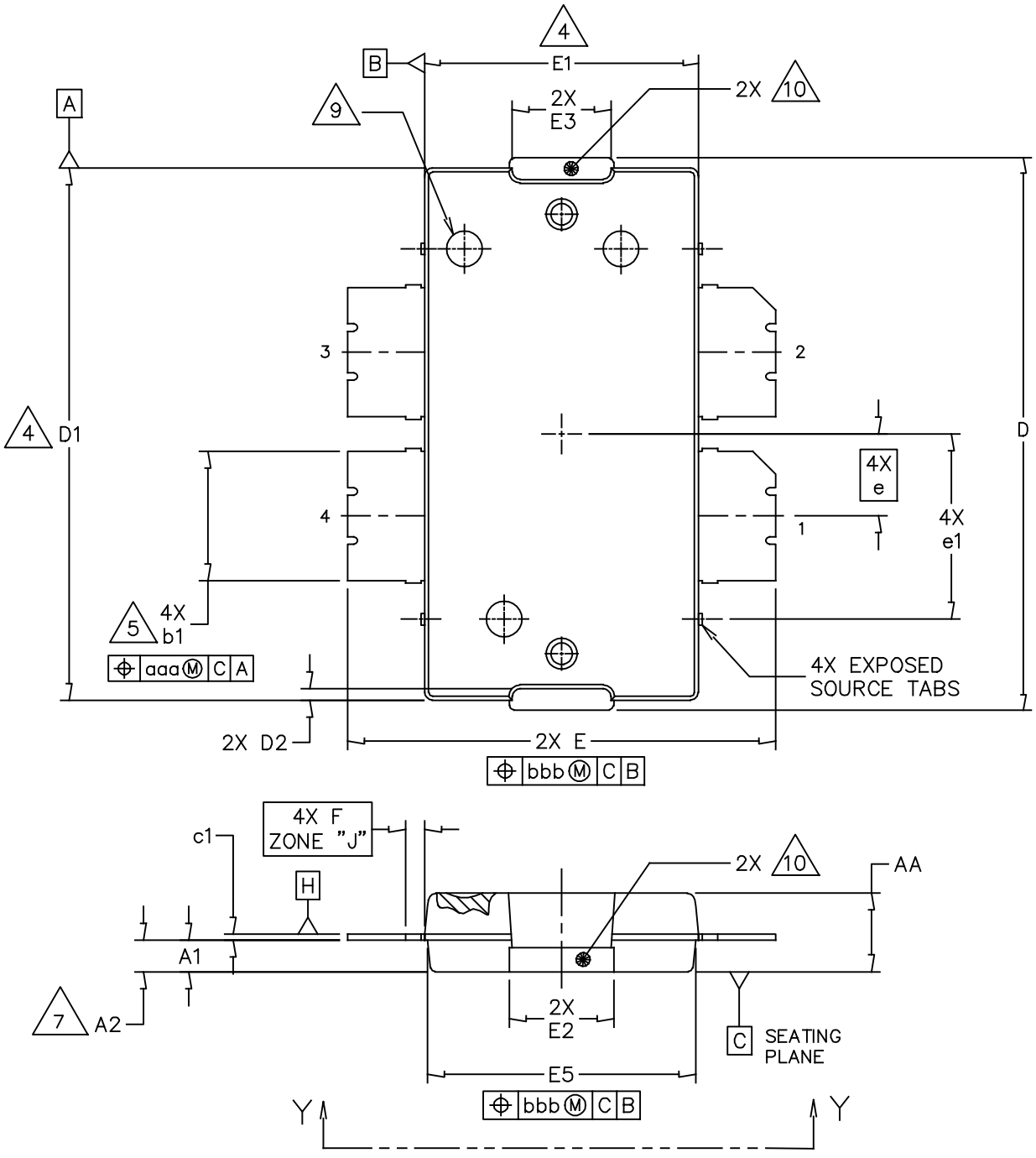
## HARMONIC MEASUREMENTS — 87.5–108 MHz
## BROADBAND REFERENCE CIRCUIT



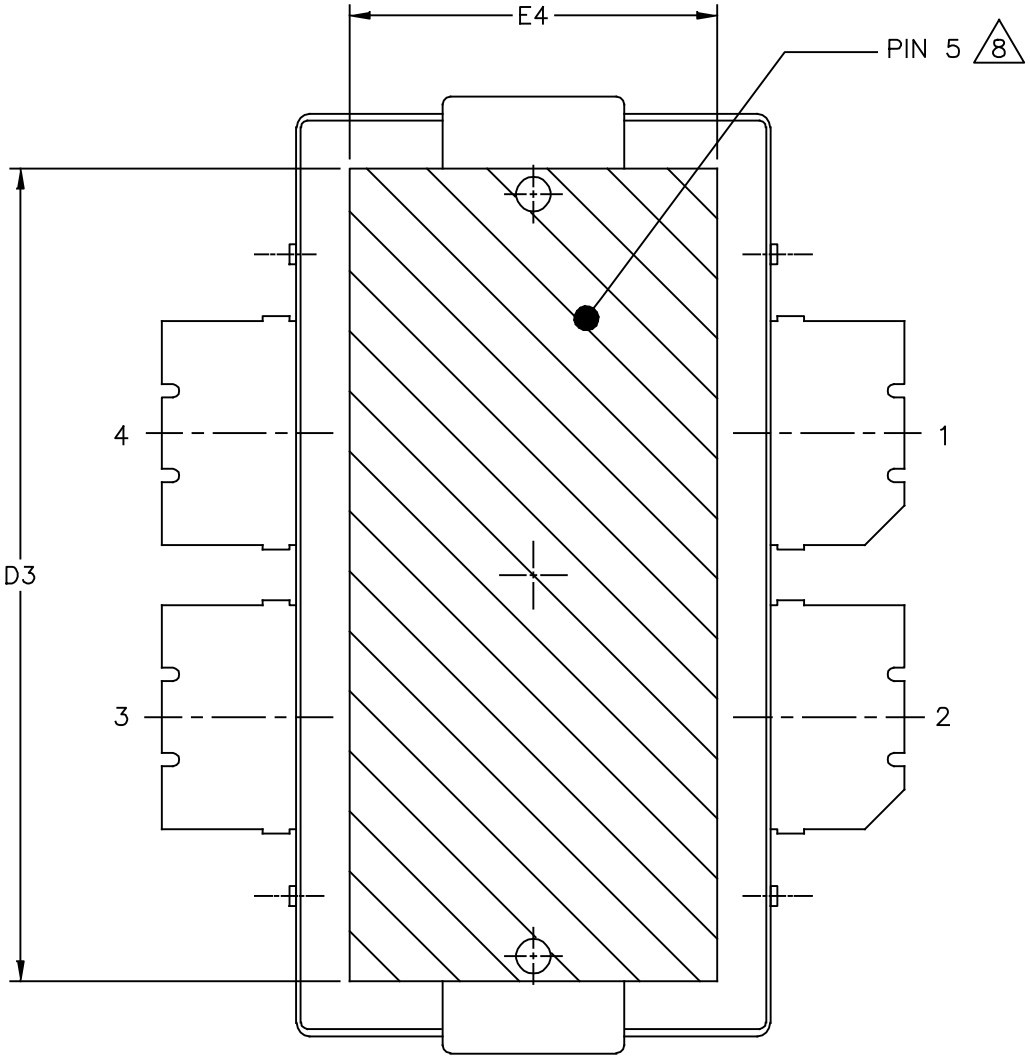

| H2 (200 MHz) | H3 (300 MHz) | H4 (400 MHz) | H5 (500 MHz) |
|---|---|---|---|
| -39.8 dB | -20.1 dB | -45.5 dB | -35.6 dB |

**Figure 21. 100 MHz Harmonics @ 150 W**

## PACKAGE DIMENSIONS




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| | STANDARD: NON–JEDEC | |
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NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15MM) PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

5. DIMENSIONS b1 DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13MM) TOTAL IN EXCESS OF THE b1 DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

7. DIMENSION A2 APPLIES WITHIN ZONE J ONLY.

8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG. DIMENSIONS D3 AND D4 REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF HEAT SLUG.

9. DIMPLED HOLE REPRESENTS INPUT SIDE.

10. THESE SURFACES OF THE HEAT SLUG ARE NOT PART OF THE SOLDERABLE SURFACES AND MAY REMAIN UNPLATED.

| DIM | INCH MIN | INCH MAX | MILLIMETER MIN | MILLIMETER MAX | DIM | INCH MIN | INCH MAX | MILLIMETER MIN | MILLIMETER MAX |
|---|---|---|---|---|---|---|---|---|---|
| AA | .100 | .104 | 2.54 | 2.64 | F | .025 BSC | | 0.64 BSC | |
| A1 | .039 | .043 | 0.99 | 1.09 | b1 | .164 | .170 | 4.17 | 4.32 |
| A2 | .040 | .042 | 1.02 | 1.07 | c1 | .007 | .011 | 0.18 | 0.28 |
| D | .712 | .720 | 18.08 | 18.29 | e | .106 BSC | | 2.69 BSC | |
| D1 | .688 | .692 | 17.48 | 17.58 | e1 | .239 INFO ONLY | | 6.07 INFO ONLY | |
| D2 | .011 | .019 | 0.28 | 0.48 | aaa | .004 | | 0.10 | |
| D3 | .600 | --- | 15.24 | --- | bbb | .008 | | 0.20 | |
| E | .551 | .559 | 14.00 | 14.20 | | | | | |
| E1 | .353 | .357 | 8.97 | 9.07 | | | | | |
| E2 | .132 | .140 | 3.35 | 3.56 | | | | | |
| E3 | .124 | .132 | 3.15 | 3.35 | | | | | |
| E4 | .270 | --- | 6.86 | --- | | | | | |
| E5 | .346 | .350 | 8.79 | 8.89 | | | | | |

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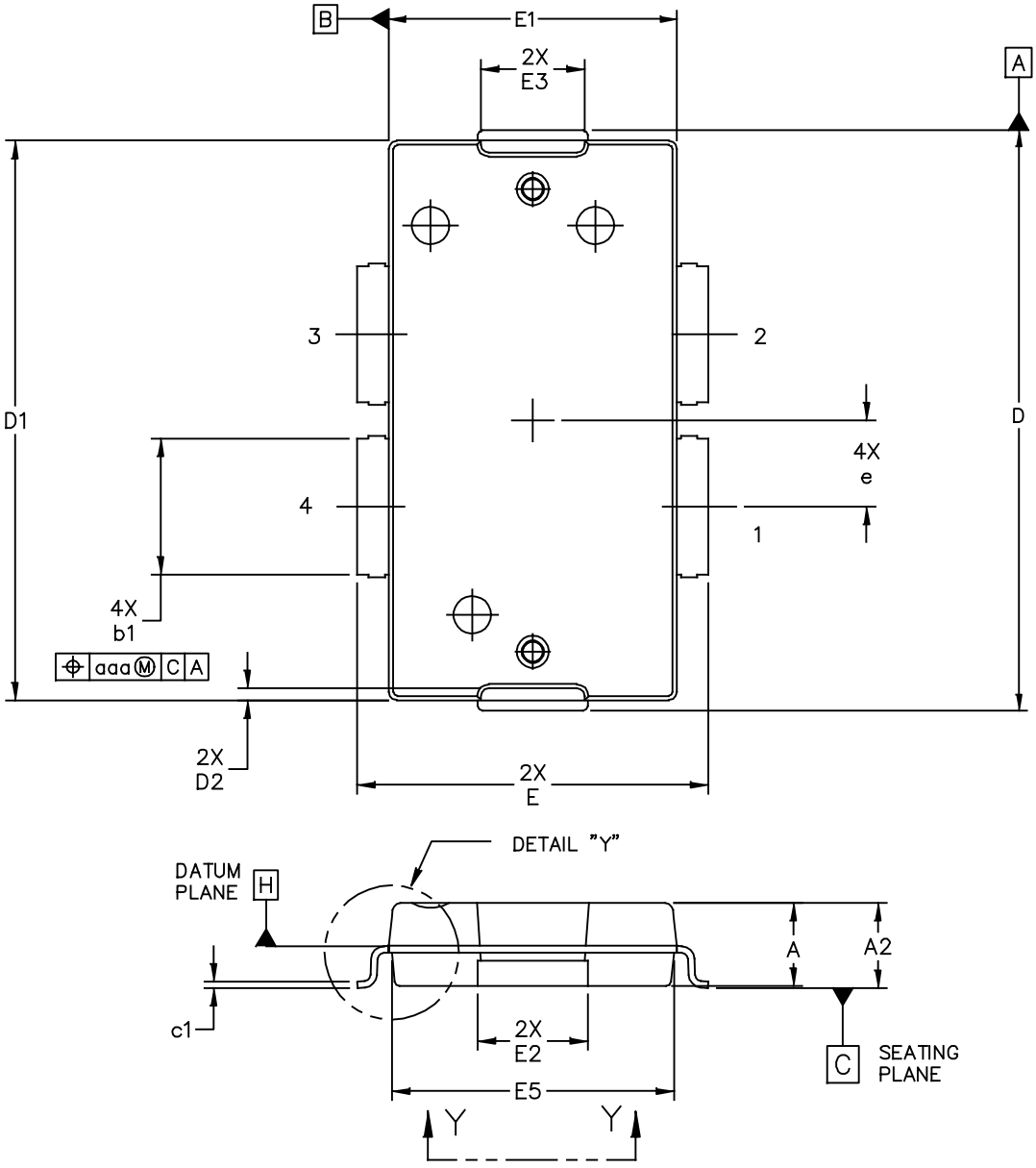
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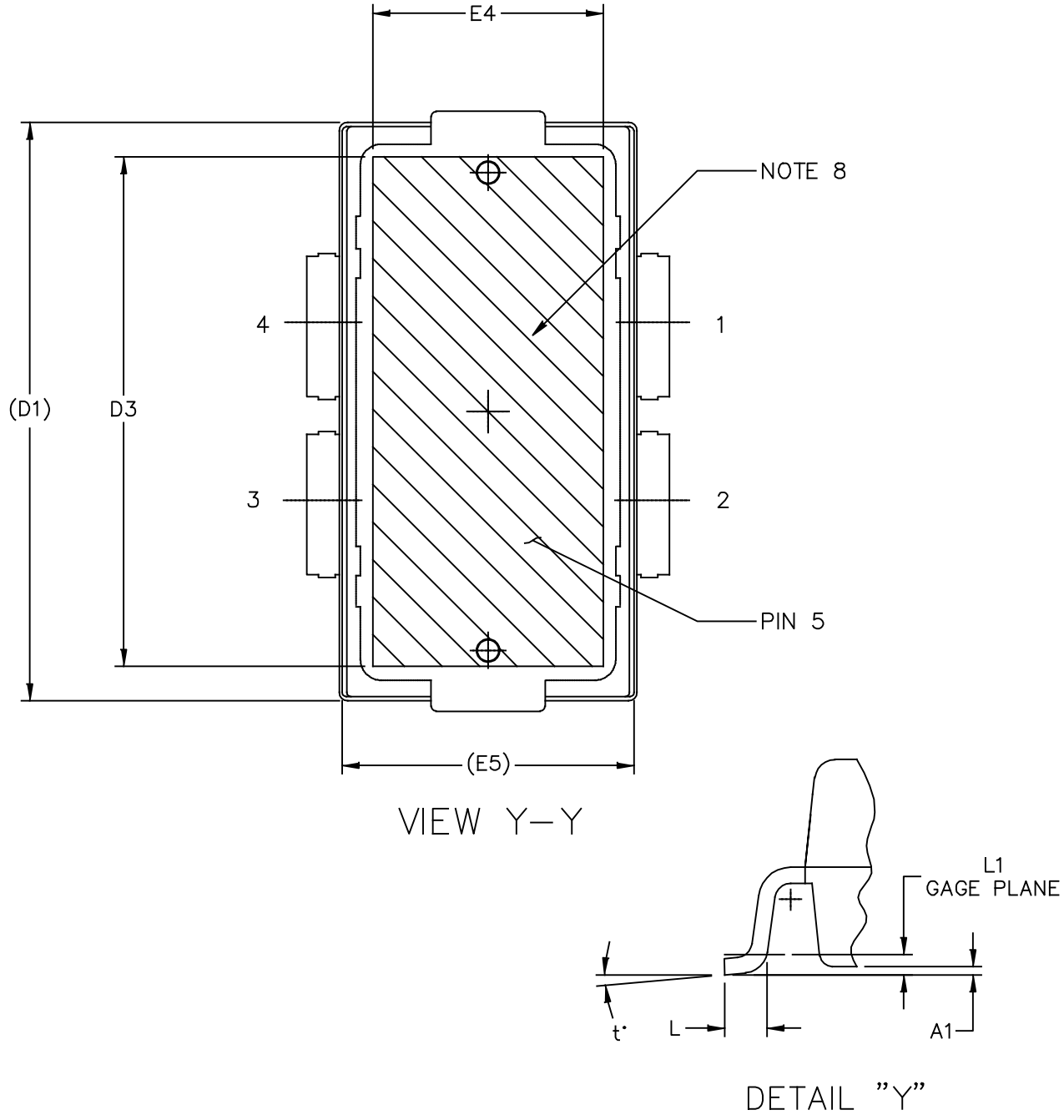
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| | CASE NUMBER: 1487-05 | 03 AUG 2007 |
| | STANDARD: JEDEC TO-270 BB | |




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| | CASE NUMBER: 1487–05 | 03 AUG 2007 |
| | STANDARD: JEDEC TO–270 BB | |

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE –H– IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.

5. DIMENSION "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

STYLE 1:
PIN 1 – DRAIN
PIN 2 – DRAIN
PIN 3 – GATE
PIN 4 – GATE
PIN 5 – SOURCE

| DIM | INCH MIN | INCH MAX | MILLIMETER MIN | MILLIMETER MAX | DIM | INCH MIN | INCH MAX | MILLIMETER MIN | MILLIMETER MAX |
|---|---|---|---|---|---|---|---|---|---|
| A | .100 | .104 | 2.54 | 2.64 | L | .018 | .024 | 0.46 | 0.61 |
| A1 | .001 | .004 | 0.02 | 0.10 | L1 | .01 BSC | | 0.25 BSC | |
| A2 | .101 | .108 | 2.56 | 2.74 | b1 | .164 | .170 | 4.17 | 4.32 |
| D | .712 | .720 | 18.08 | 18.29 | c1 | .007 | .011 | .18 | .28 |
| D1 | .688 | .692 | 17.48 | 17.58 | e | .106 BSC | | 2.69 BSC | |
| D2 | .011 | .019 | 0.28 | 0.48 | t | 2° | 8° | 2° | 8° |
| D3 | .600 | ---- | 15.24 | ---- | aaa | .004 | | 0.1 | |
| E | .429 | .437 | 10.90 | 11.10 | | | | | |
| E1 | .353 | .357 | 8.97 | 9.07 | | | | | |
| E2 | .132 | .140 | 3.35 | 3.56 | | | | | |
| E3 | .124 | .132 | 3.15 | 3.35 | | | | | |
| E4 | .270 | ---- | 6.86 | ---- | | | | | |
| E5 | .346 | .350 | 8.79 | 8.89 | | | | | |

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|---|---|---|
| TO–270<br>4 LEAD, WIDE BODY<br>GULL WING | CASE NUMBER: 1487–05 | 03 AUG 2007 |
| | STANDARD: JEDEC TO–270 BB | |

## PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

**Application Notes**

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN1643: RF LDMOS Power Modules for GSM Base Station Application: Optimum Biasing Circuit

**Engineering Bulletins**

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

**Software**

- Electromigration MTTF Calculator
- RF High Power Model

**Development Tools**

- Printed Circuit Boards

For Software and Tools, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

## REVISION HISTORY

The following table summarizes revisions to this document.

| Revision | Date | Description |
|---|---|---|
| 0 | May 2014 | • Initial Release of Data Sheet |
| 1 | July 2014 | • Table 10, Broadband Reference Circuit Component Designations and Values — 87.5–108 MHz: updated R2, R9 and R10 resistors, p. 12 |

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