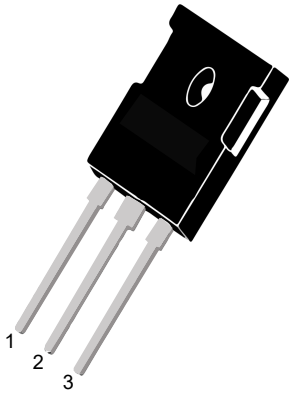
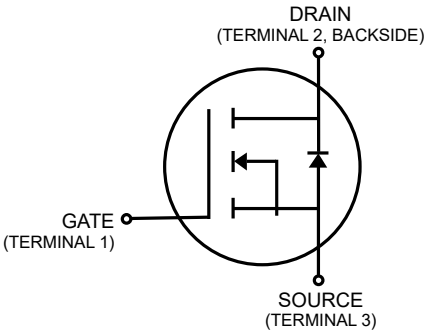
700V, 90 mΩ N-Channel mSiC™ MOSFET

MSC090SMA070B

Product Overview

700V, 90 mΩ typical at V_{GS} = 20V, 102 mΩ typical at V_{GS} = 18V, Silicon Carbide (SiC) N-Channel MOSFET, TO-247.





Features

- AEC-Q101 qualified option available
- Low capacitances and low gate charge
- Fast switching speed due to low internal gate resistance (ESR)
- Stable operation at high junction temperature, $T_{J(max)}$ = 175 °C
- Fast and reliable body diode
- Superior avalanche ruggedness
- RoHS compliant

Benefits

- High efficiency to enable lighter and more compact system
- Simple to drive and easy to parallel
- Improved thermal capabilities and lower switching losses
- Eliminates the need for external freewheeling diode
- Lower system cost of ownership

Applications

- Photovoltaic (PV) inverter, converter, and industrial motor drives
- Smart grid transmission and distribution
- Induction heating and welding
- Hybrid Electric Vehicle (HEV) powertrain and Electric Vehicle (EV) charger
- Power supply and distribution

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1. Device Specifications

This section shows the specifications of this device.

1.1 Absolute Maximum Ratings

The following table shows the absolute maximum ratings of this device.

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain source voltage	700	V
I_D	Continuous drain current at T_C = 25 °C	34	A
	Continuous drain current at T_C = 100 °C	24	
I_{DM}	Pulsed drain current[1]	126	
V_{GS}	Gate-source voltage	23 to –10	V
	Transient gate-source voltage	25 to –12	
P_D	Total power dissipation at T_C = 25 °C	153	W
	Linear derating factor	1.0	W/°C

Note:

1. Repetitive rating: pulse width and case temperature are limited by the maximum junction temperature.

The following table shows the thermal and mechanical characteristics of this device.

Table 1-2. Thermal and Mechanical Characteristics

Symbol	Characteristic/Test Conditions	Min.	Typ.	Max.	Unit
$R_{\theta JC}$	Junction-to-case thermal resistance	—	0.75	0.98	°C/W
T_J	Operating junction temperature	–55	—	175	°C
T_{STG}	Storage temperature	–55	—	175	
T_L	Lead temperature for 10 seconds	—	—	300	°C
τ_M	Mounting torque, M3 screw for heat sink attachment (requires 1, not included)	—	0.8	—	N·m
Wt	Package weight	—	6.2	—	g

ESD practices should comply with JESD-625.

1.2 Electrical Performance

The following table shows the static characteristics of this device. T_J = 25 °C unless otherwise specified.

Table 1-3. Static Characteristics

Symbol	Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0V, I_D = 100 µA	700	—	—	V
$R_{DS(on)}$	Drain-source on resistance[1]	V_{GS} = 20V, I_D = 15A	—	90	112	mΩ
		V_{GS} = 18V, I_D = 15A	—	102	—	
$V_{GS(th)}$	Gate-source threshold voltage	V_{GS} = V_{DS}, I_D = 0.75 mA	1.9	3.0	5.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 700V, V_{GS} = 0V	—	0.1	25	µA
		V_{DS} = 700V, V_{GS} = 0V, T_J = 175 °C	—	1.5	—	
I_{GSS}	Gate-source leakage current	V_{GS} = 20V/–10V	—	—	±100	nA

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Note:

1. Pulse test: pulse width < 380 µs, duty cycle < 2%.

The following table shows the dynamic characteristics of this device. T_J = 25 °C unless otherwise specified. The dynamic characteristics are characterized, not 100% tested, at the recommended operating V_{GS} = 20V/–5V.

Table 1-4. Dynamic Characteristics

Symbol	Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{GS} = 0V V_{DD} = 700V V_{AC} = 25 mV ƒ = 200 kHz	—	806	—	pF
C_{rss}	Reverse transfer capacitance		—	9.0	—	
C_{oss}	Output capacitance		—	106	—	
Q_G	Total gate charge	V_{GS} = –5V/20V V_{DD} = 470V I_D = 15A	—	41	—	nC
Q_{GS}	Gate-source charge		—	9.0	—	
Q_{GD}	Gate-drain charge		—	10	—	
$t_{d(on)}$	Turn-on delay time	V_{DD} = 470V V_{GS} = –5V/20V I_D = 14A $R_{G(ext)}$ = 8Ω Freewheeling diode = MSC090SMA070B (V_{GS} = –5V); reference Figure 1-19	—	10	—	ns
t_r	Voltage rise time		—	9.0	—	
$t_{d(off)}$	Turn-off delay time		—	18	—	
t_f	Voltage fall time		—	18	—	
E_{on}	Turn-on switching energy		—	88	—	µJ
E_{off}	Turn-off switching energy		—	27	—	
ESR	Gate equivalent series resistance	f = 1 MHz, 25 mV, drain short	—	2.4	—	Ω
SCWT	Short circuit withstand time	V_{DS} = 560V, V_{GS} = 20V	—	3.0	—	µs
E_{AS}	Avalanche energy, single pulse	I_D = 15A	—	1100	—	mJ

The following table shows the body diode characteristics of this device. T_J = 25 °C unless otherwise specified. The body diode reverse recovery is characterized, not 100% tested.

Table 1-5. Body Diode Characteristics

Symbol	Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
V_{SD}	Diode forward voltage	I_{SD} = 15A, V_{GS} = 0V	—	3.7	—	V
		I_{SD} = 15A, V_{GS} = –5V	—	3.9	5.0	
t_{rr}	Reverse recovery time	I_{SD} = 14A, V_{GS} = –5V, Drive R_G = 8Ω, V_{DD} = 470V, dI/dt = –2700 A/µs	—	21	—	ns
Q_{rr}	Reverse recovery charge		—	107	—	nC
I_{RRM}	Reverse recovery current		—	8.0	—	A

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1.3 Typical Performance Curves

Data for performance curves are characterized, not 100% tested.

Figure 1-1. Drain Current vs. V_{DS} at T_J

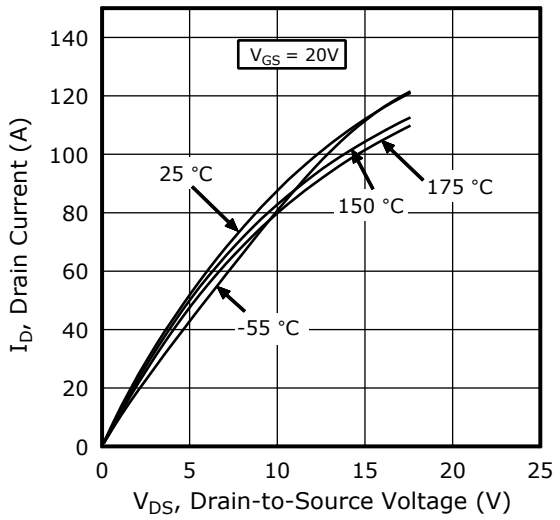


Figure 1-2. Drain Current vs. V_{DS} at V_{GS}

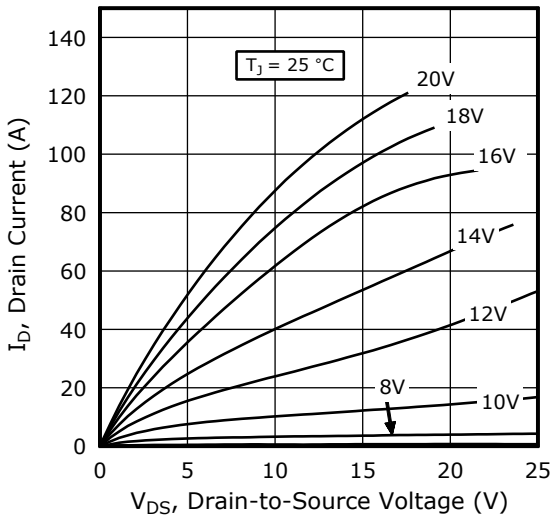


Figure 1-3. Drain Current vs. V_{DS} at V_{GS}

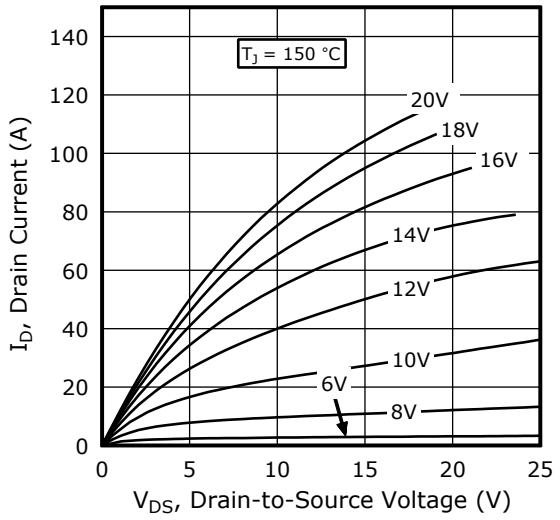
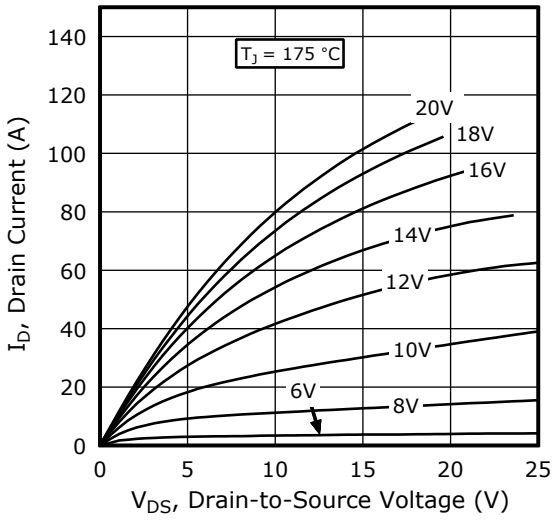


Figure 1-4. Drain Current vs. V_{DS} at V_{GS}



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Figure 1-5. $R_{DS(on)}$ vs. Junction Temperature

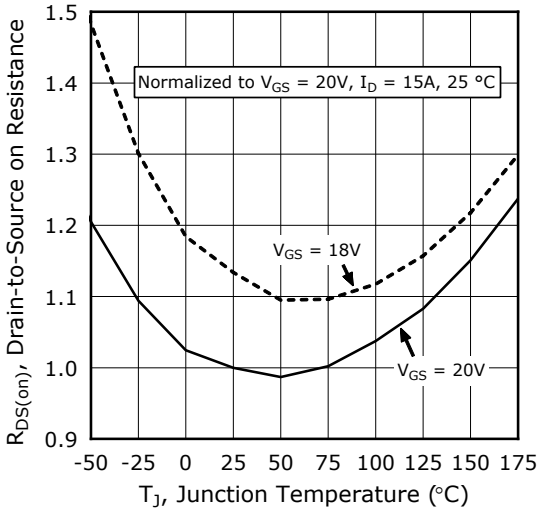


Figure 1-6. Gate Charge Characteristics

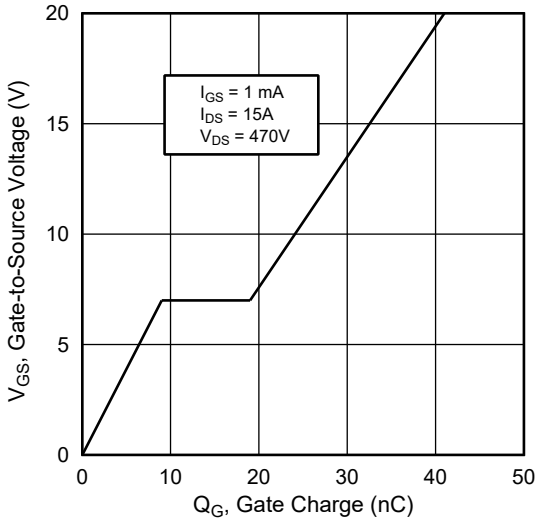


Figure 1-7. Capacitance vs. Drain-to-Source Voltage

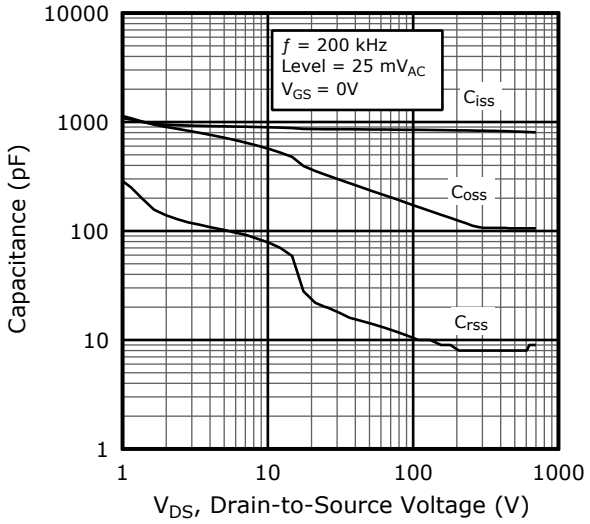
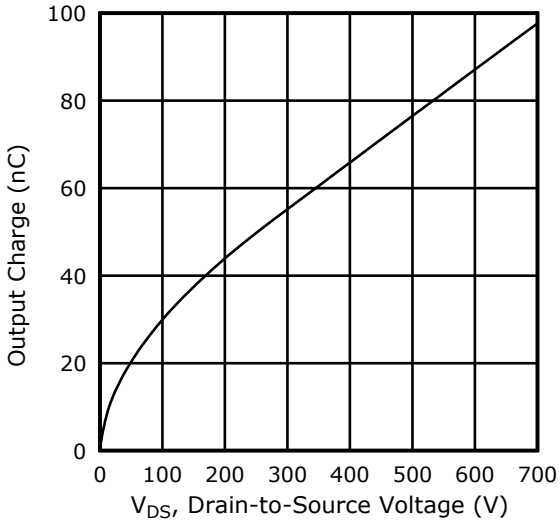


Figure 1-8. Output Charge vs. Drain-to-Source Voltage



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Figure 1-9. Output Stored Energy vs. V_{DS}

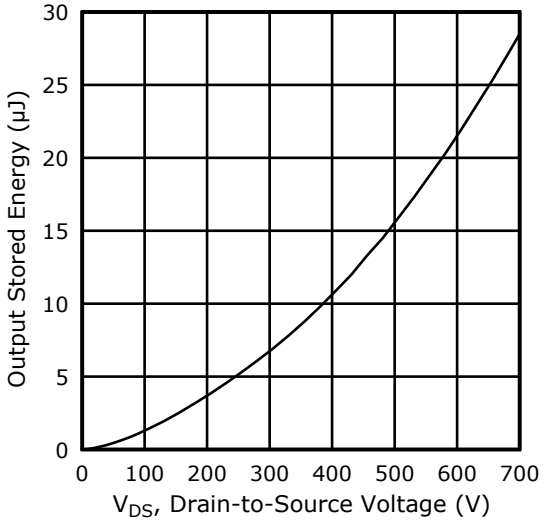


Figure 1-10. I_D vs. V_{DS} 3rd Quadrant Conduction

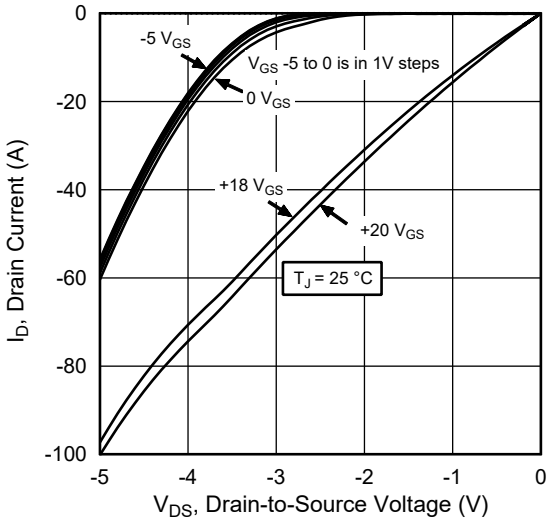


Figure 1-11. I_D vs. V_{DS} 3rd Quadrant Conduction

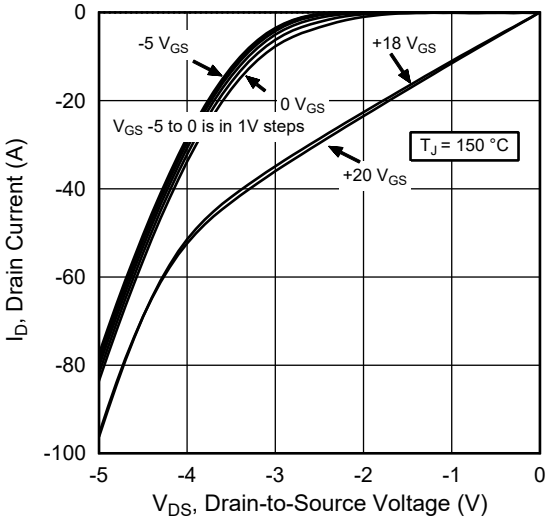
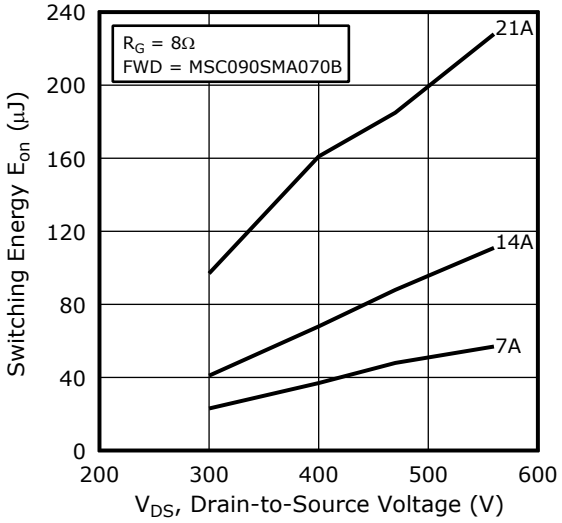


Figure 1-12. Switching Energy E_{on} vs. V_{DS} & I_D



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Figure 1-13. Switching Energy E_{off} vs. V_{DS} & I_D

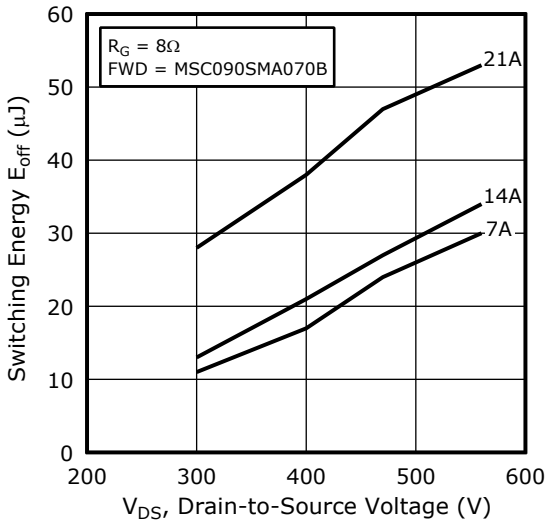


Figure 1-14. Switching Energy vs. R_G

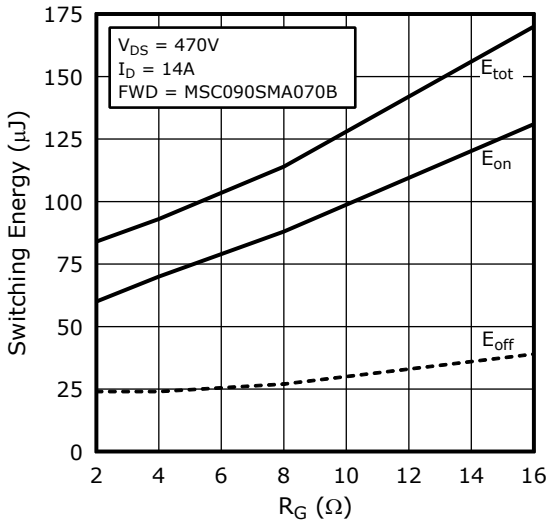


Figure 1-15. Switching Energy vs. Junction Temperature

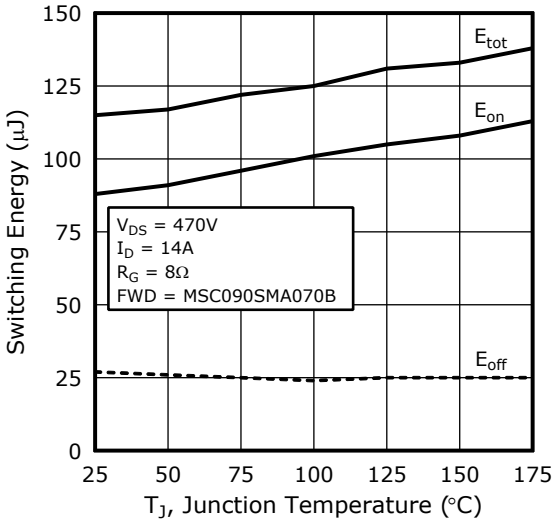
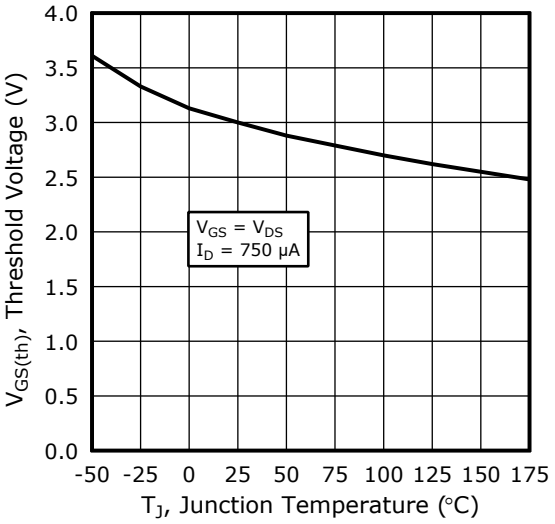


Figure 1-16. Threshold Voltage vs. Junction Temperature



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Figure 1-17. Forward Safe Operating Area

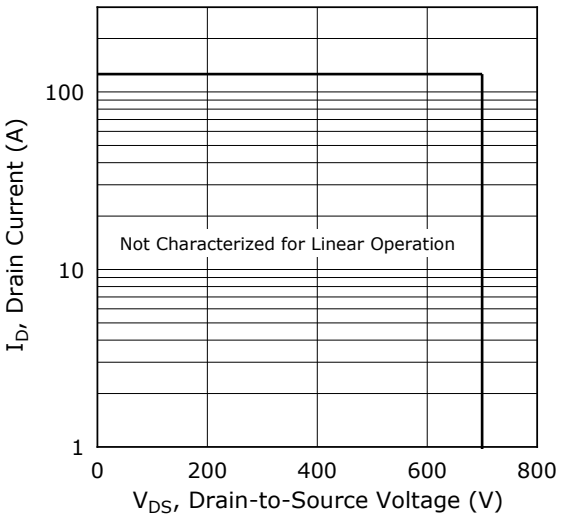
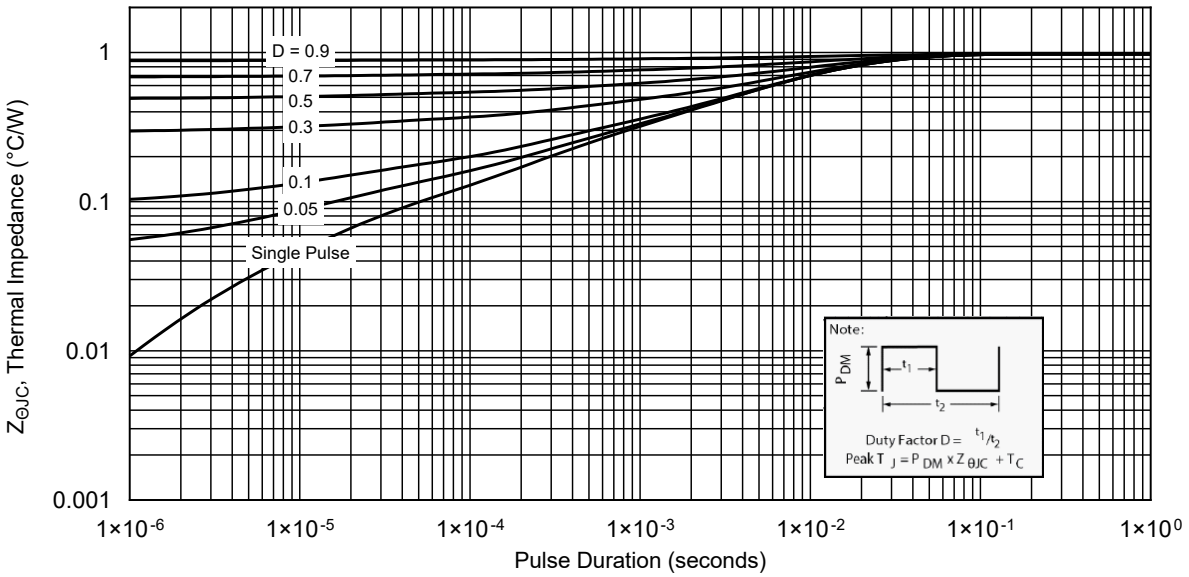
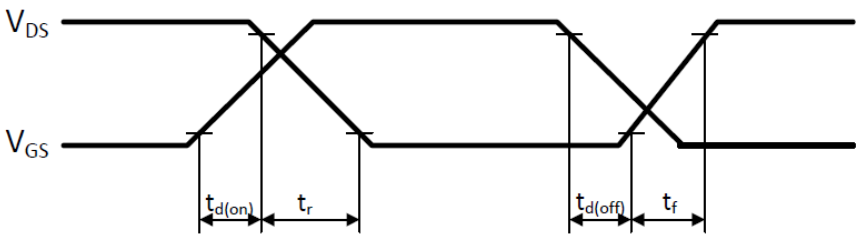


Figure 1-18. Maximum Transient Thermal Impedance



The following figure shows the switching waveform diagram of this device.

Figure 1-19. Switching Waveform



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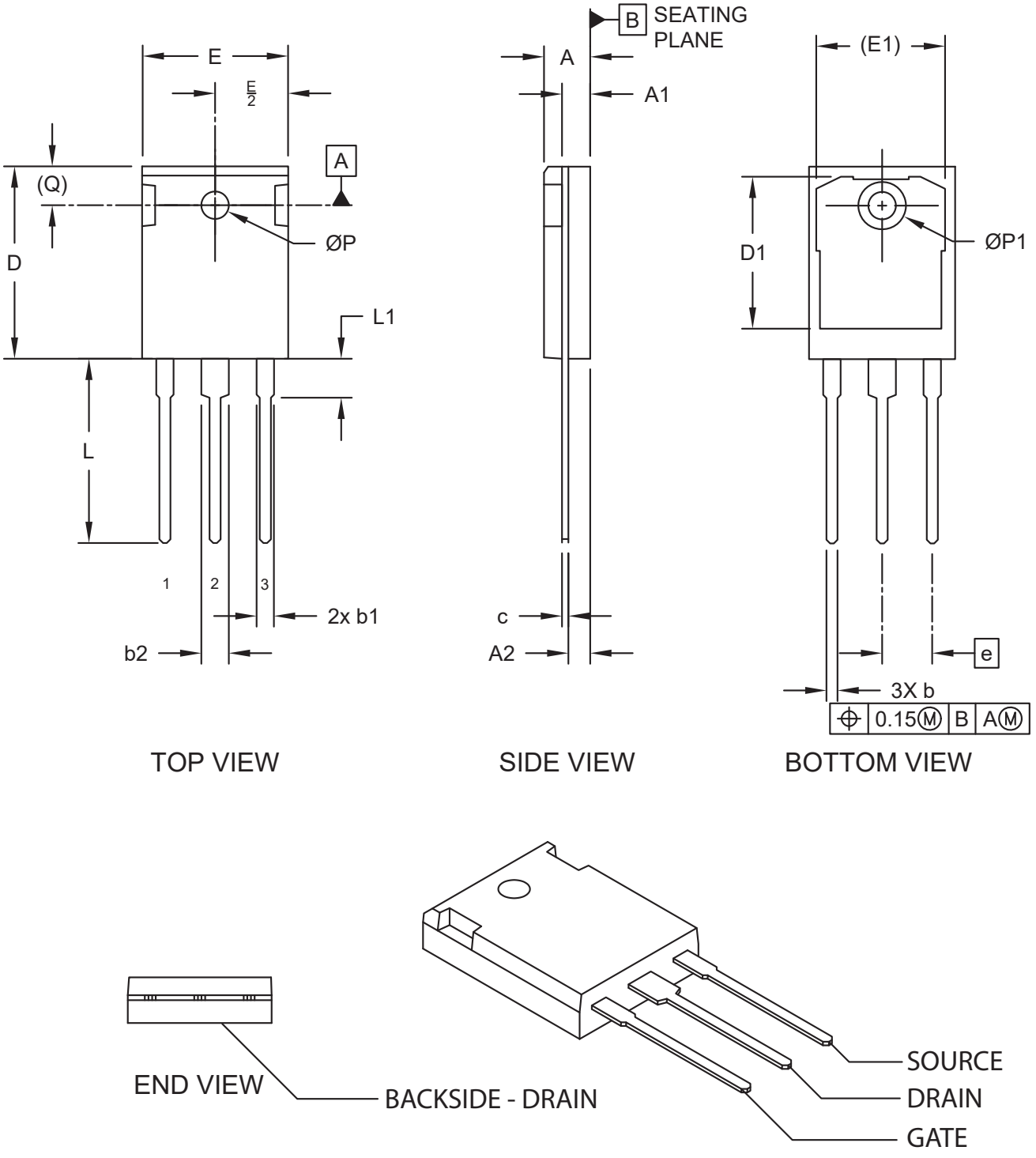
2. Package Specification

This section shows the package specification of this device.

2.1 Package Outline Drawing

The following figure illustrates the TO-247 package outline of this device.

Figure 2-1. Package Outline Drawing



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The following table shows the TO-247 dimensions and should be used in conjunction with the package outline drawing.

Table 2-1. TO-247 Dimensions

Symbol	Description	Min. (mm)	Max. (mm)
N	Number of leads	3	
e	Pitch	5.44 BSC	
A	Overall height	4.70	5.31
A1	Tab height	1.50	2.49
A2	Seating plane to lead	2.21	2.59
b	Lead width	1.02	1.40
b1	Lead shoulder width (X2)	1.65	2.41
b2	Lead shoulder width	2.87	3.38
c	Lead thickness	0.41	0.79
L	Lead length	19.81	20.32
L1	Lead shoulder length	3.99	4.50
D	Molded body length	20.80	21.46
D1	Thermal pad length	16.25	17.65
E	Total width	15.49	16.26
E1	Thermal pad width	13.10	14.50
Q	Hole center to tab edge	6.15 REF	
∅P	Hole diameter	3.51	3.81
∅P1	Thermal pad hole diameter	7.18 REF	

Notes:
Dimensioning and tolerancing per ASME Y14.5M.

- BSC: Basic dimension. Theoretically exact value shown without tolerances.
- REF: Reference dimension, usually without tolerance, for information purposes only.

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3. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 3-1. Revision History

Revision	Date	Description
C	07/2024	Added τ_M symbol for mounting torque in Table 1-2.
B	05/2024	Updated Figure 1-5.
A	04/2024	The following changes are made in this revision of the document: • Document migrated from Microsemi template to Microchip template; Assigned Microchip literature number DS-00005366A, which replaces the previous Microsemi literature number 050-7756. • Updated values in Table 1-1, Table 1-4, and Table 1-5. • Updated values for $R_{DS(on)}$, $V_{GS(th)}$, and I_{DSS} in Table 1-3. • Updated 1.3. Typical Performance Curves and 2.1. Package Outline Drawing.
Initial release (Microsemi Revision A)	09/2019	Document created.

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