High Voltage Ultra low current consumption Io=100mA LDO

■GENERAL DESCRIPTION

The NJW4182 is a 100mA output Low dropout regulator with high maximum input voltage, ultra-low current consumption and small package.

Due to the low current consumption, the NJW4182 is suitable for light load and continuously running applications such as power management microprocessor, RTC, protection circuit, security system and so on.

■PACKAGE OUTLINE



NJW4182KH1



NJW4182F

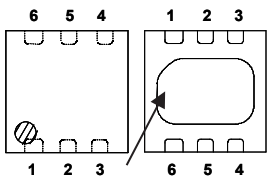


NJW4182U3

■FEATURES

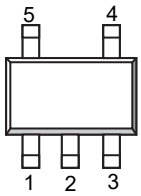
- Wide Operation Voltage Range — 4.0 to 40V
- Low Current Consumption — 9μA (typ.)
- MLCC correspond
- Output Current — I_O(min.)=100mA
- High Precision Output Voltage — V_O ±1.0%
- Internal Thermal Overload Protection
- Internal Over Current Protection
- Package Outline — DFN6-H1(ESON6-H1), SOT-23-5, SOT-89-3

■PIN CONFIGRATION



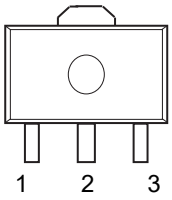
1. N.C.
2. GND
3. N.C
4. V_{IN}
5. N.C
6. V_{OUT}

NJW4182KH1



1. N.C.
2. GND
3. N.C
4. V_{OUT}
5. V_{IN}

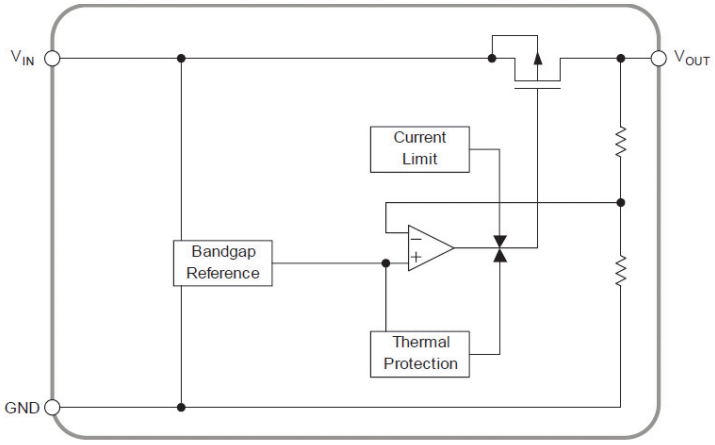
NJW4182F



1.V_{OUT}
2.GND
3.V_{IN}

NJW4182U3

■BLOCK DIAGRAM



■OUTPUT VOLTAGE RANK LIST

DFN6-H1(ESON6-H1) SOT-23-5 SOT-89-3

Device Name	V_{OUT}	Device Name	V_{OUT}	Device Name	V_{OUT}
NJW4182KH1-25	2.5V	NJW4182F25	2.5V	NJW4182U3-33	3.3V
NJW4182KH1-33	3.3V	NJW4182F33	3.3V	NJW4182U3-05	5.0V
NJW4182KH1-05	5.0V	NJW4182F05	5.0V		

■ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYNBOL	RATINGS		UNIT
Input Voltage	V_{IN}	-0.3 to +45		V
Output Voltage	V_{OUT}	-0.3 to $V_{IN} \leq 17$		V
Power Dissipation	P_D	DFN6-H1 (ESON6-H1)	450 (*1)	mW
			1200 (*2)	
		SOT-23-5	480 (*3)	
			650 (*4)	
		SOT-89-3	625(*5)	
			2400(*6)	
Junction Temperature	Tj	-40 to +150		°C
Operating Temperature	Topr	-40 to +85		°C
Storage Temperature	Tstg	-40 to +150		°C

(*1): Mounted on glass epoxy board based on EIA/JEDEC STANDARD. (101.5×114.5×1.6mm: 2Layers with Exposed Pad FR-4)

(*2): Mounted on glass epoxy board based on EIA/JEDEC STANDARD. (101.5×114.5×1.6mm: 4Layers FR-4)
(4Layers inner foil: 99.5×99.5mm, Applying a thermal via hole to a board based on JEDEC standard JESD51-5)

(*3): Mounted on glass epoxy board based on EIA/JEDEC. (114.3×76.2×1.6mm: 2Layers FR-4)

(*4): Mounted on glass epoxy board based on EIA/JEDEC. (114.3×76.2×1.6mm: 4Layers FR-4), internal Cu area: 74.2×74.2mm

(*5): Mounted on glass epoxy board. (76.2 × 114.3 × 1.6mm:based on EIA/JDEC standard size, 2Layers, Cu area 100mm^2)

(*6): Mounted on glass epoxy board. (76.2 × 114.3 × 1.6mm:based on EIA/JDEC standard, 4Layers)
(4Layers inner foil: 74.2×74.2mm, Applying a thermal via hole to a board based on JEDEC standard JESD51-5)

■ OPERATION VOLTAGE RANGE

V_{IN} = 4.0V to 40V

■ ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $V_O \geq 3V$:$V_{IN}=V_O+1V$, $C_{IN}=1.0\mu F$, $C_O=4.7\mu F$, Ta=25°C

$V_O<3V$:$V_{IN}=4V$, $C_{IN}=1.0\mu F$, $C_O=10\mu F$, Ta=25°C

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Output Voltage	V_O	I_O=30mA		-1.0%	-	+1.0%	V
Quiescent Current	I_Q	I_O=0mA		-	9	18	μA
Output Current	Io	$V_O \times 0.9$		100	-	-	mA
Line Regulation	$\Delta V_O/\Delta V_{IN}$	V_{IN}= V_O +1V to 40V, I_O =30mA($V_O \geq 3V$), V_{IN}= 4V to 40V, I_O =30mA(V_O <3V)		-	-	0.05	%/V
Load Regulation	$\Delta V_O/\Delta I_O$	I_O=0mA to 100mA		-	-	0.018	%/mA
Dropout Voltage(*7)	ΔV_{IO}	I_O=60mA		-	0.18	0.3	V
Ripple Rejection	RR	V_{IN} = 5V, ein = 50mVrms, f=1kHz, Io=10mA	Vo=2.5V	-	54	-	dB
		V_{IN}= V_O+2V, ein = 50mVrms, f = 1kHz , Io = 10mA	Vo=3.3V	-	52	-	
			Vo=5.0V	-	48	-	
Average Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta Ta$	Ta=0 to 85°C, I_O=30mA		-	±50	-	ppm/°C

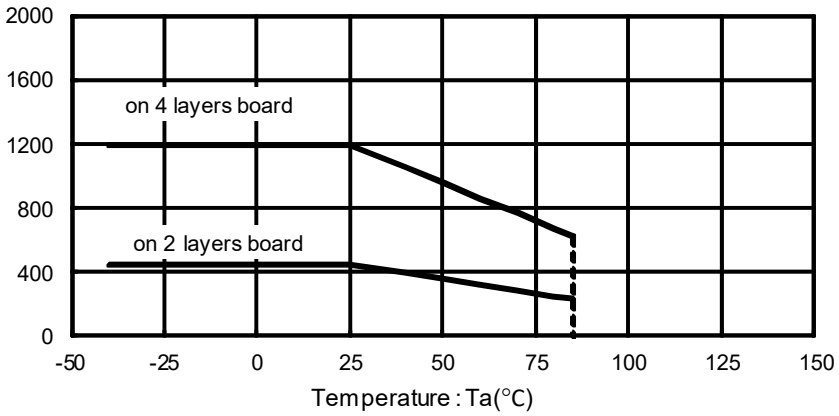
(*7): The output voltage excludes under 3.8V.

The above specification is a common specification for all output voltages.

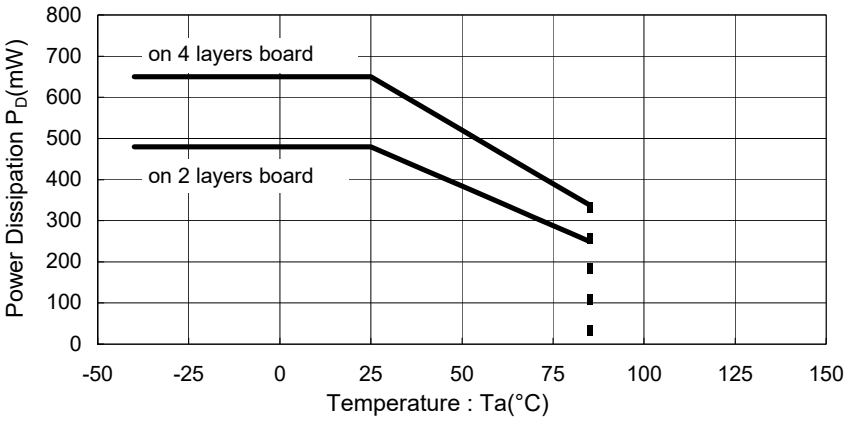
Therefore, it may be different from the individual specification for a specific output voltage.

■ POWER DISSIPATION vs. AMBIENT TEMPERATURE

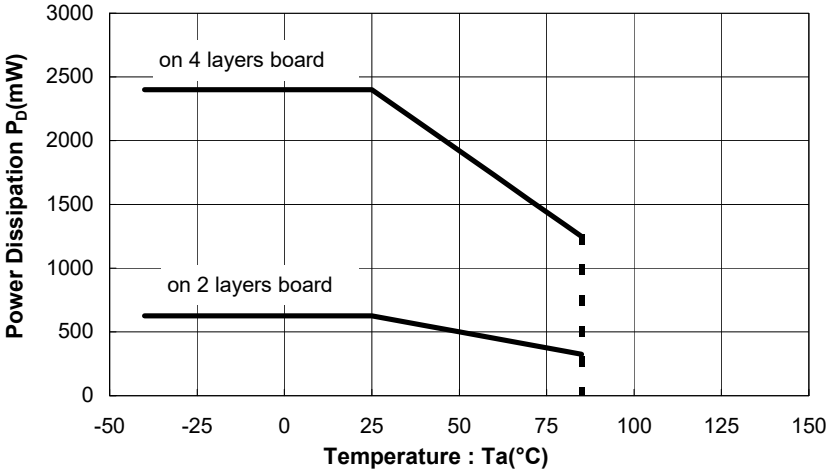
NJW4182KH1 PowerDissipation
(Topr=-40~+85°C,Tj=150°C)



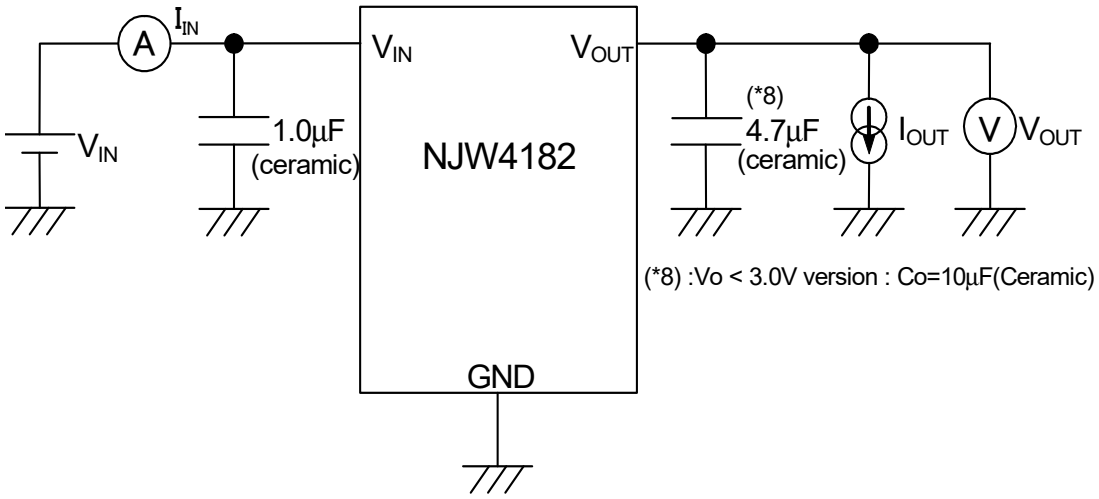
NJW4182F PowerDissipation
(Topr=-40~+85°C,Tj=150°C)



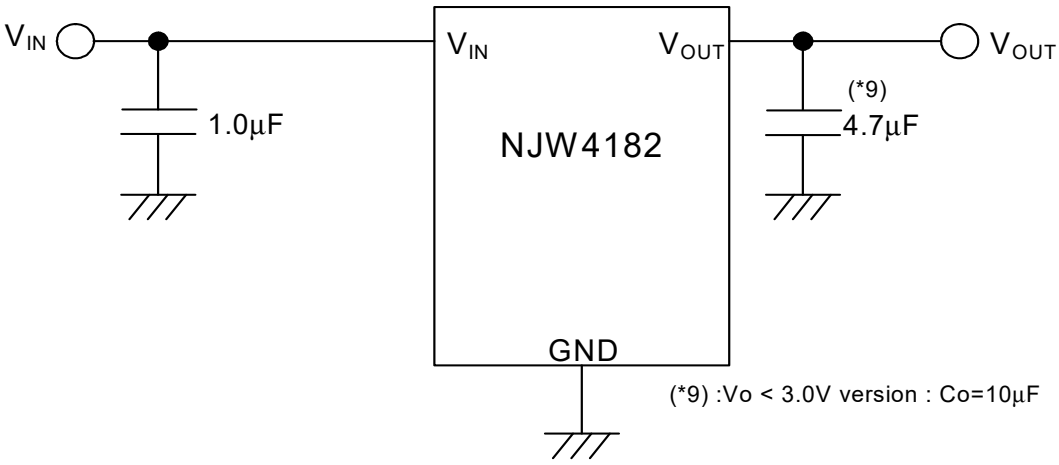
NJW4182U3 PowerDissipation
(Topr= -40~+85°C,Tj=150°C)



■ TEST CIRCUIT



■ TYPICAL APPLICATION



*Input Capacitor C_{IN}

Input Capacitor C_{IN} is required to prevent oscillation and reduce power supply ripple for applications when high power supply impedance or a long power supply line.

Therefore, use the recommended C_{IN} value (refer to conditions of ELECTRIC CHARACTERISTIC) or larger and should connect between GND and V_{IN} as shortest path as possible to avoid the problem.

*Output Capacitor C_O

Output capacitor (C_O) will be required for a phase compensation of the internal error amplifier.

The capacitance and the equivalent series resistance (ESR) influence to stable operation of the regulator.

Use of a smaller C_O may cause excess output noise or oscillation of the regulator due to lack of the phase compensation.

On the other hand, Use of a larger C_O reduces output noise and ripple output, and also improves output transient response when rapid load change.

Therefore, use the recommended C_O value (refer to conditions of ELECTRIC CHARACTERISTIC) or larger and should connect between GND and V_{OUT} as shortest path as possible for stable operation

The recommended capacitance depends on the output voltage rank. Especially, low voltage regulator requires larger C_O value.

In addition, you should consider varied characteristics of capacitor (a frequency characteristic, a temperature characteristic, a DC bias characteristic and so on) and unevenness peculiar to a capacitor supplier enough.

When selecting C_O, recommend that have withstand voltage margin against output voltage and superior temperature characteristic though this product is designed stability works with wide range ESR of capacitor including low ESR products.

*Overshoot of Output Voltage

Transient fluctuation of output voltage tends to be large compared to other typical regulators because the NJW4182 is designed with the concept of low current consumption characteristics.

In general, overshoot or undershoot of output voltage is more likely to occur when the following cases.

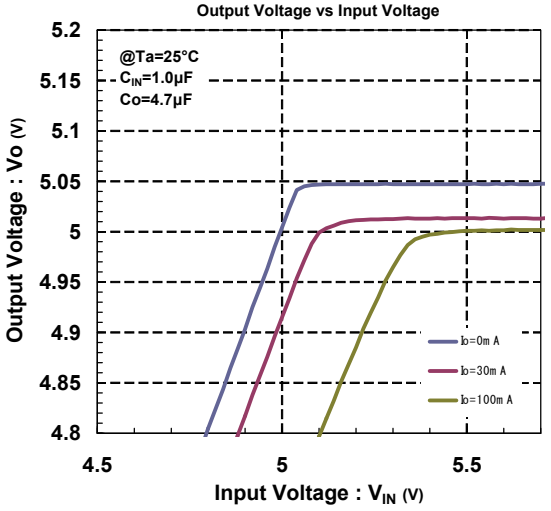
- When input voltage or output current fluctuate sharply
- When output capacitance is small
- When output load is light
- When start up from the condition of narrow voltage difference between an Input and an output.

The NJW4182 can reduce overshoot voltage compared to other low current consumption products by a built-in overshoot protection (OSP).
However, very large overshoot may occur because of delay of the OSP circuit when the input voltage rises from between 2.0V and 2.5V.
The value of overshoot varies with composite conditions, please refer the above and check the actual condition.
In addition, the following measures will be mentioned as a method to reduce the overshoot value.

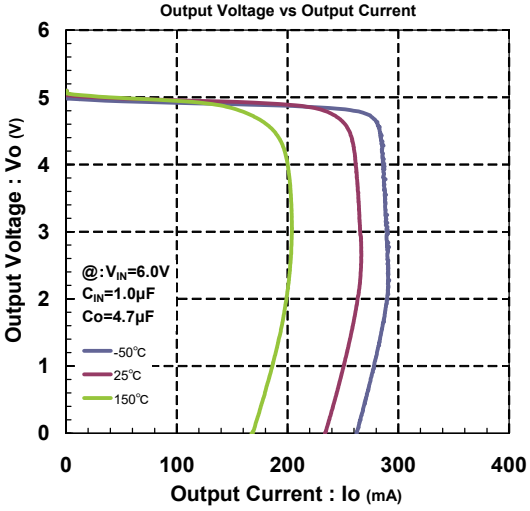
a. By increasing the input and output capacitors to absorb overshoot value.
b. Adjust the rising speed of the input voltage, to avoid rising from between 2.0V and 2.5V.

■ TYPICAL CHARACTERISTICS

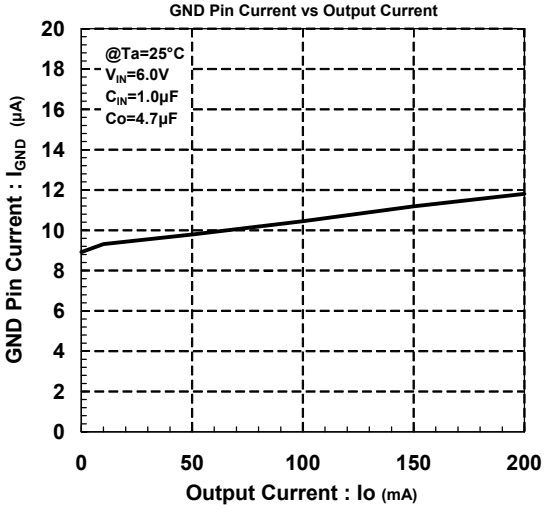
NJW4182_5.0V
Output Voltage vs Input Voltage



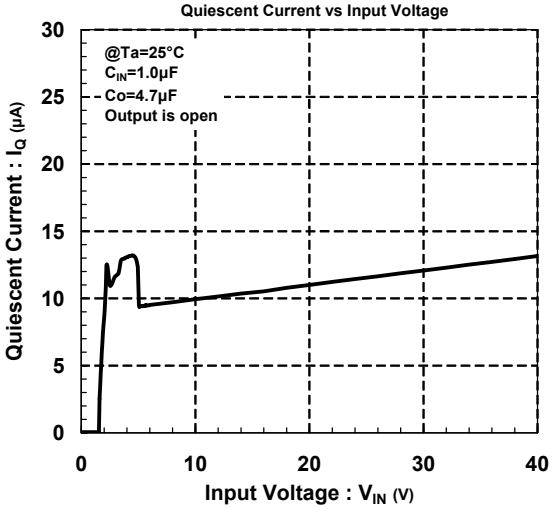
NJW4182_5.0V
Output Voltage vs Output Current



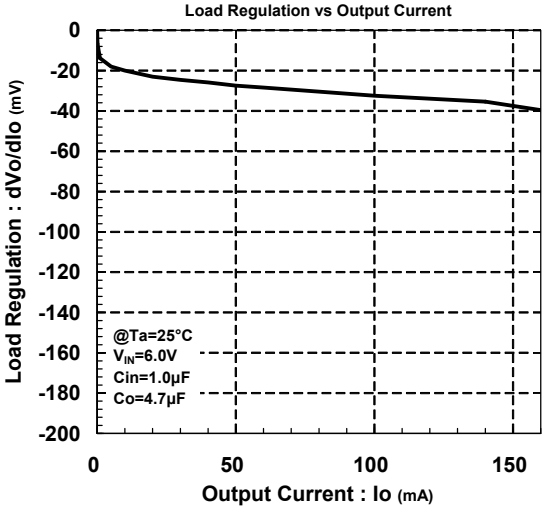
NJW4182_5.0V
GND Pin Current vs Output Current



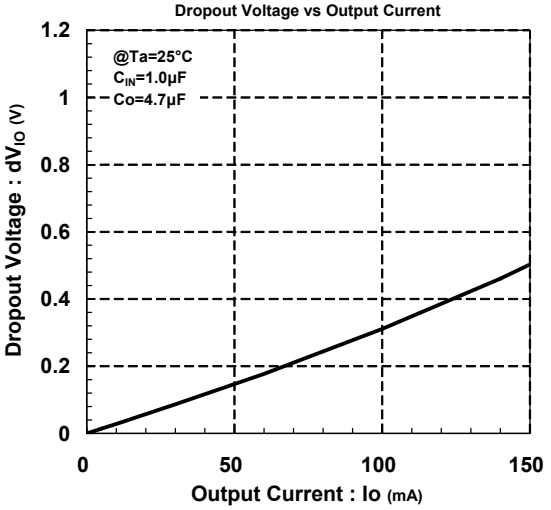
NJW4182_5.0V
Quiescent Current vs Input Voltage



NJW4182_5.0V
Load Regulation vs Output Current

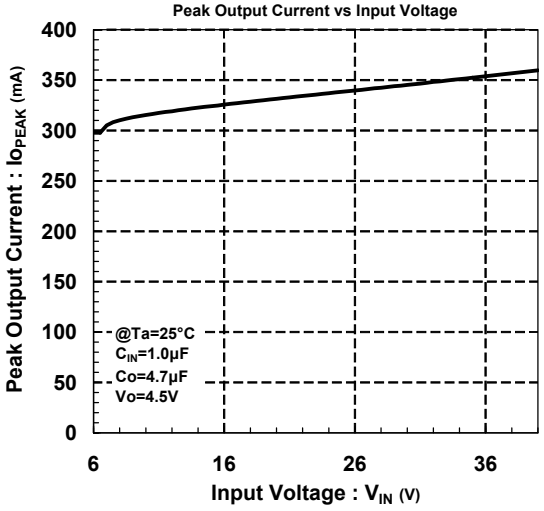


NJW4182_5.0V
Dropout Voltage vs Output Current



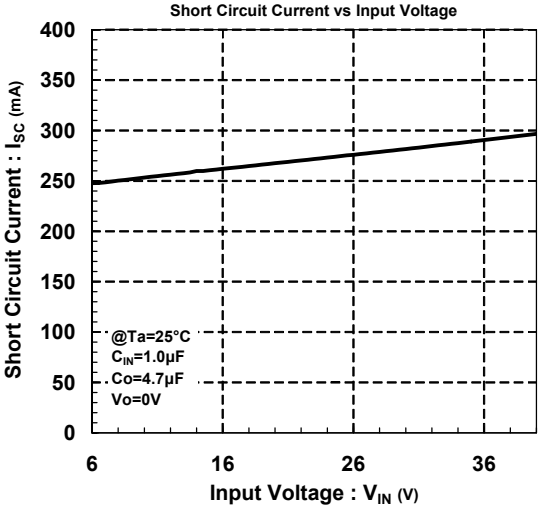
NJW4182_5.0V

Peak Output Current vs Input Voltage



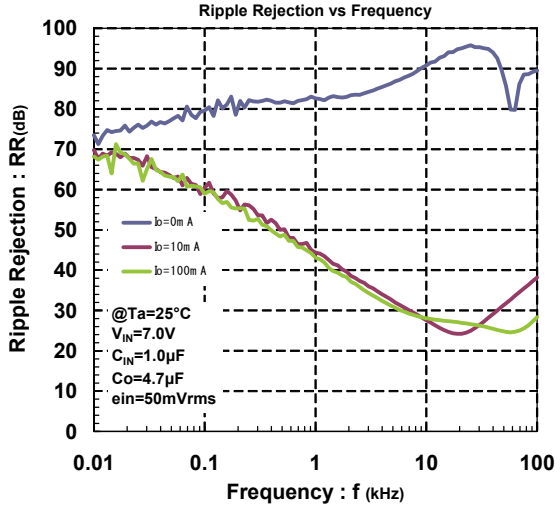
NJW4182_5.0V

Short Circuit Current vs Input Voltage



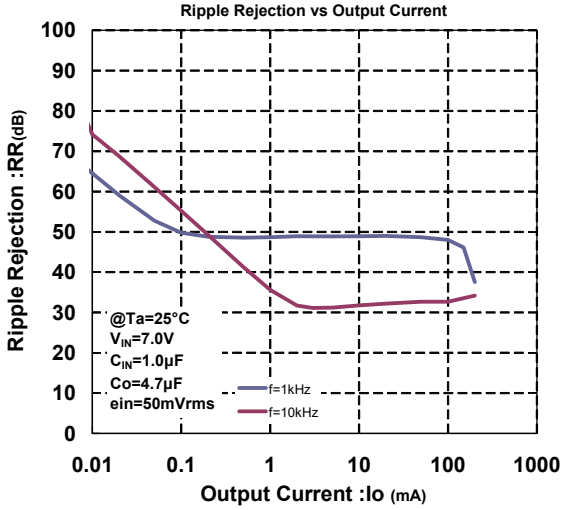
NJW4182_5.0V

Ripple Rejection vs Frequency



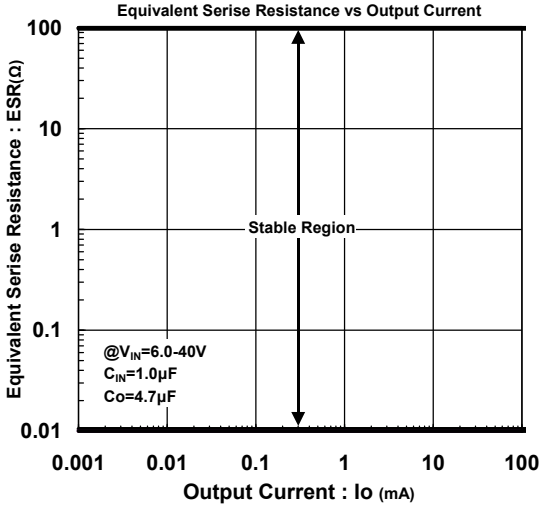
NJW4182_5.0V

Ripple Rejection vs Output Current



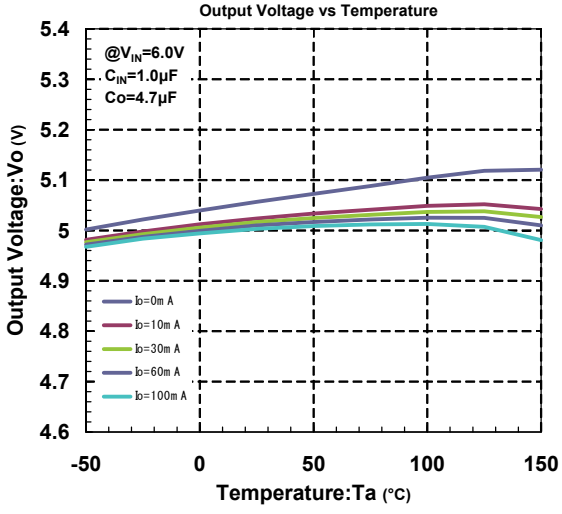
NJW4182_5.0V

Equivalent Serise Resistance vs Output Current



NJW4182_5.0V

Output Voltage vs Temperature



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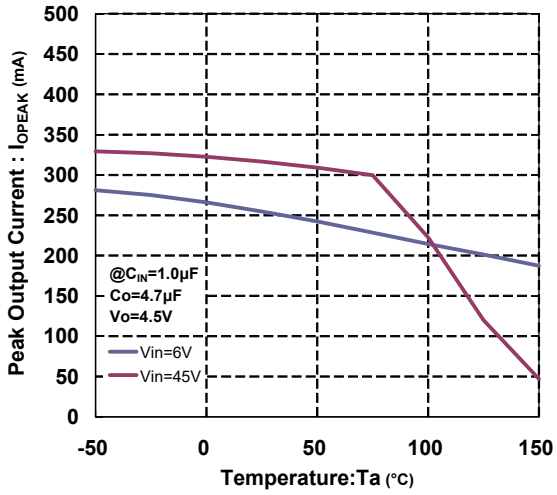
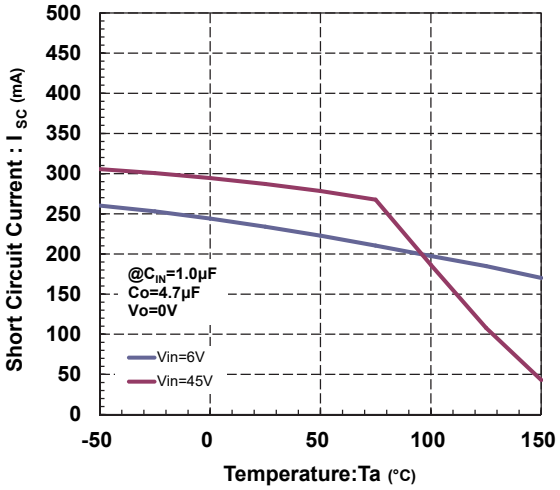
Peak Output Current vs Temperature



NJW4182_5.0V

Short Circuit Current vs Temperature



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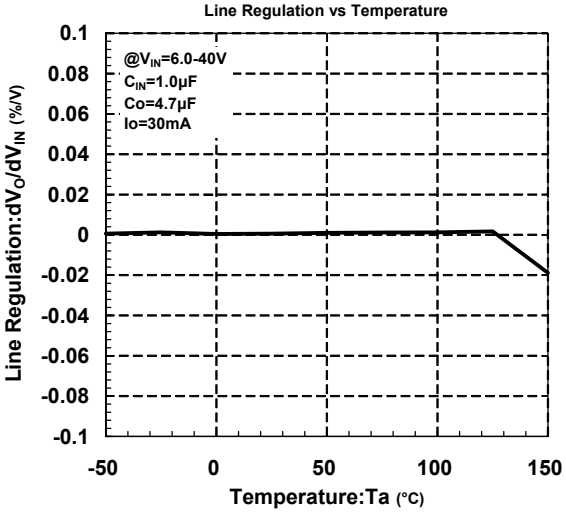
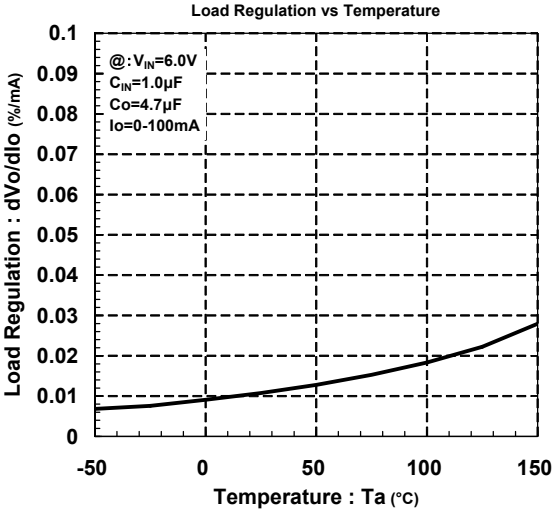
Line Regulation vs Temperature



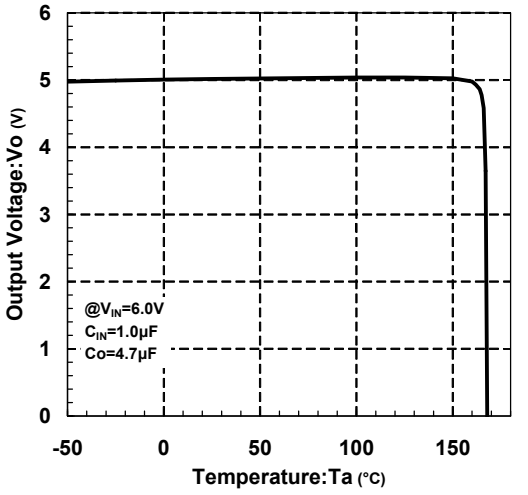
NJW4182_5.0V

Load Regulation vs Temperature



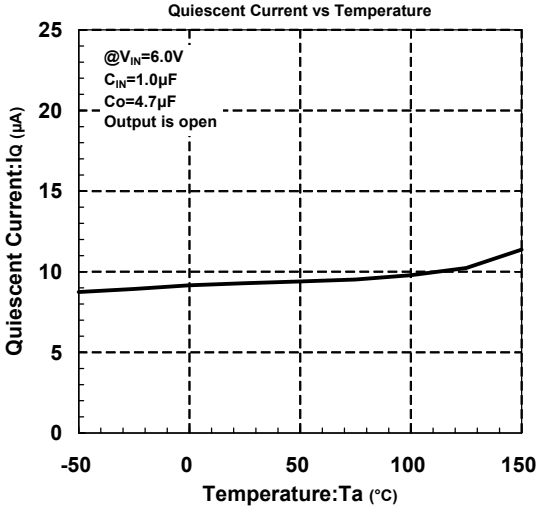
NJW4182_5.0V

Output Voltage vs Temperature



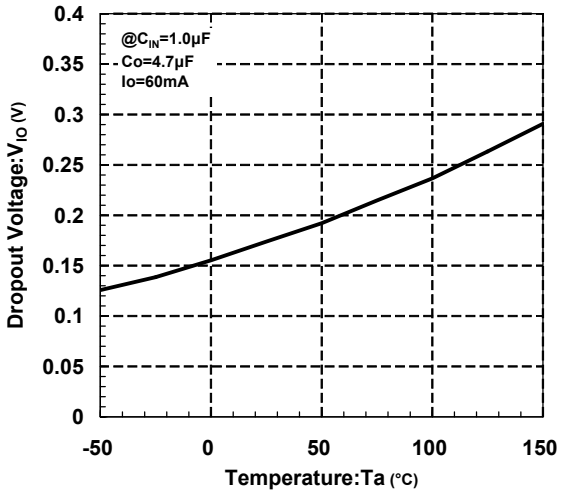
NJW4182_5.0V

Quiescent Current vs Temperature



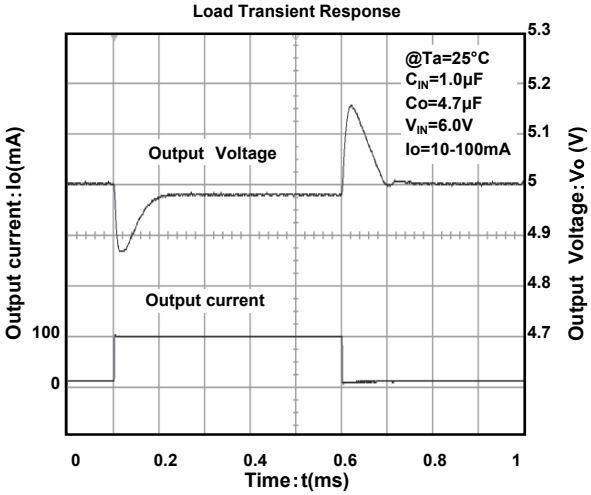
NJW4182_5.0V

Dropout Voltage vs. Temperature



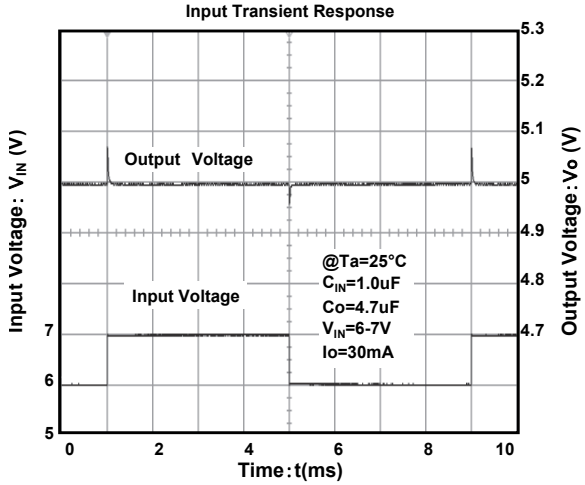
NJW4182_5.0V

Load Transient Response



NJW4182_5.0V

Input Transient Response



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