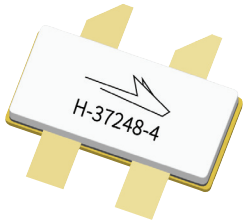
PXAC210552FC

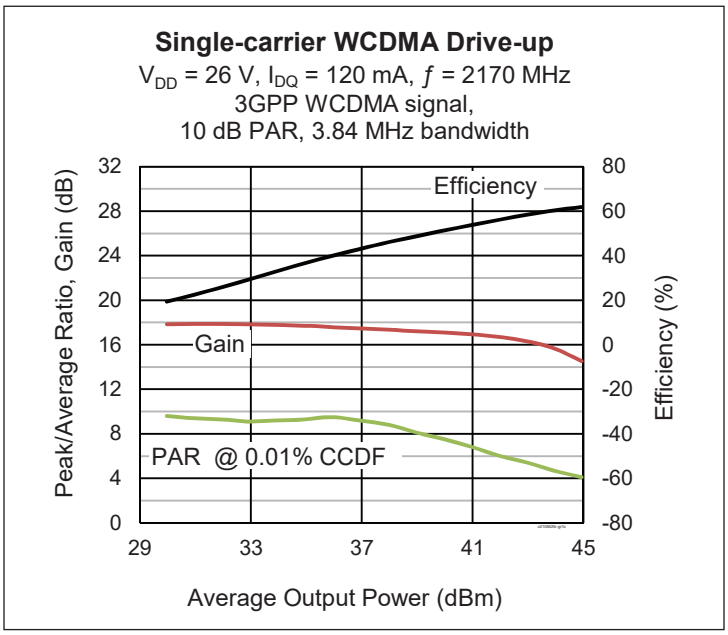
Thermally-Enhanced High Power RF LDMOS FET
55 W, 28 V, 1805 – 2170 MHz

Description

The PXAC210552FC is a 55-watt LDMOS FET with an asymmetric design for use in multi-standard cellular power amplifier applications in the 1805 to 2170 MHz frequency band. It features dual-path design, input and output matching, and a thermally-enhanced package with earless flange. Manufactured with Wolfspeed's advanced LDMOS process, this device provides excellent thermal performance and superior reliability.



PXAC210552FC
Package H-37248-4



Features

- Broadband internal matching
- Asymmetric Doherty design
  - Main: P1dB = 20 W Typ
  - Peak: P1dB = 35 W Typ
- CW performance, 2170 MHz, 26 V
  - Output power at P_{1dB} = 27 W
  - Gain = 17 dB
  - Efficiency = 59%
- Integrated ESD protection
- ESD: Human Body Model, Class 1B (per ANSI/ESDA/JEDEC JS-001)
- Capable of handling 10:1 VSWR @28 V, 55 W (CW) output power
- Low thermal resistance
- Pb-free and RoHS compliant

RF Characteristics

Single-carrier WCDMA Specifications (tested in Wolfspeed Doherty test fixture)

V_{DD} = 26 V, $V_{GS(peak)}$ = 1.5 V, I_{DQ} = 120 mA, P_{OUT} = 39 dBm average, f = 2170 MHz. 3GPP WCDMA signal: 3.84 MHz bandwidth, 10 dB PAR @0.01% CCDF.

Characteristic	Symbol	Min	Typ	Max	Unit
Linear Gain	G_{ps}	16	17.2	—	dB
Drain Efficiency	η_D	46	49	—	%
Adjacent Channel Power Ratio	ACPR	—	–29	–25	dBc

All published data at T_{CASE} = 25°C unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

DC Characteristics

Characteristic		Conditions	Symbol	Min	Typ	Max	Unit
Drain-source Breakdown Voltage		V_{GS} = 0 V, I_{DS} = 10 mA	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current (main and peak)		V_{DS} = 28 V, V_{GS} = 0 V	I_{DSS}	—	—	0.1	µA
		V_{DS} = 63 V, V_{GS} = 0 V	I_{DSS}	—	—	1.0	µA
Gate Leakage Current		V_{GS} = 10 V, V_{DS} = 0 V	I_{GSS}	—	—	0.1	µA
On-state Resistance	(main)	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	0.38	—	Ω
	(peak)	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	0.19	—	Ω
Operating Gate Voltage	(main)	V_{DS} = 26 V, I_{DQ} = 120 mA	V_{GS}	2.16	2.65	3.15	V
	(peak)	V_{DS} = 26 V, I_{DQ} = 0 mA	V_{GS}	1.00	1.50	2.00	V

Maximum Ratings

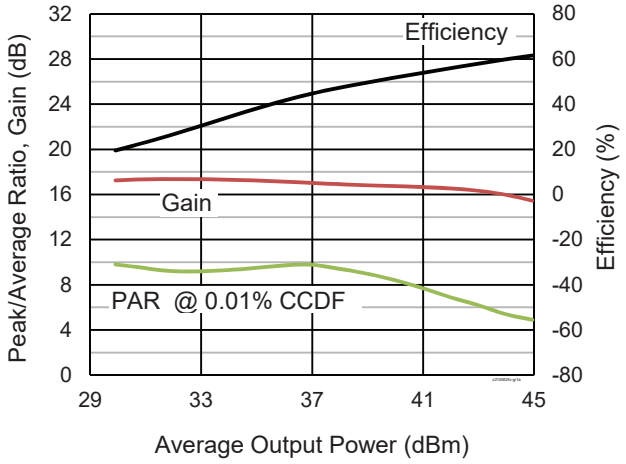
Parameter	Symbol	Value	Unit
Drain-source Voltage	V_{DSS}	65	V
Gate-source Voltage	V_{GS}	–6 to +10	V
Operating Voltage	V_{DD}	0 to +32	V
Junction Temperature	T_J	225	°C
Storage Temperature Range	T_{STG}	–65 to +150	°C
Thermal Resistance (T_{CASE} = 70°C, 26 V, 8 W CW)	$R_{\theta JC}$	1.44	°C/W

Ordering Information

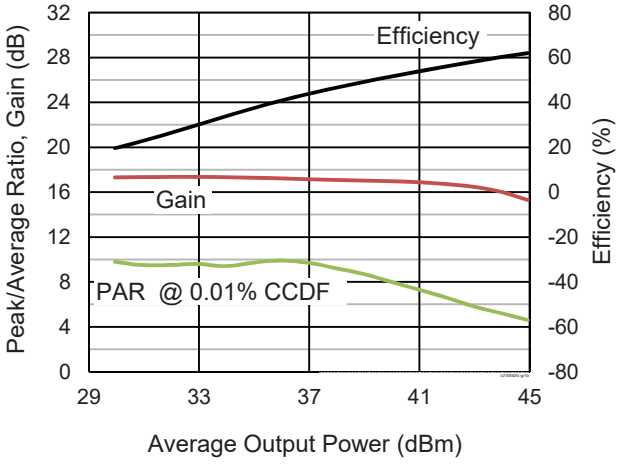
Type and Version	Order Code	Package and Description	Shipping
PXAC210552FC V1 R0	PXAC210552FC-V1-R0	H-37248-4, ceramic open-cavity, earless	Tape & Reel, 50 pcs
PXAC210552FC V1 R2	PXAC210552FC-V1-R2	H-37248-4, ceramic open-cavity, earless	Tape & Reel, 250 pcs

Typical Performance (data taken in Wolfspeed Doherty reference test fixture)

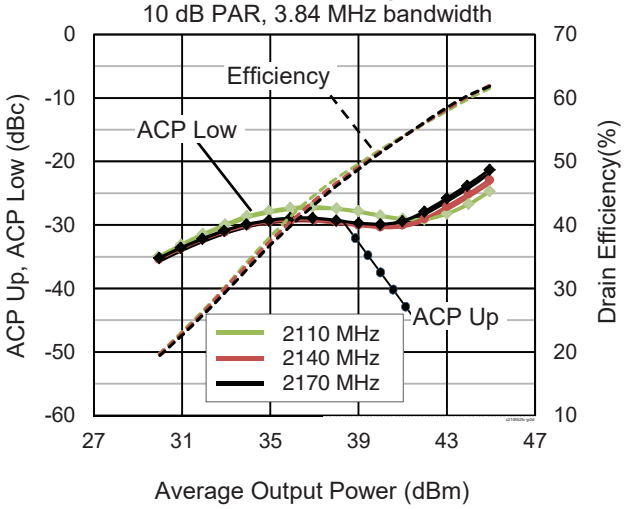
Single-carrier WCDMA Drive-up
V_{DD} = 26 V, I_{DQ} = 120 mA, f = 2110 MHz
3GPP WCDMA signal,
10 dB PAR, 3.84 MHz bandwidth



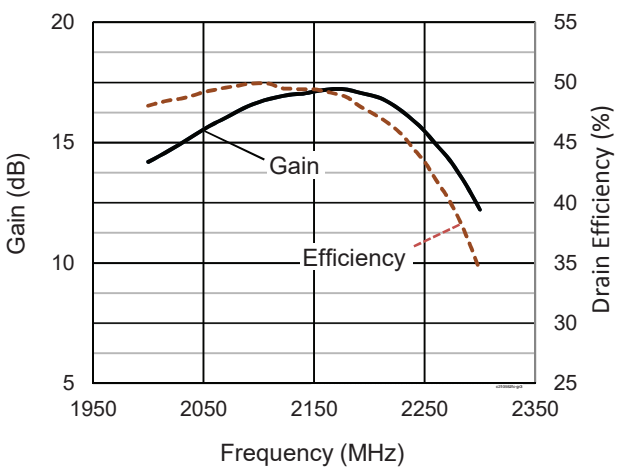
Single-carrier WCDMA Drive-up
V_{DD} = 26 V, I_{DQ} = 120 mA, f = 2140 MHz
3GPP WCDMA signal,
10 dB PAR, 3.84 MHz bandwidth



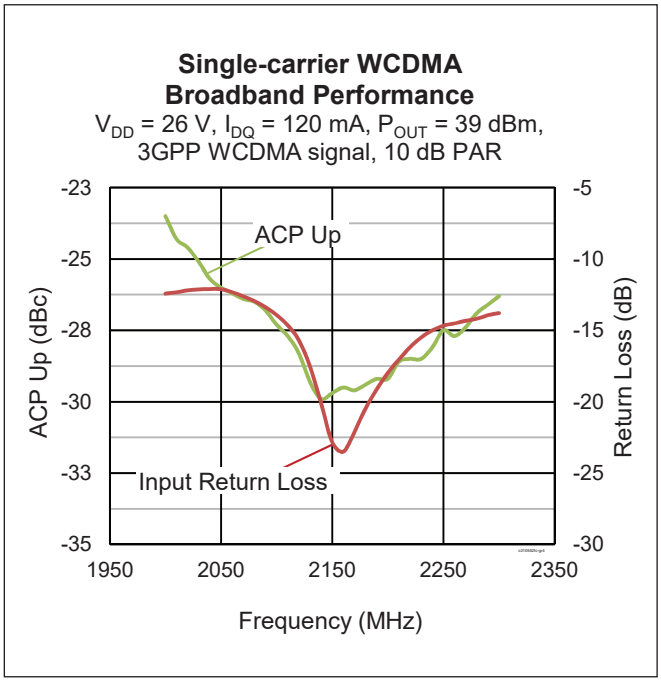
Single-carrier WCDMA 3GPP Drive-up
V_{DD} = 26 V, I_{DQ} = 120 mA,
f = 2110, 2140, 2170 MHz
3GPP WCDMA signal,
10 dB PAR, 3.84 MHz bandwidth

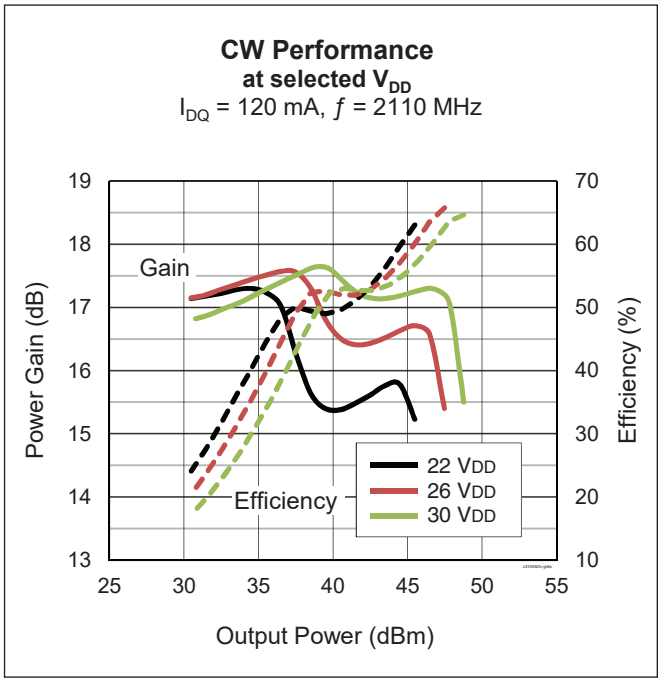


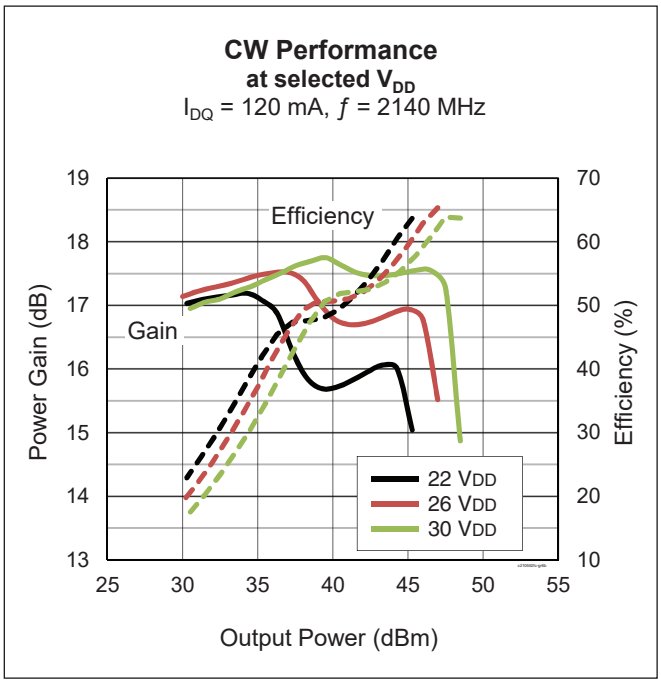
Single-carrier WCDMA Broadband Performance
V_{DD} = 26 V, I_{DQ} = 120 mA, P_{OUT} = 39 dBm,
3GPP WCDMA signal, 10 dB PAR

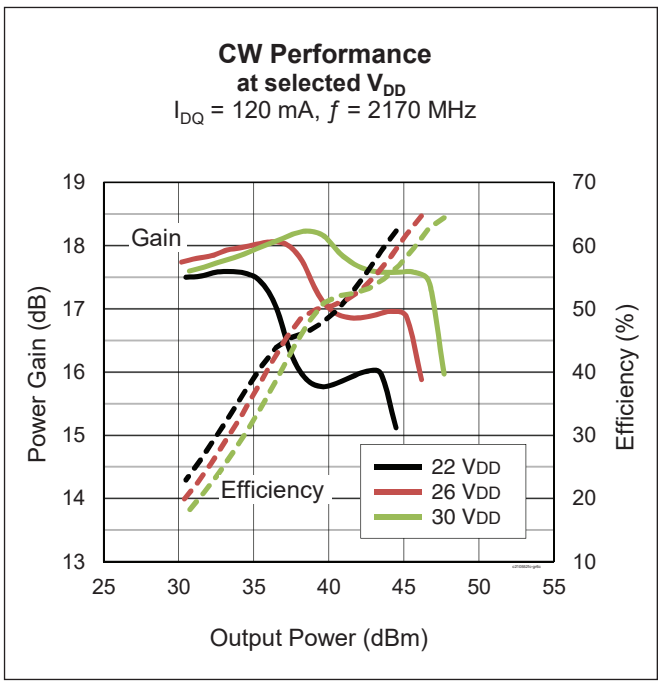


Typical Performance (cont.)

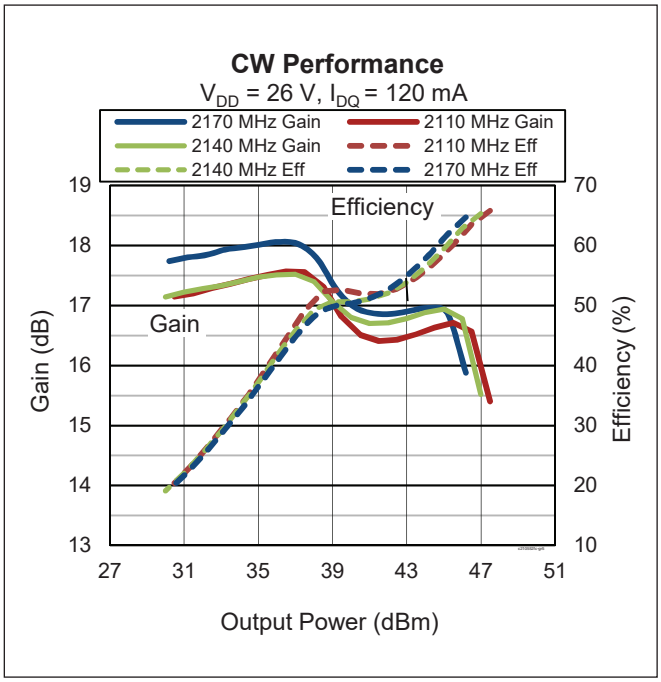


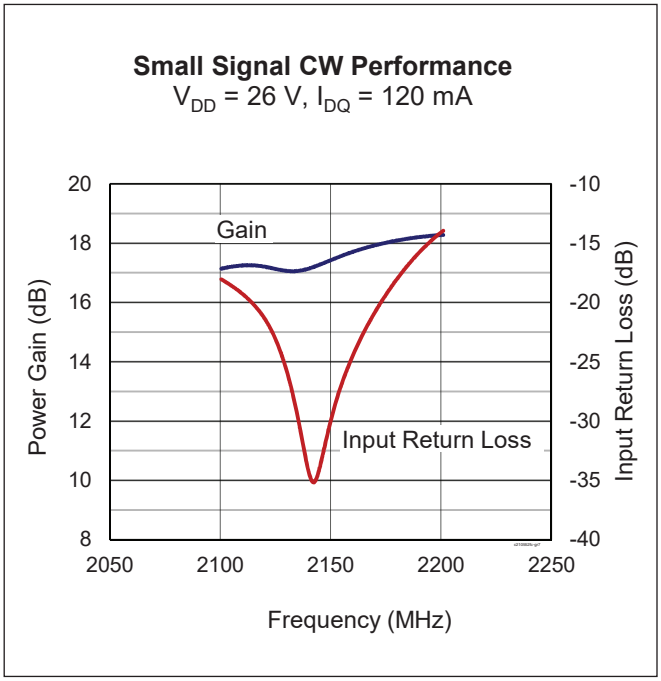






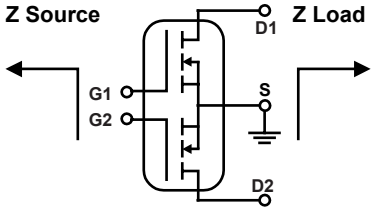
Typical Performance (cont.)





See next page for load pull information

Load Pull Performance



Main side pulsed CW signal: 160 µsec, 10% duty cycle, V_{DD} = 26 V, I_{DQ} = 120 mA

		P_{1dB}									
Class AB		Max Output Power					Max PAE				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	PAE [%]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	PAE [%]
2110	19.70 – j30.49	11.34 – j3.06	20.9	43.74	23.7	59.4	11.02 – j3.49	22.3	42.70	18.6	66.0
2140	17.03 – j36.14	9.73 – j2.15	20.9	43.48	22.3	58.6	9.78 – j3.58	22.9	42.26	16.8	64.6
2170	34.36 – j32.08	10.27 – j2.68	20.8	43.71	23.5	58.4	9.47 – j3.32	22.5	42.53	17.9	64.6

Peak side pulsed CW signal: 160 µsec, 10% duty cycle, V_{DD} = 26 V, $V_{GS(peak)}$ = 1.5 V

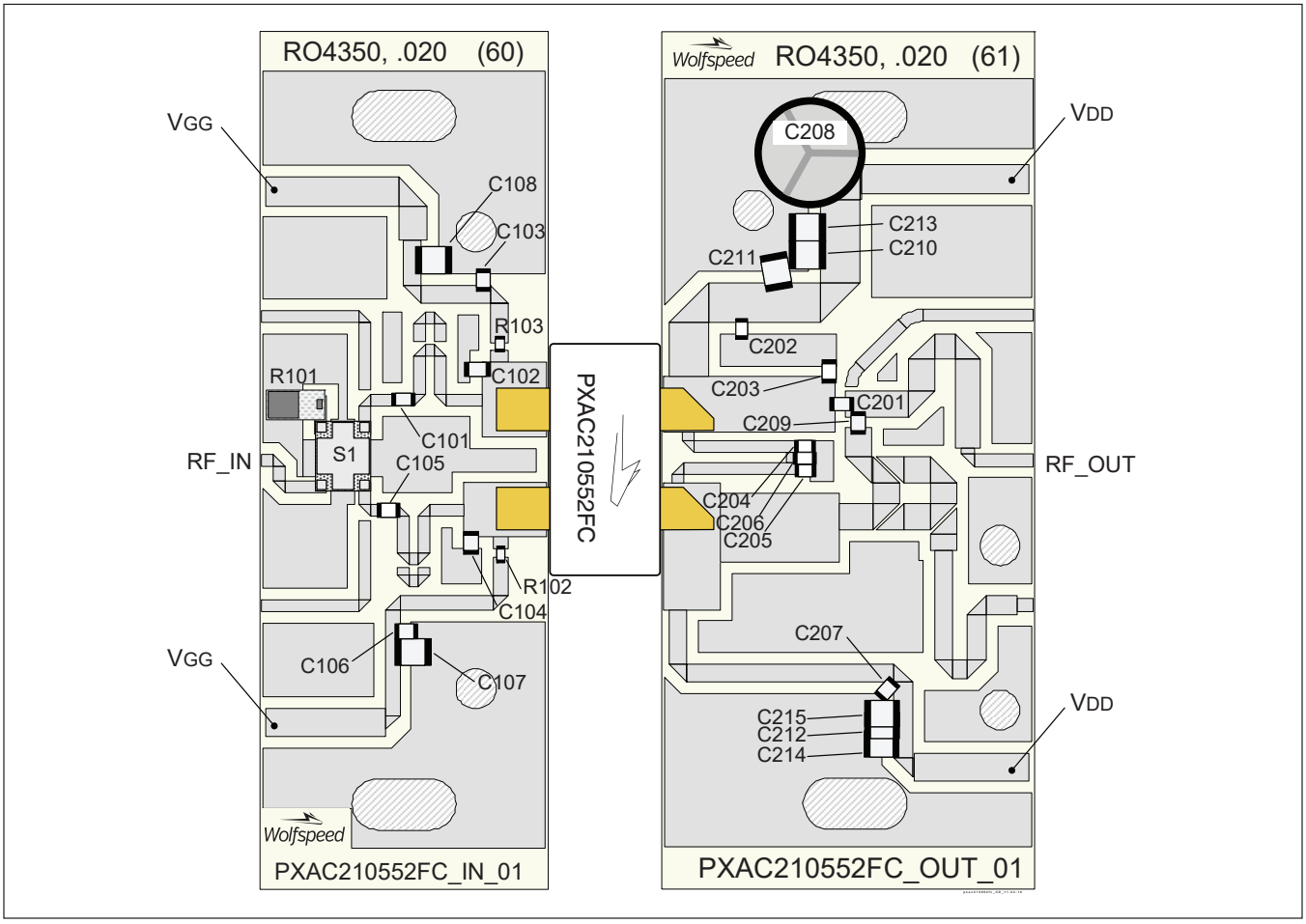
		P_{1dB}									
Class C		Max Output Power					Max PAE				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	PAE [%]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	PAE [%]
2110	9.80 – j12.90	3.28 – j4.71	15.5	47.56	57.0	60.7	4.00 – j1.52	16.5	45.6	36.3	71.8
2140	10.71 – j17.59	3.51 – j5.03	16.0	47.50	56.2	60.7	3.88 – j1.93	17.0	45.9	38.7	71.3
2170	15.51 – j13.51	3.58 – j5.14	15.6	47.53	56.6	60.0	3.69 – j1.47	16.6	45.4	34.9	70.9

Reference Circuit, tuned for 2110 – 2170 MHz

DUT	PXAC210552FC
Test Fixture Part No.	LTA/PXAC210552FC V1
PCB	Rogers 4350, 0.508 mm [.020"] thick, 2 oz. copper, ε_r = 3.66

Find Gerber files for this reference fixture on the Wolfspeed Web site at **www.wolfspeed.com/RF**

Reference Circuit (cont.)



Reference circuit assembly diagram (not to scale)

Component Information

Component	Description	Manufacturer	P/N
Input			
C101, C103, C105, C106	Capacitor, 18 pF	ATC	ATC600F180GW250T
C102	Capacitor, 0.5 pF	ATC	ATC600F0R5CW250T
C104	Capacitor, 0.8 pF	ATC	ATC600F0R8CW250T
C107, C108	Capacitor, 10 µF	Taiyo Yuden	UMK325C7106MM-T
R101	Termination, 50 ohms	Anaren	C8A50Z4A
R102, R103	Resistor, 10 ohms	Panasonic	ERJ-3GEYJ100V
U1	Hybrid coupler	Anaren	X3C21P1-03S

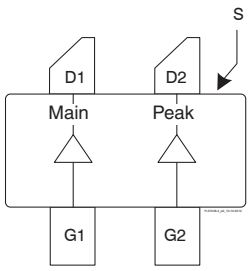
table continued next page

Reference Circuit (cont.)

Component Information (cont.)

Component	Description	Manufacturer	P/N
Output			
C201	Capacitor, 5.1 pF	ATC	ATC600F5R1BW250T
C202, C204, C205, C207, C209	Capacitor, 18 pF	ATC	ATC600F180GW250T
C203	Capacitor, 0.8 pF	ATC	ATC600F0R8CW250T
C206	Capacitor, 0.1 µF	Panasonic	ECJ-3VB1H104K
C208	Capacitor, 220 µF	Cornell Dubilier Electronics (CDE)	SK221M050ST
C210, C211, C212 C213, C214, C215	Capacitor, 10 µF	Taiyo Yuden	UMK325C7106MM-T

Pinout Diagram (top view)



Pin	Description
D1	Drain device 1 (main)
D2	Drain device 2 (peak)
G1	Gate device 1 (main)
G2	Gate device 2 (peak)
S	Source (flange)

Package Outline Specifications

Package H-37248-4

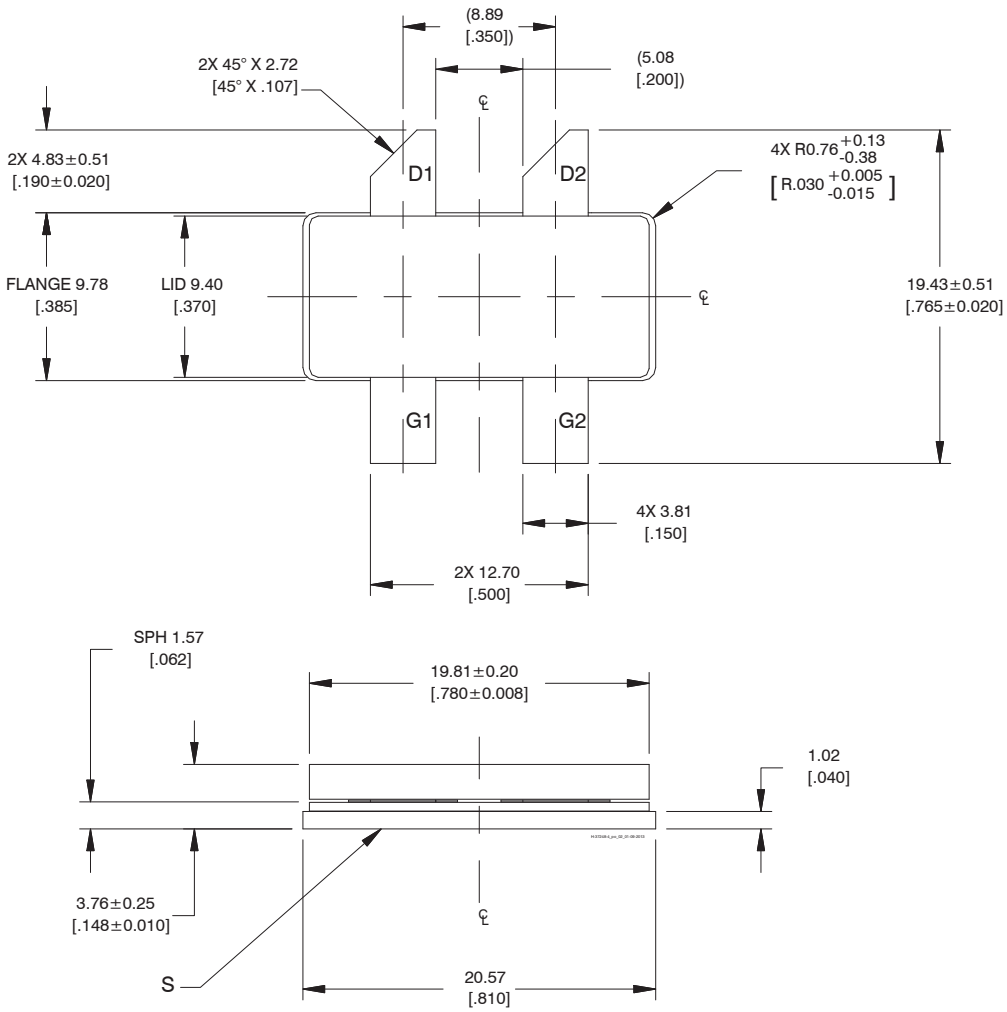


Diagram Notes—unless otherwise specified:

1. Interpret dimensions and tolerances per ASME Y14.5M-1994.
2. Primary dimensions are mm, alternate dimensions are inches.
3. All tolerances ± 0.127 [.005].
4. Pins: D1, D2 – drain; G1, G2 – gate; S (flange) – source.
5. Lead thickness: 0.10 +0.076/–0.025 [.004 +.003/–.001].
6. Gold plating thickness: 1.14 ± 0.38 micron [45 ± 15 microinch].

Revision History

Revision	Date	Data Sheet Type	Page	Subjects (major changes since last revision)
01	2015-03-02	Advance	All	Proposed specification for new product development.
02	2015-12-04	Production	All	Information for production-released product, including firm specifications, operating performance, and reference circuit specifications.
03	2018-07-02	Production	All	Converted to Wolfspeed Data Sheet

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Notes

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