FEATURES

- RoHS Compliant
- Halogen-Free according to IEC 61249-2-21

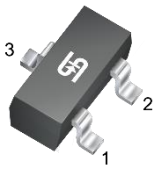
APPLICATIONS

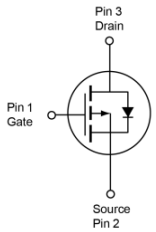
- Load Switch

PRODUCT SUMMARY			
PARAMETER		**VALUE**	**UNIT**
V_{DS}		-60	V
$R_{DS(on)}$ (max)	V_{GS} = -10V	190	mΩ
	V_{GS} = -4.5V	240	
Q_g	V_{GS} = -10V	8.2	nC

Pb-Free RoHS COMPLIANT HALOGEN FREE

SOT-23





Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)				
PARAMETER		**SYMBOL**	**LIMIT**	**UNIT**
Drain-Source Voltage		V_{DS}	-60	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	-3.1	A
	T_C = 100°C		-2	
Pulsed Drain Current		I_{DM}	-12.4	A
Total Power Dissipation	T_A = 25°C	P_D	1.56	W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

THERMAL RESISTANCE			
PARAMETER	**SYMBOL**	**MAXIMUM**	**UNIT**
Thermal Resistance – Junction to Ambient	$R_{\Theta JA}$	80	°C/W

Note: $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. $R_{\Theta JA}$ is guaranteed by design while $R_{\Theta CA}$ is determined by the user's board design. $R_{\Theta JA}$ shown below for single device operation on FR-4 PCB with minimum recommended footprint in still air.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)						
PARAMETER	**CONDITIONS**	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = -250μA	BV_{DSS}	-60	--	--	V
Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = -250μA	$V_{GS(TH)}$	-1.2	-1.9	-2.5	V
Gate-Source Leakage Current	V_{GS} = ±20V, V_{DS} = 0V	I_{GSS}	--	--	±100	nA
Drain-Source Leakage Current	V_{GS} = 0V, V_{DS} = -60V	I_{DSS}	--	--	-1	μA
	V_{GS} = 0V, V_{DS} = -48V T_J = 125°C		--	--	-10	
Drain-Source On-State Resistance (Note 1)	V_{GS} = -10V, I_D =-3A	$R_{DS(on)}$	--	160	190	mΩ
	V_{GS} = -4.5V, I_D = -1.5A		--	200	240	
Forward Transconductance (Note 1)	V_{DS} = -10V, I_D = -3A	g_{fs}	--	3.5	--	S
Dynamic						
Total Gate Charge	V_{GS} = -10V, V_{DS} = -30V I_D = -3A	Q_g	--	8.2	--	nC
Gate-Source Charge		Q_{gs}	--	1.8	--	
Gate-Drain Charge		Q_{gd}	--	1.5	--	
Input Capacitance	V_{GS} = 0V, V_{DS} = -30V, f = 1.0MHz	C_{iss}	--	425	--	pF
Output Capacitance		C_{oss}	--	35	--	
Reverse Transfer Capacitance		C_{rss}	--	20	--	
Switching (Note 2)						
Turn-On Delay Time	V_{GS} = -10V,V_{DS} = -30V, I_D = -1A, R_G = 6Ω	$t_{d(on)}$	--	5.2	--	ns
Rise Time		t_r	--	19	--	
Turn-Off Delay Time		$t_{d(off)}$	--	35	--	
Fall Time		t_f	--	10.6	--	
Source-Drain Diode						
Maximum Continuous Drain-Source Diode Forward Current	Integral reverse diode in the MOSFET	I_S	--	--	-3.1	A
Maximum Pulse Drain-Source Diode Forward Current		I_{SM}	--	--	-12.4	A
Diode Forward Voltage (Note 1)	V_{GS} = 0V, I_S = -1A	V_{SD}	--	--	-1	V

Notes:

1. Pulse test: Pulse Width ≤ 300μs, duty cycle ≤ 2%.
2. Switching time is essentially independent of operating temperature.

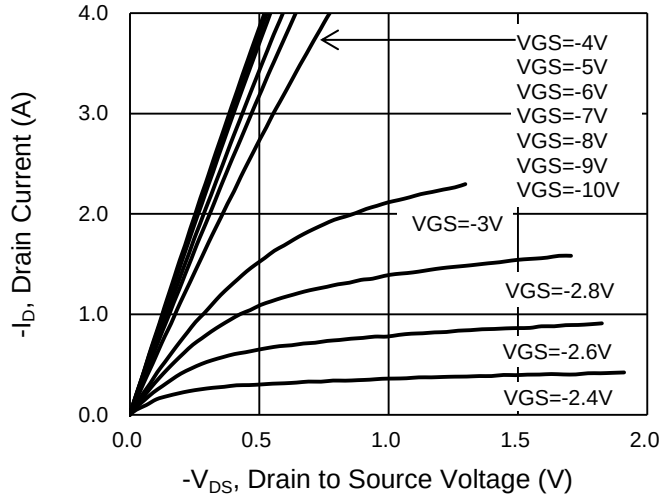
ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TSM2309CX RFG	SOT-23	3kpcs / 7” Reel
TSM2309CX RKG	SOT-23	10kpcs / 13” Reel

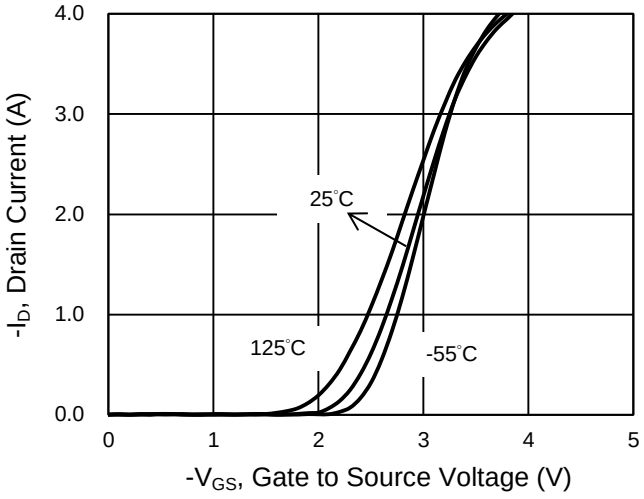
CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

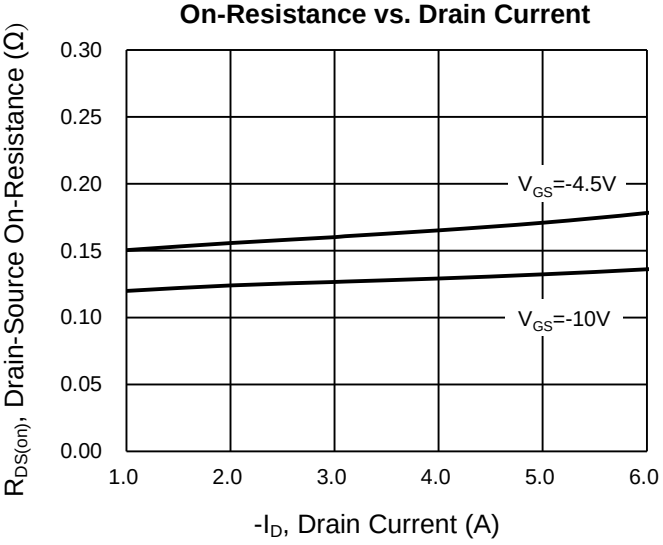
Output Characteristics



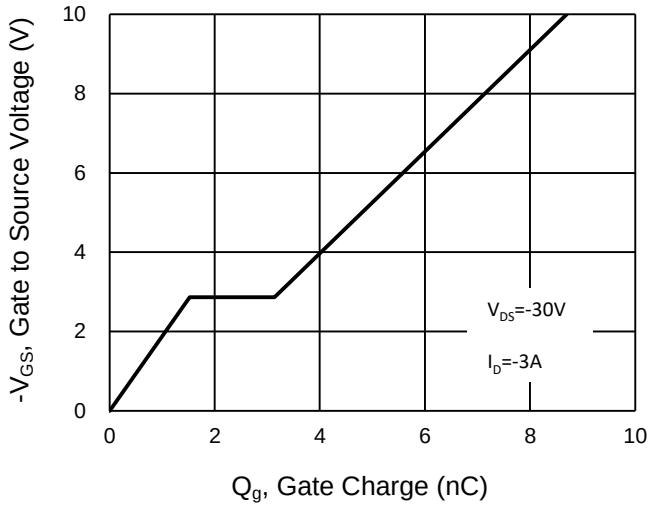
Transfer Characteristics



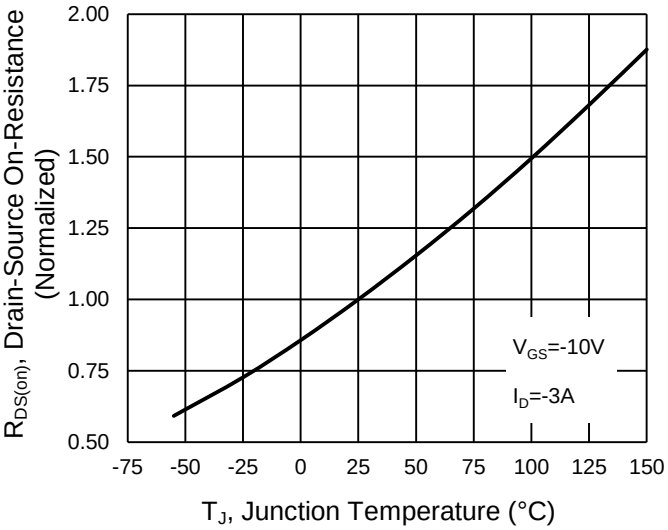
On-Resistance vs. Drain Current



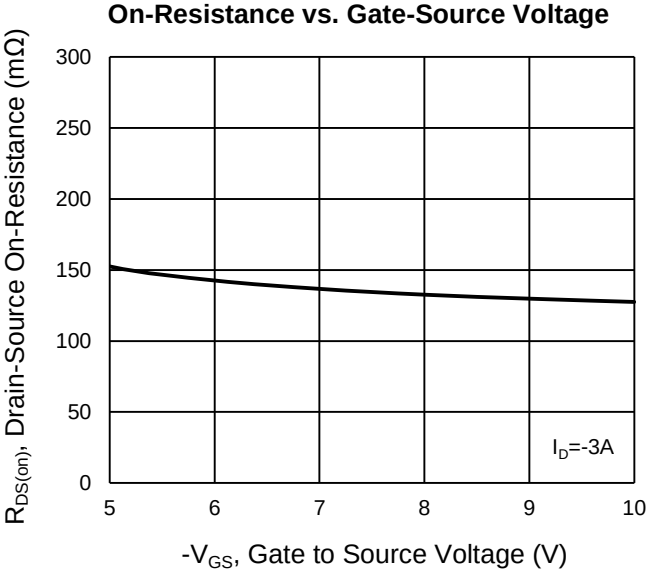
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



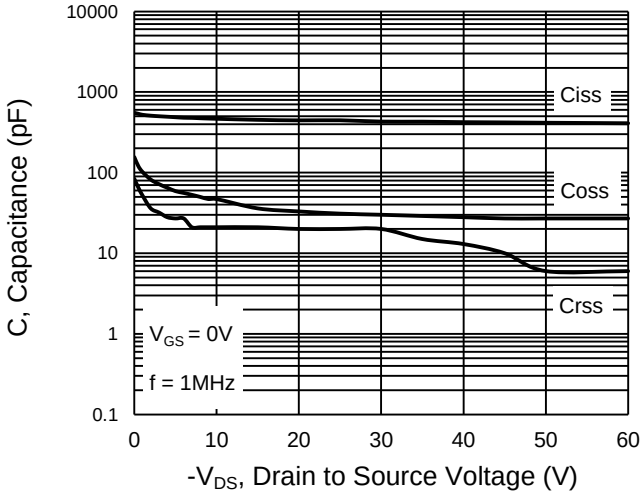
On-Resistance vs. Gate-Source Voltage



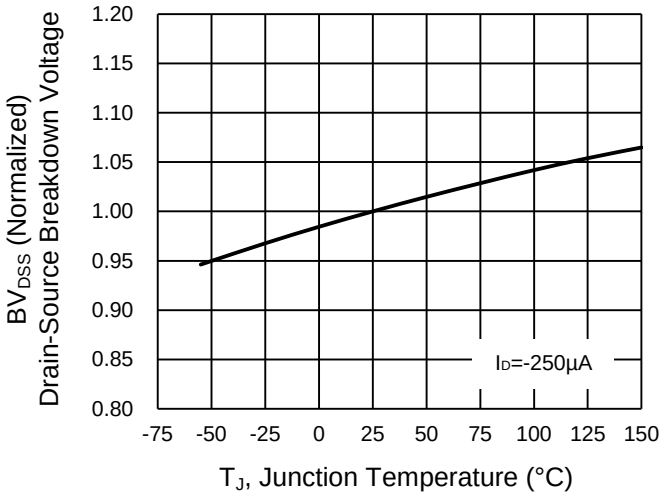
CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

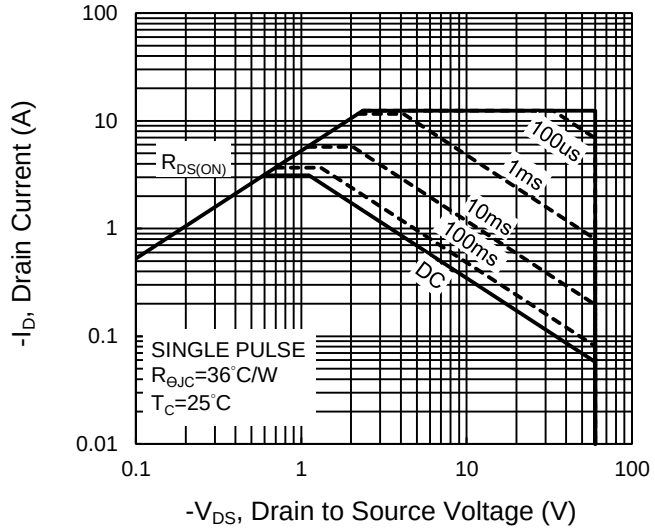
Capacitance vs. Drain-Source Voltage



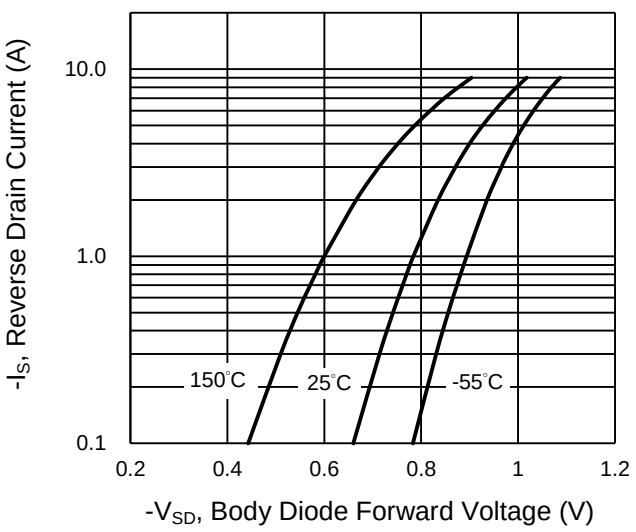
BV_{DSS} vs. Junction Temperature



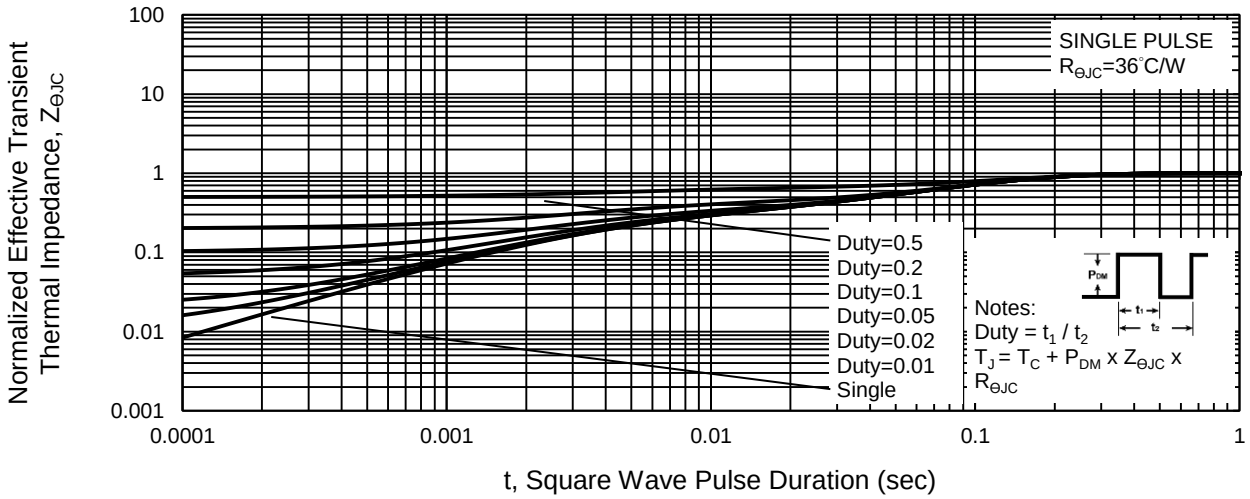
Maximum Safe Operating Area, Junction-to-Case



Source-Drain Diode Forward Current vs. Voltage



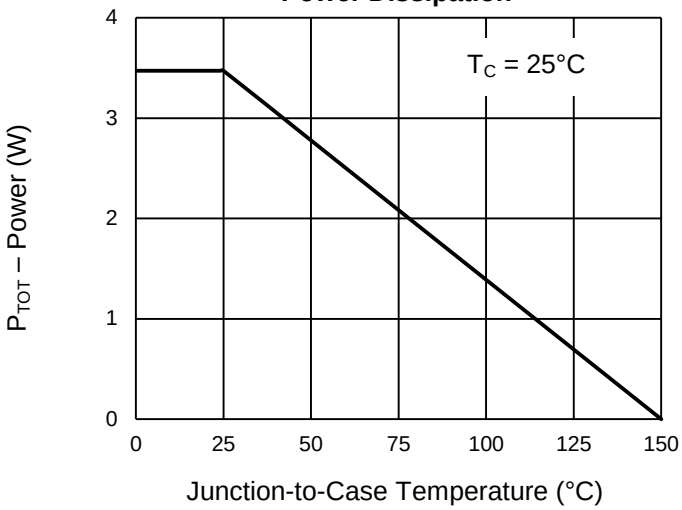
Normalized Thermal Transient Impedance, Junction-to-Case



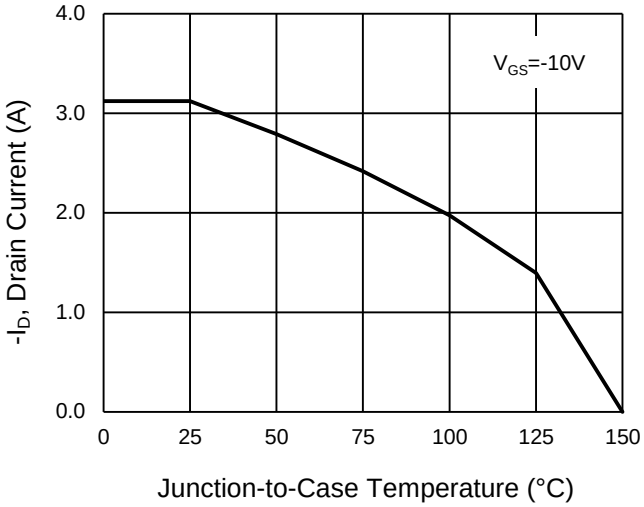
CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

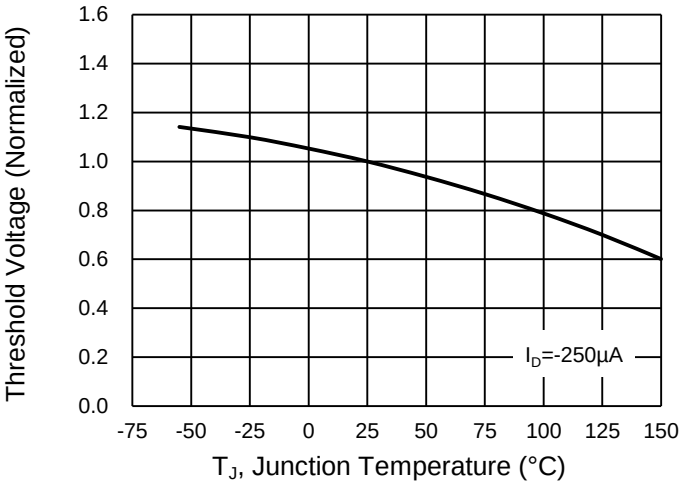
Power Dissipation



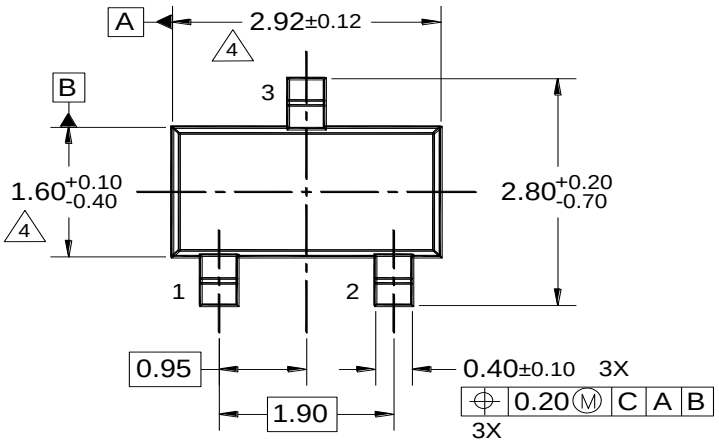
Drain Current

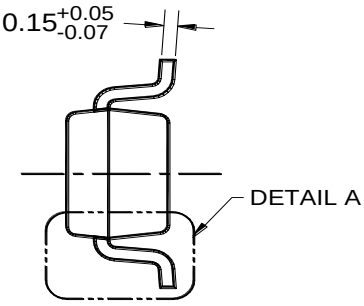


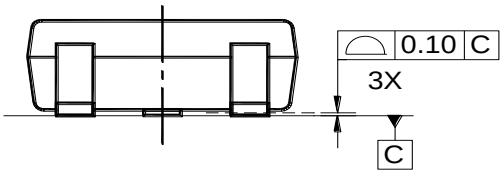
Normalized gate threshold voltage vs Temperature

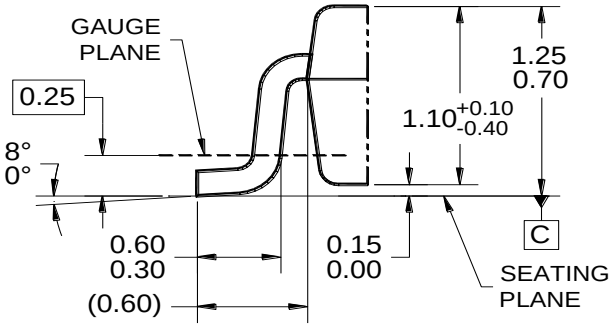


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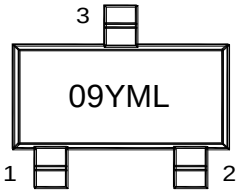


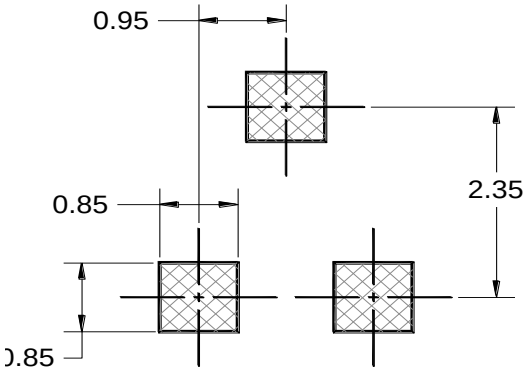






DETAIL A, ROTATED -90°
(SCALE 2:1)





SUGGESTED PAD LAYOUT

09 = Device Code
Y = Year Code
M = Month Code

O	=Jan	**P**	=Feb	**Q**	=Mar	**R**	=Apr
S	=May	**T**	=Jun	**U**	=Jul	**V**	=Aug
W	=Sep	**X**	=Oct	**Y**	=Nov	**Z**	=Dec

L = Lot Code (1~9, A~Z)

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PACKAGE OUTLINE REFERENCE: JEDEC TO-236, ISSUE H, VARIATION AA.
4. MOLDED PLASTIC BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
5. DWG NO REF: HQ2SD07-SOT23-025 REV A.

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