N-Channel Power MOSFET

600V, 2.3A, 4.4Ω

FEATURES

- 100% UIS and Rg tested
- Pb-free plating
- RoHS compliant
- Halogen-free according to IEC 61249-2-21

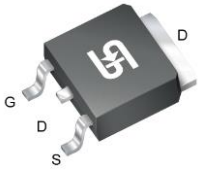
PRODUCT SUMMARY			
PARAMETER		**VALUE**	**UNIT**
V_{DS}		600	V
$R_{DS(on)}$ (max)	V_{GS} = 10V	4.4	Ω
Q_g	V_{GS} = 10V	9.9	nC

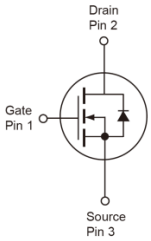
APPLICATIONS

- Lighting
- Charger
- Power Supply
- Switching applications

Pb-Free RoHS COMPLIANT HALOGEN FREE

TO-252 (DPAK)





Note: MSL 3 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)				
PARAMETER		**SYMBOL**	**LIMIT**	**UNIT**
Drain-Source Voltage		V_{DS}	600	V
Gate-Source Voltage		V_{GS}	±30	V
Continuous Drain Current	T_C = 25°C	I_D	2.3	A
	T_C = 100°C		1.5	
	T_A = 25°C		0.4	
Pulsed Drain Current (Note 1)		I_{DM}	9.2	A
Single Pulse Avalanche Current (Note 2)		I_{AS}	3.3	A
Single Pulse Avalanche Energy (Note 2)		E_{AS}	55	mJ
Total Power Dissipation	T_C = 25°C	P_D	62	W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +150	°C

THERMAL RESISTANCE			
PARAMETER	**SYMBOL**	**MAXIMUM**	**UNIT**
Thermal Resistance – Junction to Case	$R_{\Theta JC}$	2	°C/W
Thermal Resistance – Junction to Ambient	$R_{\Theta JA}$	62	°C/W

Note: $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. $R_{\Theta JA}$ is guaranteed by design while $R_{\Theta CA}$ is determined by the user's board design. $R_{\Theta JA}$ shown below for single device operation on FR-4 PCB with minimum recommended footprint in still air.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)						
PARAMETER	**CONDITIONS**	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	BV_{DSS}	600	--	--	V
Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	$V_{GS(TH)}$	2.5	2.9	4.5	V
Gate-Source Leakage Current	V_{GS} = ±30V, V_{DS} = 0V	I_{GSS}	--	--	±100	nA
Drain-Source Leakage Current	V_{GS} = 0V, V_{DS} = 600V	I_{DSS}	--	--	10	μA
Drain-Source On-State Resistance (Note 3)	V_{GS} = 10V, I_D = 1A	$R_{DS(on)}$	--	3.9	4.4	Ω
Forward Transfer Conductance	V_{DS} = 10V, I_D = 1A	g_{fs}	--	2.8	--	S
Dynamic						
Total Gate Charge	V_{GS} = 10V, V_{DS} = 480V, I_D = 2A	Q_g	--	9.9	--	nC
Gate-Source Charge		Q_{gs}	--	1.5	--	
Gate-Drain Charge		Q_{gd}	--	4.7	--	
Input Capacitance	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz	C_{iss}	--	316	--	pF
Output Capacitance		C_{oss}	--	32	--	
Reverse Transfer Capacitance		C_{rss}	--	1	--	
Gate Resistance	f = 1.0MHz	R_g	--	2.8	--	Ω
Switching (Note 4)						
Turn-On Delay Time	V_{GS} = 10V, V_{DS} = 300V, I_D = 2A, R_G = 25Ω	$t_{d(on)}$	--	7.3	--	ns
Rise Time		t_r	--	9.6	--	
Turn-Off Delay Time		$t_{d(off)}$	--	23	--	
Fall Time		t_f	--	18	--	
Source-Drain Diode						
Diode Forward Voltage (Note 3)	V_{GS} = 0V, I_S = 2A	V_{SD}	--	0.8	1.4	V
Source Current	Integral reverse diode In the MOSFET	I_S	--	--	2.3	A
Source Current (Pulse)		I_{SM}	--	--	9.2	

Notes:

1. Pulsed width limited by maximum junction temperature.
2. L = 10mH, V_{GS} = 10V, R_G = 25Ω , Starting T_J = 25°C.
3. Pulse test: Pulse Width ≤ 300μs, duty cycle ≤ 2%.
4. Switching time is essentially independent of operating temperature.

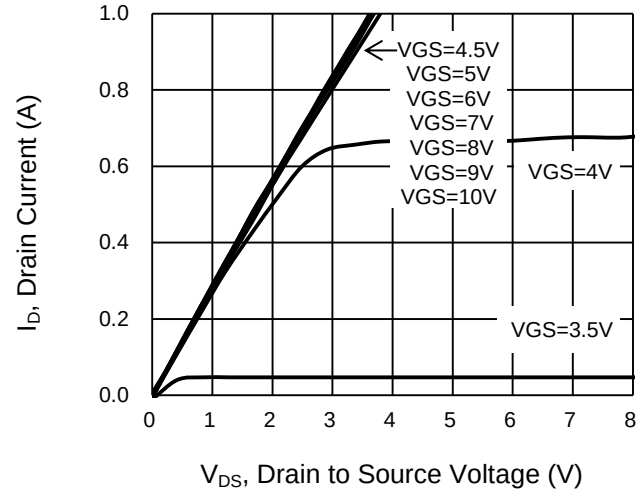
ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TSM2NB60CP ROG	TO-252 (DPAK)	2,500 pcs / 13” Reel

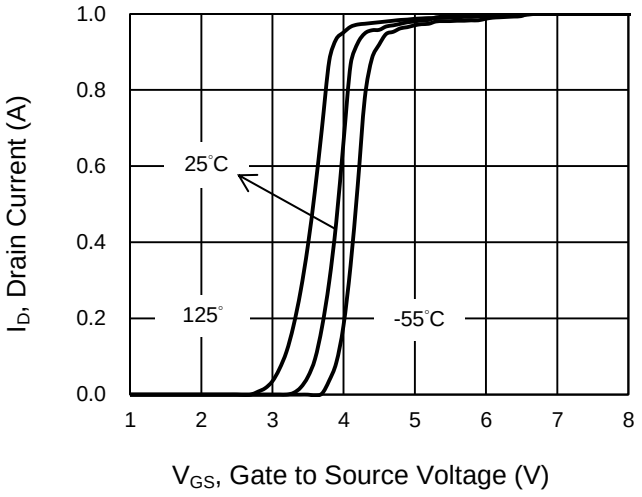
CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

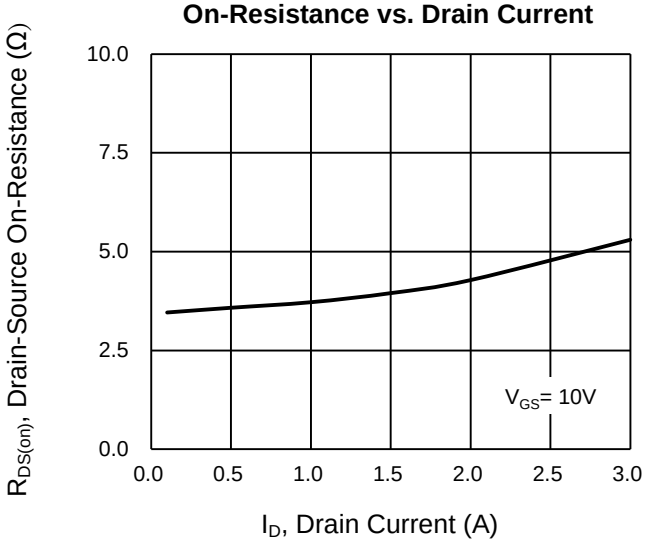
Output Characteristics



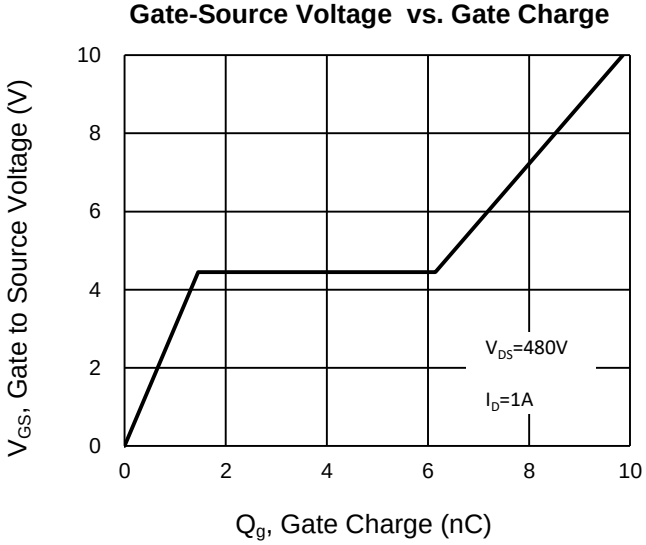
Transfer Characteristics



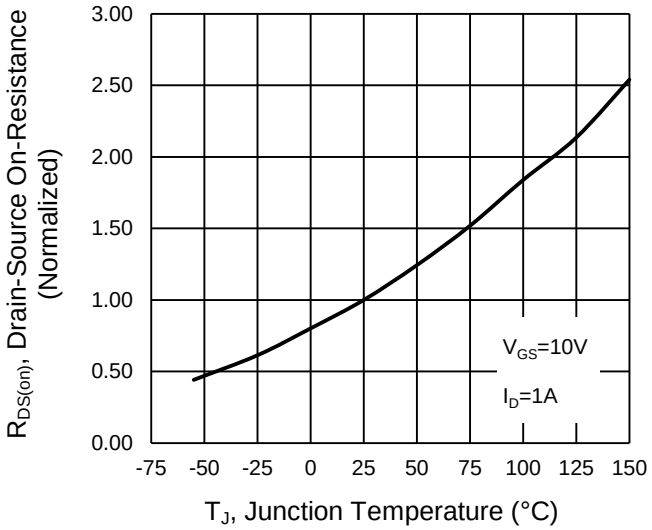
On-Resistance vs. Drain Current



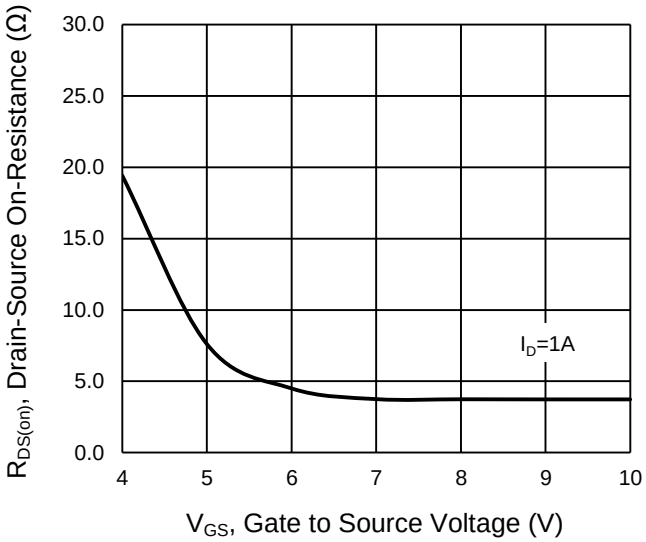
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



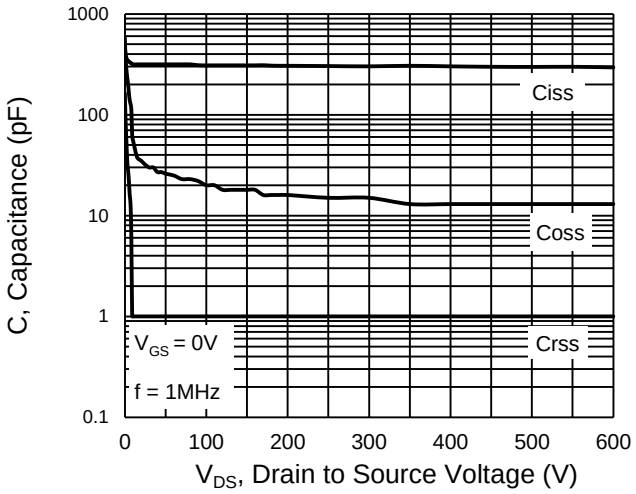
On-Resistance vs. Gate-Source Voltage



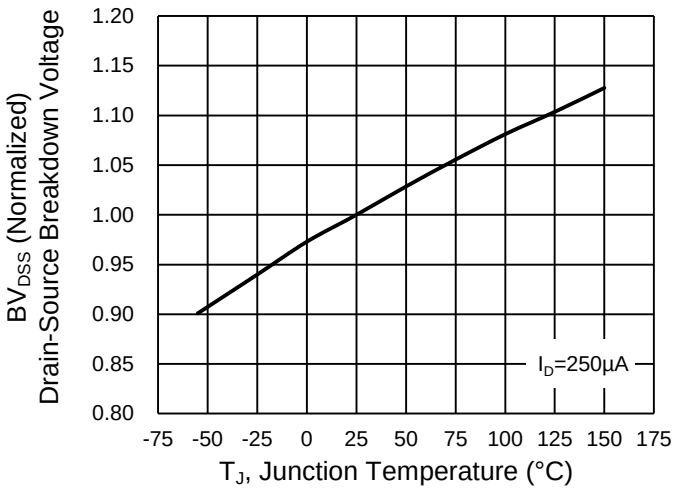
CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

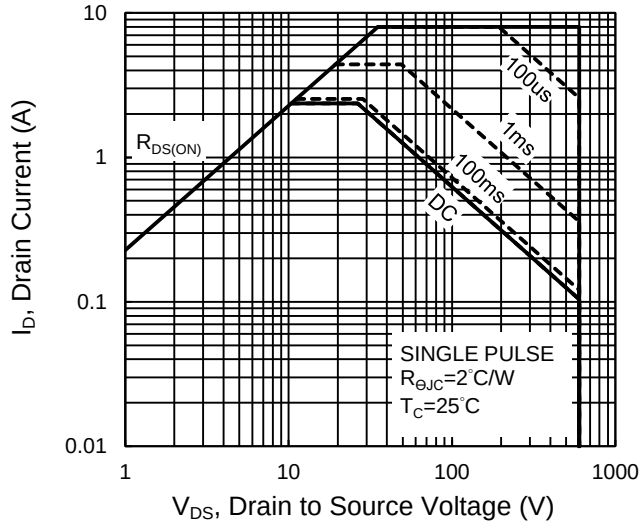
Capacitance vs. Drain-Source Voltage



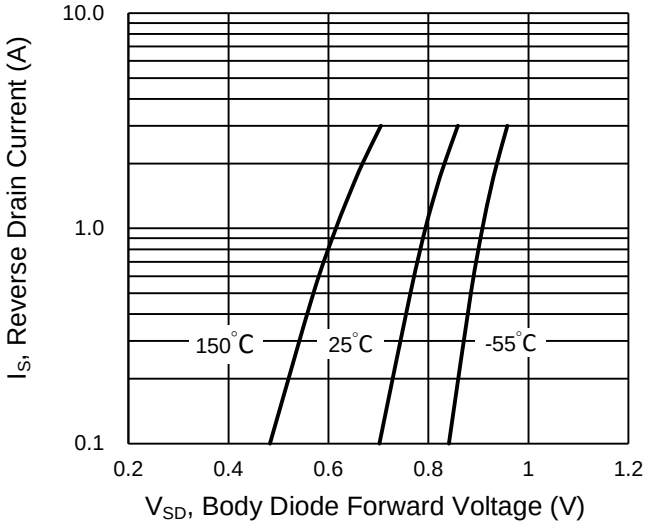
BV_{DSS} vs. Junction Temperature



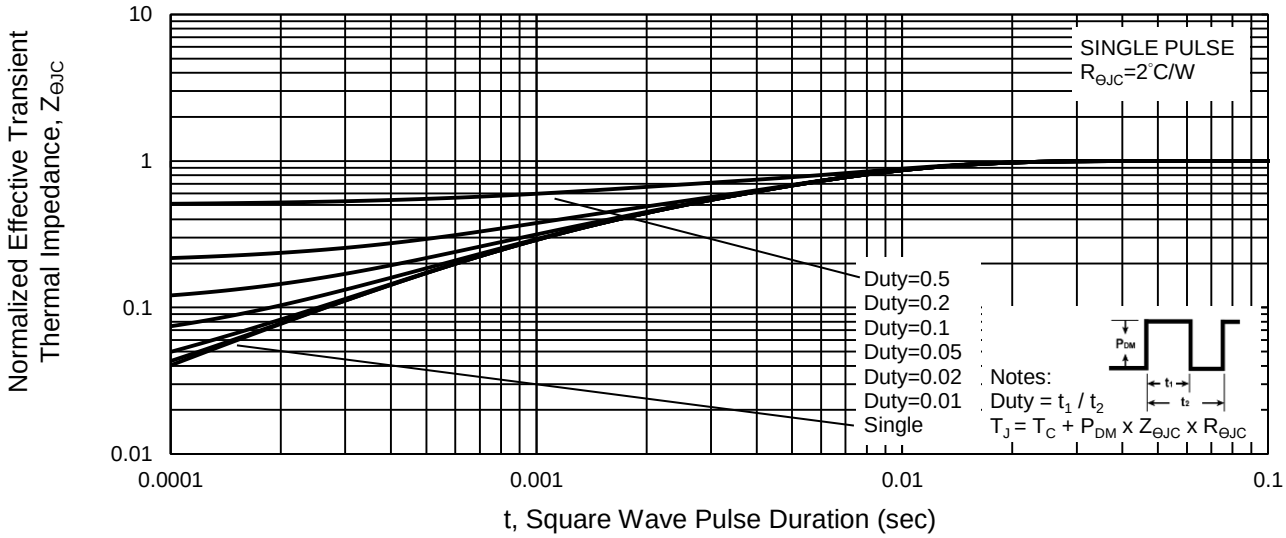
Maximum Safe Operating Area, Junction-to-Case



Source-Drain Diode Forward Current vs. Voltage



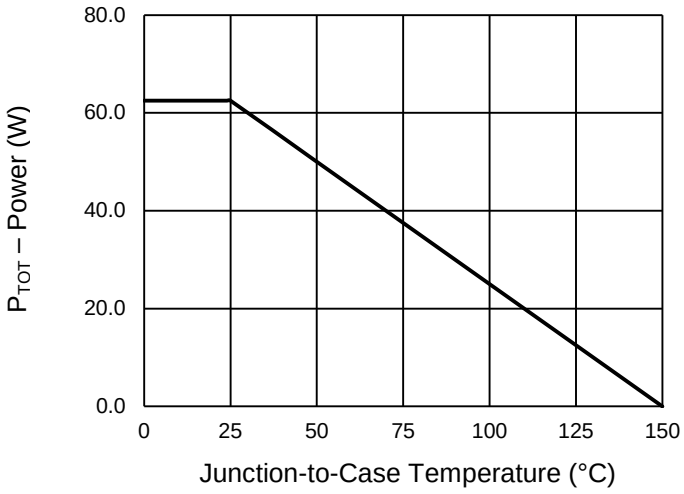
Normalized Thermal Transient Impedance, Junction-to-Case



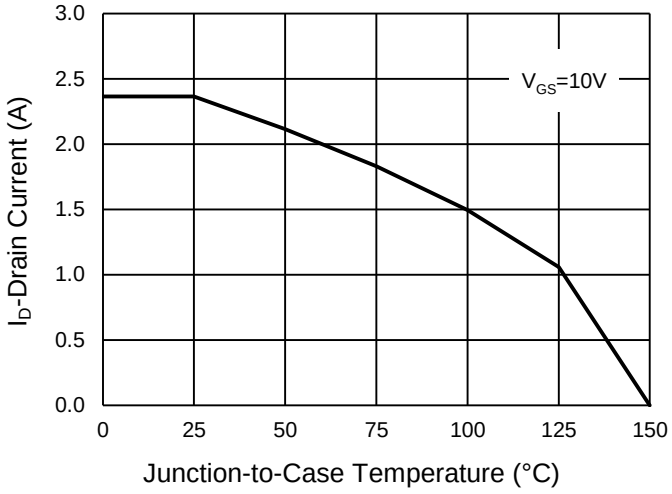
CHARACTERISTICS CURVES

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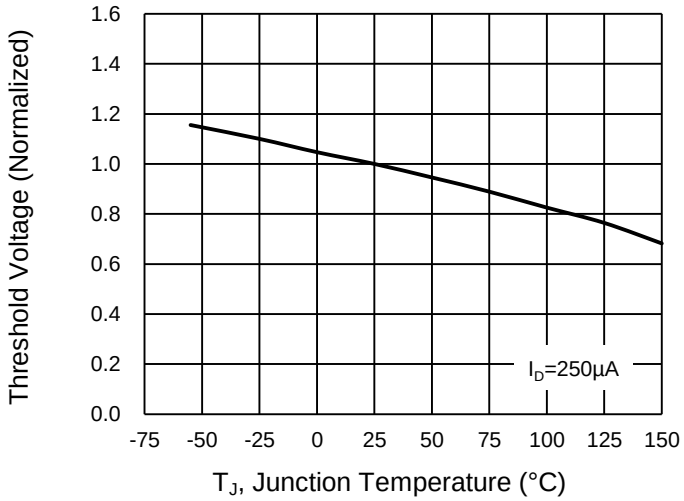
Power Dissipation



Drain Current

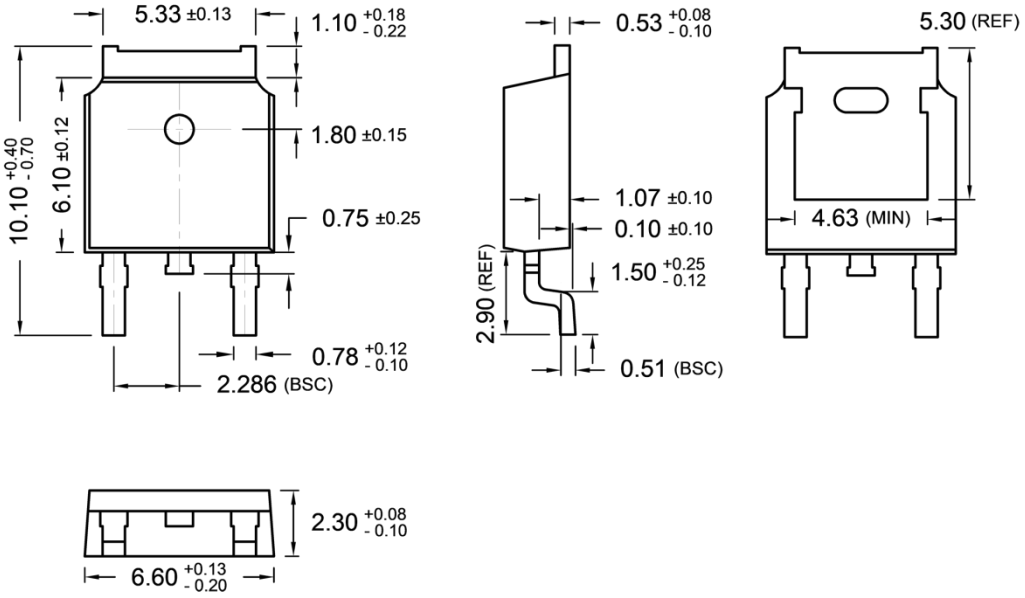


Normalized gate threshold voltage vs Temperature

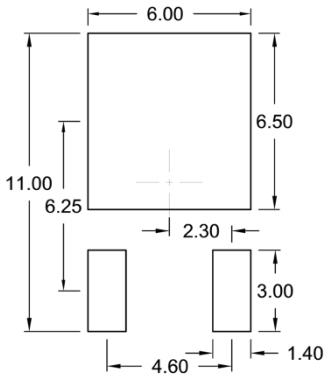


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

TO-252 (DPAK)



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



Y = Year Code

M = Month Code

O	=Jan	**P**	=Feb	**Q**	=Mar	**R**	=Apr
S	=May	**T**	=Jun	**U**	=Jul	**V**	=Aug
W	=Sep	**X**	=Oct	**Y**	=Nov	**Z**	=Dec

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