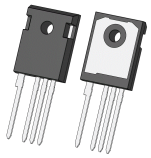
Silicon Carbide (SiC) Cascode JFET – EliteSiC, Power N-Channel, TO247-4, 750 V, 58 mohm

UJ4C075060K4S



TO247-4
CASE 340AN

Description

The UJ4C075060K4S is a 750 V, 58 mΩ G4 SiC FET. It is based on unique 'cascode' circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device's standard gate-drive characteristics allows for a true "drop-in replacement" to Si IGBTs, Si FETs, SiC MOSFETs or Si superjunction devices. Available in the TO247-4 package, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads and any application requiring standard gate drive.

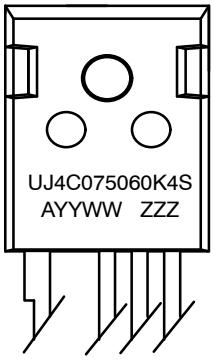
Features

- On-Resistance $R_{DS(on)}$: 58 mΩ (typ)
- Operating Temperature: 175 °C (max)
- Excellent Reverse Recovery: Q_{rr} = 52 nC
- Low Body Diode V_{FSD}: 1.31 V
- Low Gate Charge: Q_G = 37.8 nC
- Threshold Voltage $V_{G(th)}$: 4.8 V (typ) Allowing 0 to 15 V Drive
- Low Intrinsic Capacitance
- ESD Protected: HBM Class 2
- This Device is Pb-Free, Halogen Free and is RoHS Compliant

Typical Applications

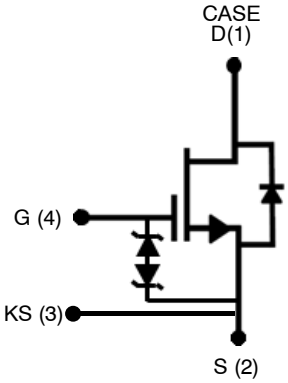
- EV Charging
- PV Inverters
- Switch Mode Power Supplies
- Power Factor Correction Modules
- Motor Drives
- Induction Heating

MARKING DIAGRAM



UJ4C075060K4S	= Specific Device Number
A	= Assembly Location
YY	= Year
WW	= Work Week
ZZZ	= Lot ID

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 10 of this data sheet.

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MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Value	Unit
V_{DS}	Drain-Source Voltage		750	V
V_{GS}	Gate-Source Voltage	DC	−20 to +20	V
		AC (f > 1 Hz)	−25 to +25	V
I_D	Continuous Drain Current (Note 1)	T_C = 25 °C	28	A
		T_C = 100 °C	20.6	A
I_{DM}	Pulsed Drain Current (Note 2)	T_C = 25 °C	62	A
E_{AS}	Single Pulsed Avalanche Energy (Note 3)	L = 15 mH, I_{AS} = 1.8 A	24.3	mJ
P_{tot}	Power Dissipation	T_C = 25 °C	155	W
$T_{J,max}$	Maximum Junction Temperature		175	°C
T_J, T_{STG}	Operating and Storage Temperature		−55 to 175	°C
T_L	Max. Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		250	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Limited by $T_{J,max}$.
2. Pulse width t_p limited by $T_{J,max}$.
3. Starting T_J = 25 °C.

THERMAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case		–	0.75	0.97	°C/W

ELECTRICAL CHARACTERISTICS (T_J = +25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
TYPICAL PERFORMANCE – STATIC							
BV_{DS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 1 mA		750	–	–	V
I_{DSS}	Total Drain Leakage Current	V_{DS} = 750 V, V_{GS} = 0 V, T_J = 25 °C		–	0.7	40	μA
		V_{DS} = 750 V, V_{GS} = 0 V, T_J = 175°C		–	15	–	
I_{GSS}	Total Gate Leakage Current	V_{DS} = 0 V , T_J = 25 °C V_{GS} = −20 V / + 20 V		–	4.7	±20	μA
$R_{DS(on)}$	Drain-Source On-resistance	V_{GS} = 12 V, I_D = 20 A	T_J = 25 °C	–	58	74	mΩ
			T_J = 125 °C	–	106	–	
			T_J = 175 °C	–	147	–	
$V_{G(th)}$	Gate Threshold Voltage	V_{DS} = 5 V, I_D = 10 mA		4	4.8	6	V
R_G	Gate Resistance	f = 1 MHz, open drain		–	4.5	–	Ω
TYPICAL PERFORMANCE – REVERSE DIODE							
I_S	Diode Continuous Forward Current (Note 1)	T_C = 25 °C		–	–	28	A
$I_{S,pulse}$	Diode Pulse Current (Note 2)	T_C = 25 °C		–	–	62	A
V_{FSD}	Forward Voltage	V_{GS} = 0 V, I_S = 10 A, T_J = 25 °C		–	1.31	1.75	V
		V_{GS} = 0 V, I_S = 10 A, T_J = 175 °C		–	1.8	–	
Q_{rr}	Reverse Recovery Charge	V_{DS} = 400 V, I_S = 20 A, V_{GS} = 0 V, R_{G_EXT} = 20 Ω, di/dt = 1060 A/μs, T_J = 25 °C		–	52	–	nC
t_{rr}	Reverse Recovery Time			–	16	–	ns
Q_{rr}	Reverse Recovery Charge	V_{DS} = 400 V, I_S = 20 A, V_{GS} = 0 V, R_{G_EXT} = 20 Ω, di/dt = 1060 A/μs, T_J = 150 °C		–	58	–	nC
t_{rr}	Reverse Recovery Time			–	19	–	ns

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ELECTRICAL CHARACTERISTICS (T_J = +25 °C unless otherwise specified) (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
TYPICAL PERFORMANCE – DYNAMIC						
C_{iss}	Input Capacitance	V_{DS} = 100 V, V_{GS} = 0 V, f = 100 kHz	–	1422	–	pF
C_{oss}	Output Capacitance		–	68	–	
C_{rss}	Reverse Transfer Capacitance		–	2.7	–	
$C_{oss(er)}$	Effective Output Capacitance, Energy Related	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	–	50	–	pF
$C_{oss(tr)}$	Effective Output Capacitance, Time Related		–	94	–	pF
E_{oss}	C_{OSS} Stored Energy	V_{DS} = 400 V, V_{GS} = 0 V	–	4	–	μJ
Q_G	Total Gate Charge	V_{DS} = 400 V, I_D = 20 A, V_{GS} = 0 V to 15 V	–	37.8	–	nC
Q_{GD}	Gate-Drain Charge		–	8	–	
Q_{GS}	Gate-Source Charge		–	11.8	–	
$t_{d(on)}$	Turn-on Delay Time	Notes 4 V_{DS} = 400 V, I_D = 20 A, Gate Driver = 0 V, to +15 V, Turn-on $R_{G,EXT}$ = 1 Ω, Turn-off $R_{G,EXT}$ = 20 Ω, Inductive Load, FWD: same device with V_{GS} = 0 V and R_G = 20 Ω, T_J = 25 °C	–	12	–	ns
t_r	Rise Time		–	19	–	
$t_{d(off)}$	Turn-off Delay Time		–	78	–	
t_f	Fall Time		–	12	–	
E_{ON}	Turn-on Energy		–	126	–	μJ
E_{OFF}	Turn-off Energy		–	37	–	
E_{TOTAL}	Total Switching Energy		–	163	–	
$t_{d(on)}$	Turn-on Delay Time	Notes 4 V_{DS} = 400 V, I_D = 20 A, Gate Driver = 0 V, to +15 V, Turn-on $R_{G,EXT}$ = 1 Ω, Turn-off $R_{G,EXT}$ = 20 Ω, Inductive Load, FWD: same device with V_{GS} = 0 V and R_G = 20 Ω, T_J = 150 °C	–	12	–	ns
t_r	Rise Time		–	21	–	
$t_{d(off)}$	Turn-off Delay Time		–	83	–	
t_f	Fall Time		–	14	–	
E_{ON}	Turn-on Energy		–	151	–	μJ
E_{OFF}	Turn-off Energy		–	50	–	
E_{TOTAL}	Total Switching Energy		–	201	–	
$t_{d(on)}$	Turn-on Delay Time	Notes 5 V_{DS} = 400 V, I_D = 20 A, Gate Driver = 0 V, to +15 V, $R_{G,EXT}$ = 1 Ω, Inductive Load, FWD: same device with V_{GS} = 0 V and R_G = 1 Ω, RC snubber: R_{S1} = 10 Ω and C_{S1} = 95 pF, T_J = 25 °C	–	12	–	ns
t_r	Rise Time		–	22	–	
$t_{d(off)}$	Turn-off Delay Time		–	31	–	
t_f	Fall Time		–	9	–	
E_{ON}	Turn-on Energy Including R_S Energy		–	142	–	μJ
E_{OFF}	Turn-off Energy Including R_S Energy		–	17	–	
E_{TOTAL}	Total Switching Energy		–	159	–	
E_{RS_ON}	Snubber R_S Energy During Turn-on		–	0.7	–	
E_{RS_OFF}	Snubber R_S Energy During Turn-off		–	1	–	
$t_{d(on)}$	Turn-on Delay Time	Notes 5 V_{DS} = 400 V, I_D = 20 A, Gate Driver = 0 V, to +15 V, $R_{G,EXT}$ = 1 Ω, Inductive Load, FWD: same device with V_{GS} = 0 V and R_G = 1 Ω, RC snubber: R_{S1} = 10 Ω and C_{S1} = 95 pF, T_J = 150 °C	–	12	–	ns
t_r	Rise Time		–	25	–	
$t_{d(off)}$	Turn-off Delay Time		–	35	–	
t_f	Fall Time		–	9	–	
E_{ON}	Turn-on Energy Including R_S Energy		–	153	–	μJ
E_{OFF}	Turn-off Energy Including R_S Energy		–	18	–	
E_{TOTAL}	Total Switching Energy		–	171	–	
E_{RS_ON}	Snubber R_S Energy During Turn-on		–	0.7	–	
E_{RS_OFF}	Snubber R_S Energy During Turn-off		–	1	–	

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ELECTRICAL CHARACTERISTICS (T_J = +25 °C unless otherwise specified) (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
TYPICAL PERFORMANCE – DYNAMIC						
$t_{d(on)}$	Turn-on Delay Time	Notes 6 V_{DS} = 400 V, I_D = 20 A, Gate Driver = 0 V, to +15 V, Turn-on $R_{G,EXT}$ = 1 Ω, Turn-off $R_{G,EXT}$ = 20 Ω, Inductive Load, FWD: UJ3D06510TS T_J = 25 °C	–	12	–	ns
t_r	Rise Time		–	18	–	
$t_{d(off)}$	Turn-off Delay Time		–	78	–	
t_f	Fall Time		–	12	–	
E_{ON}	Turn-on Energy		–	90	–	μJ
E_{OFF}	Turn-off Energy		–	37	–	
E_{TOTAL}	Total Switching Energy		–	127	–	
$t_{d(on)}$	Turn-on Delay Time	Notes 6 V_{DS} = 400 V, I_D = 20 A, Gate Driver = 0 V, to +15 V, Turn-on $R_{G,EXT}$ = 1 Ω, Turn-off $R_{G,EXT}$ = 20 Ω, Inductive Load, FWD: UJ3D06510TS T_J = 150 °C	–	12	–	ns
t_r	Rise Time		–	19	–	
$t_{d(off)}$	Turn-off Delay Time		–	84	–	
t_f	Fall Time		–	15	–	
E_{ON}	Turn-on Energy		–	104	–	μJ
E_{OFF}	Turn-off		–	49	–	
E_{TOTAL}	Total Switching Energy		–	153	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Measured with the half−bridge mode switching test circuit in Figure 29.
5. Measured with the half−bridge mode switching test circuit in Figure 31.
6. Measured with the chopper mode switching test circuit in Figure 30.

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TYPICAL PERFORMANCE DIAGRAMS

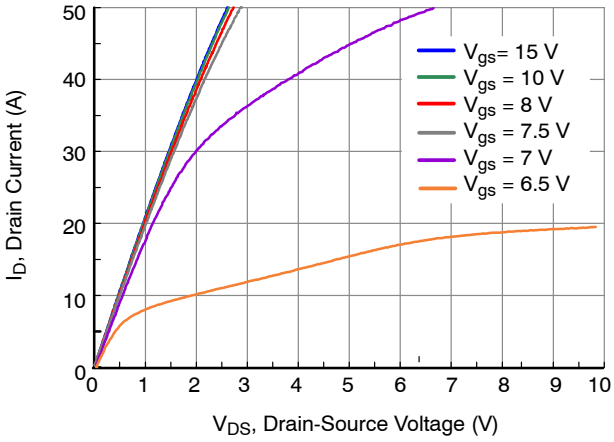


Figure 1. Typical Output Characteristics at T_J = −55 °C, t_p < 250 μs

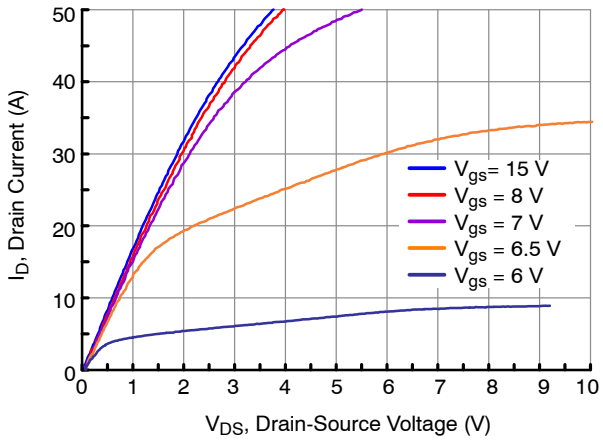


Figure 2. Typical Output Characteristics at T_J = 25 °C, t_p < 250 μs

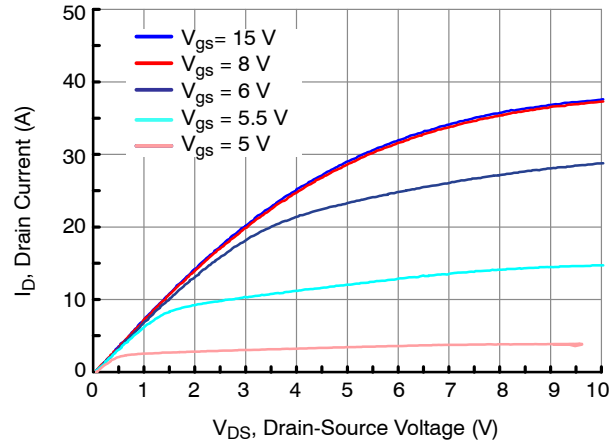


Figure 3. Typical Output Characteristics at T_J = 175 °C, t_p < 250 μs

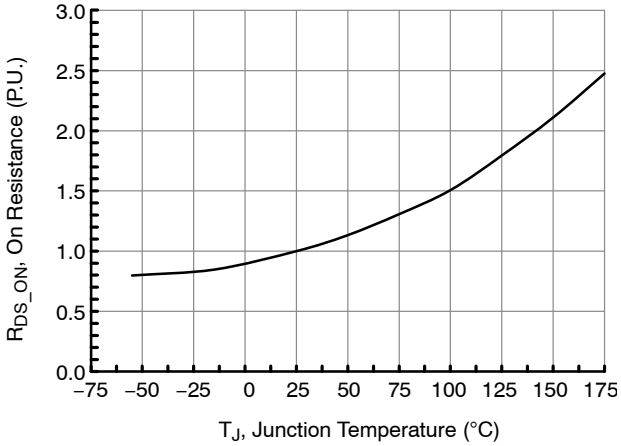


Figure 4. Normalized On-Resistance vs. Temperature at V_{GS} = 12 V and I_D = 20 A

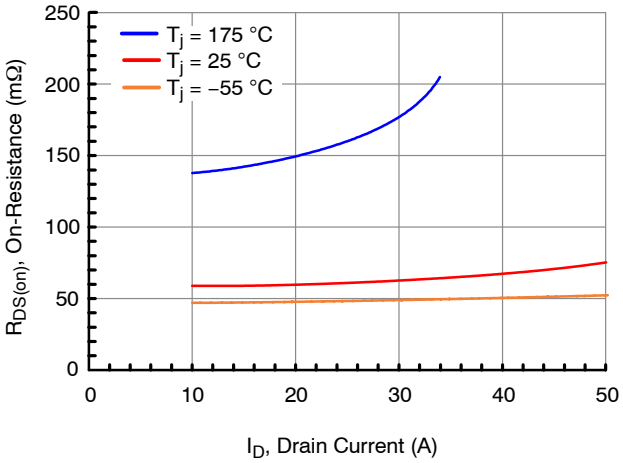


Figure 5. Typical Drain-Source On-Resistances at V_{GS} = 12 V

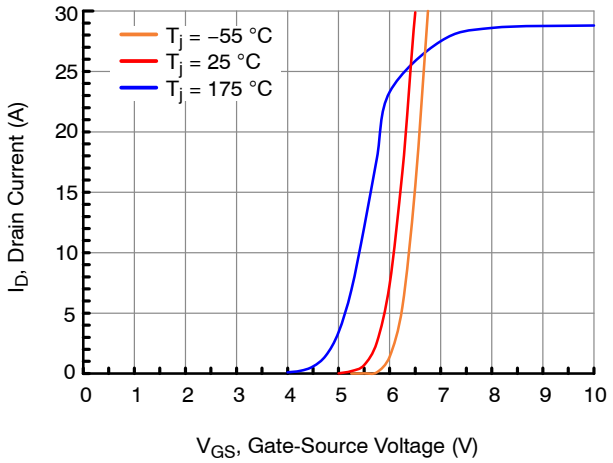


Figure 6. Typical Transfer Characteristics at V_{DS} = 5 V

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TYPICAL PERFORMANCE DIAGRAMS (continued)

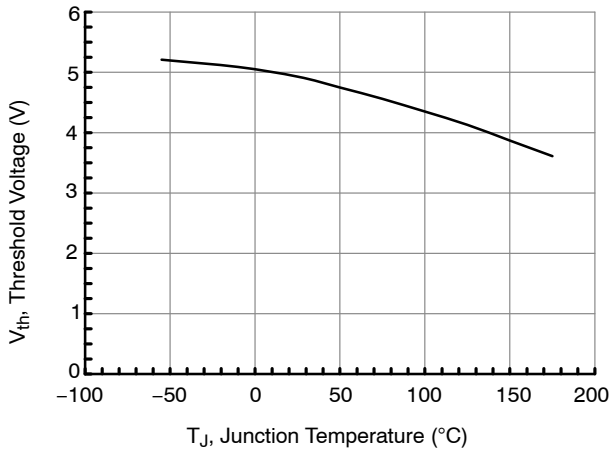


Figure 7. Threshold Voltage vs. Junction Temperature at V_{DS} = 5 V and I_D = 10 mA

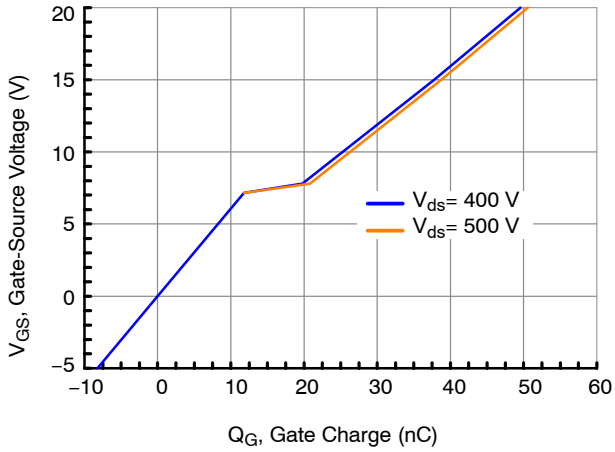


Figure 8. Typical Gate Charge at I_D = 20 A

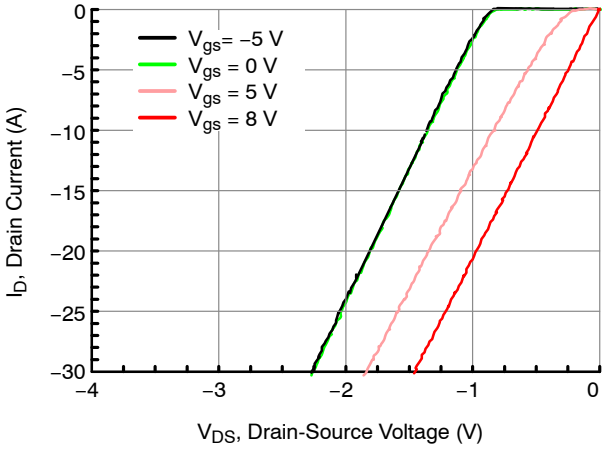


Figure 9. 3rd Quadrant Characteristics at T_J = −55 °C

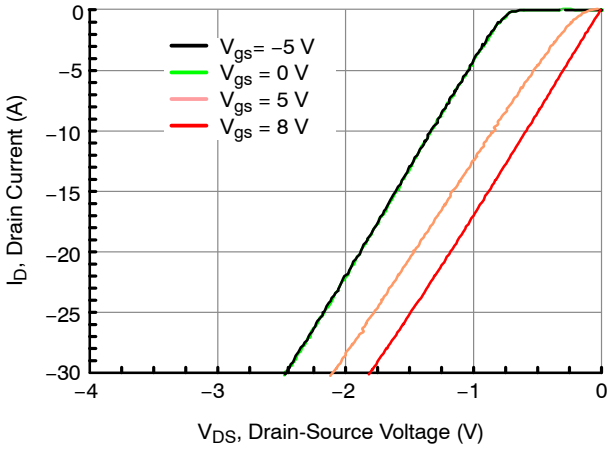


Figure 10. 3rd Quadrant Characteristics at T_J = 25 °C

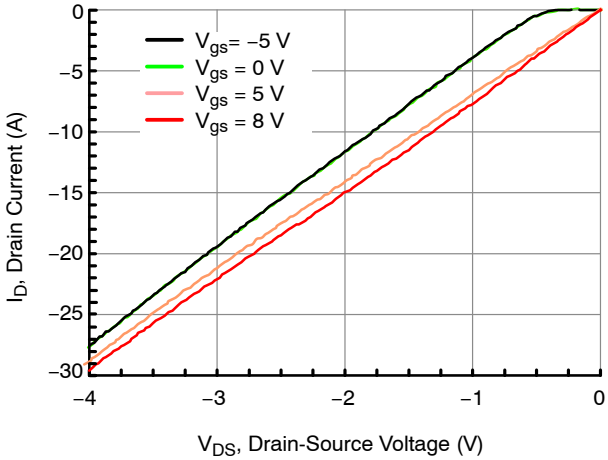


Figure 11. 3rd Quadrant Characteristics at T_J = 175 °C

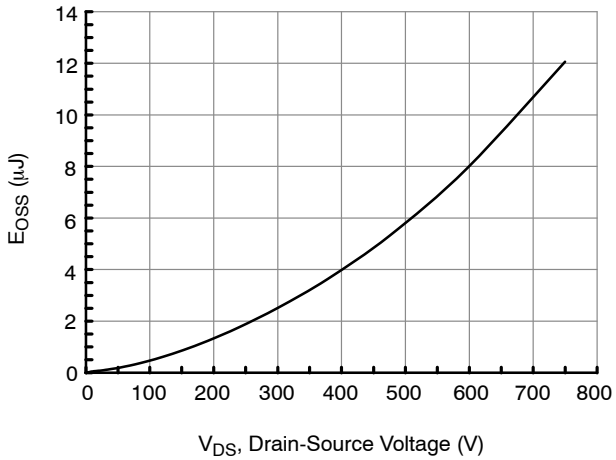


Figure 12. Typical Stored Energy in C_{OSS} at V_{GS} = 0 V

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TYPICAL PERFORMANCE DIAGRAMS (continued)

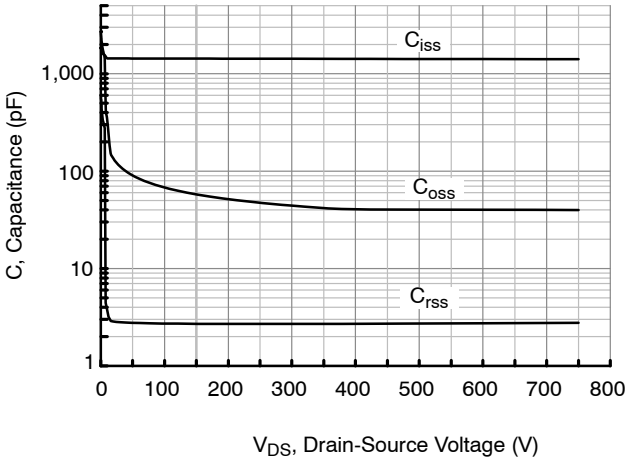


Figure 13. Typical Capacitances at f = 100 kHz and V_{GS} = 0 V

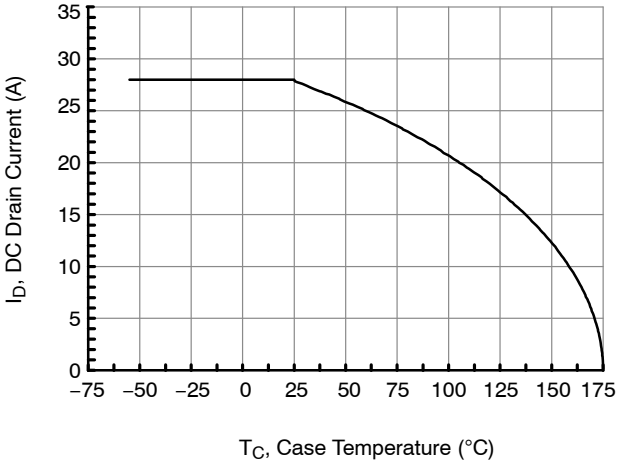


Figure 14. DC Drain Current Derating

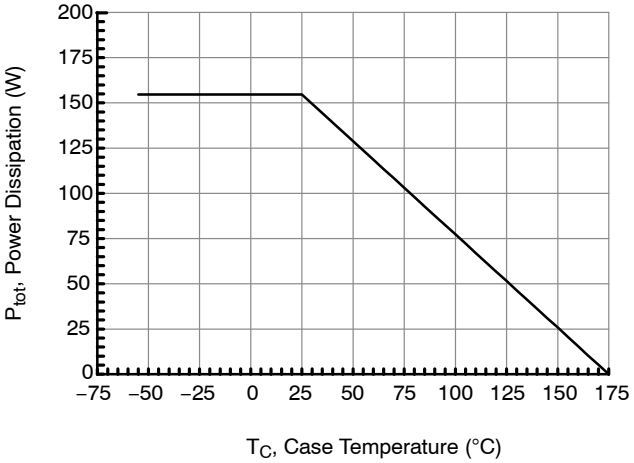


Figure 15. Total Power Dissipation

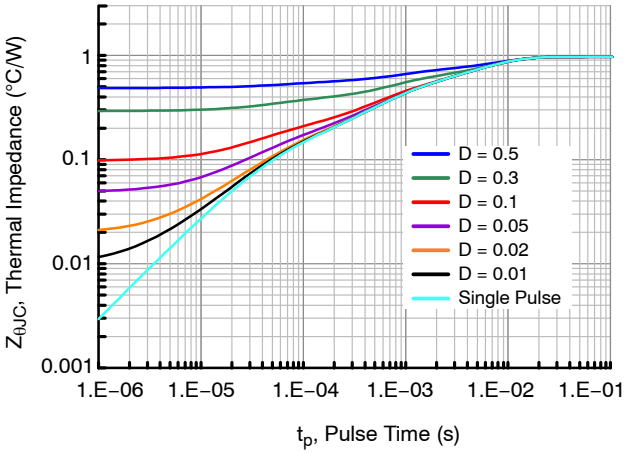


Figure 16. Maximum Transient Thermal Impedance

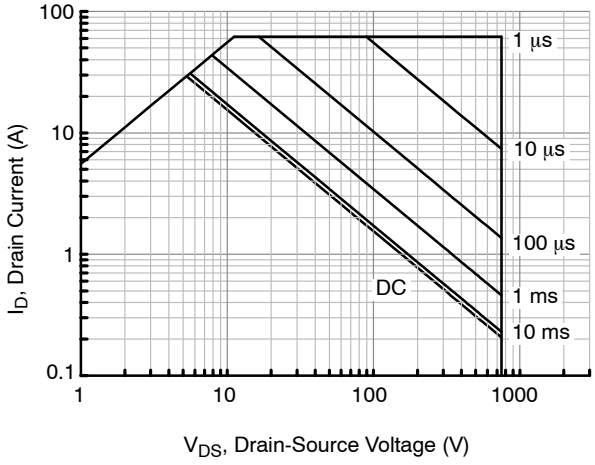


Figure 17. Safe Operation Area at T_C = 25 °C, D = 0, Parameter t_p

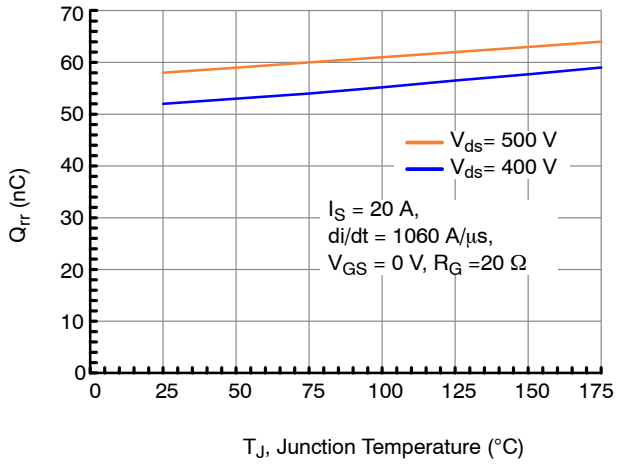


Figure 18. Reverse Recovery Charge Q_{rr} vs. Junction Temperature

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TYPICAL PERFORMANCE DIAGRAMS (continued)

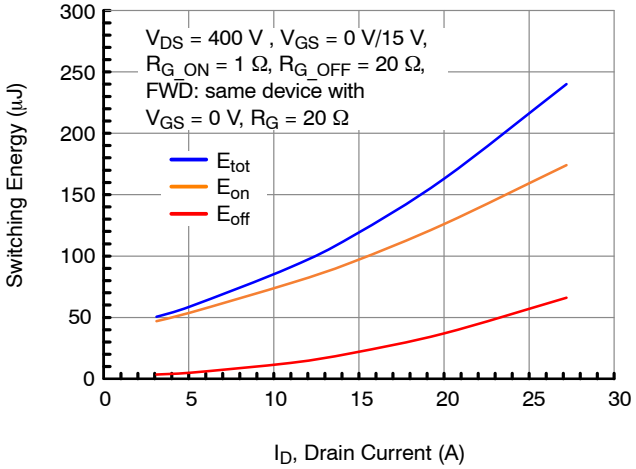


Figure 19. Clamped Inductive Switching Energy vs. Drain Current at V_{DS} = 400 V and T_J = 25 °C

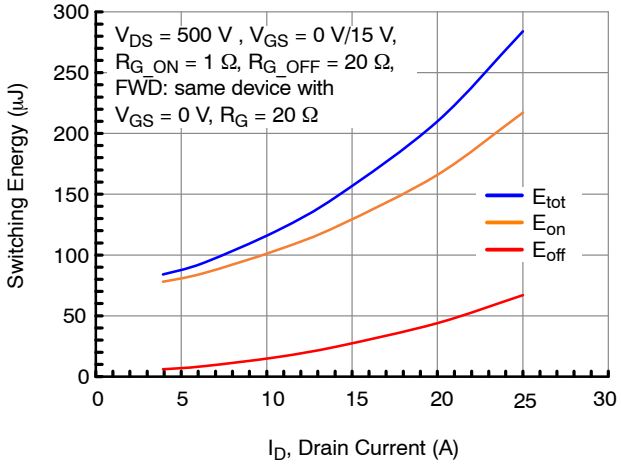


Figure 20. Clamped Inductive Switching Energy vs.Drain Current at V_{DS} = 500 V, and T_J = 25 °C

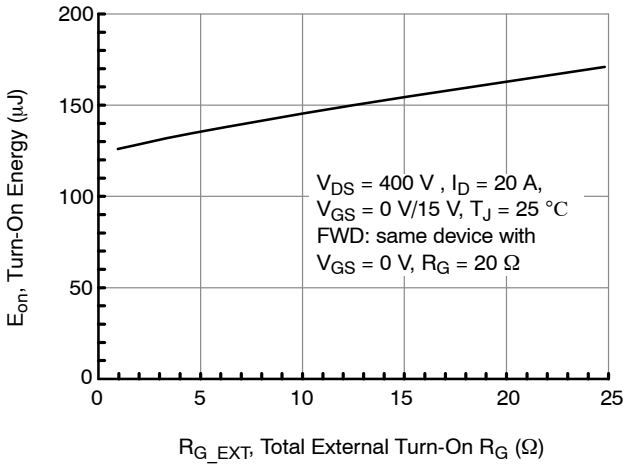


Figure 21. Clamped Inductive Switching Turn-On Energy vs. R_{G,EXT_ON}

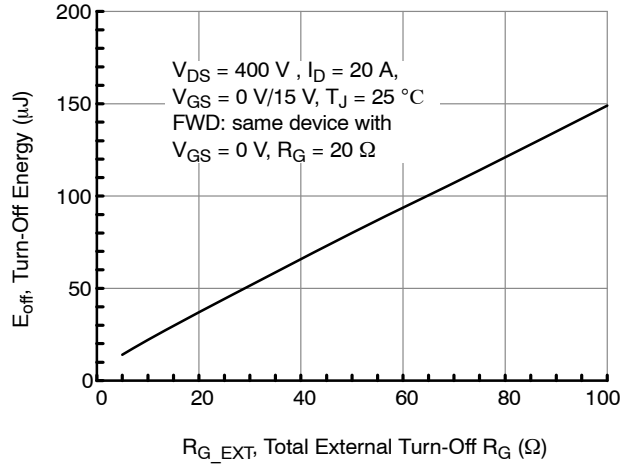


Figure 22. Clamped Inductive Switching Turn-Off Energy vs. R_{G,EXT_OFF}

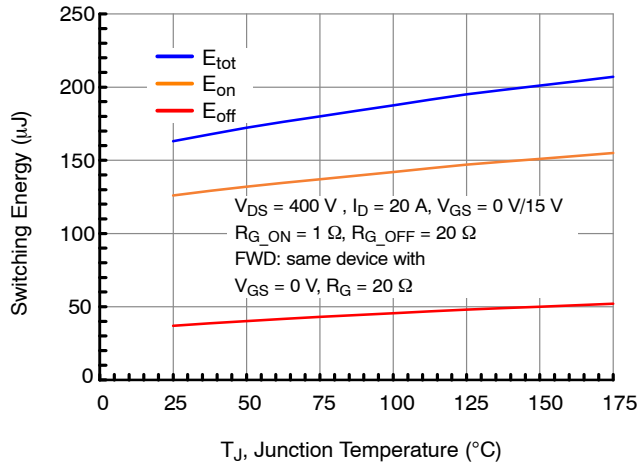


Figure 23. Clamped Inductive Switching Energy vs. JunctionTemperature at V_{DS} = 400 V, and I_D = 20 A

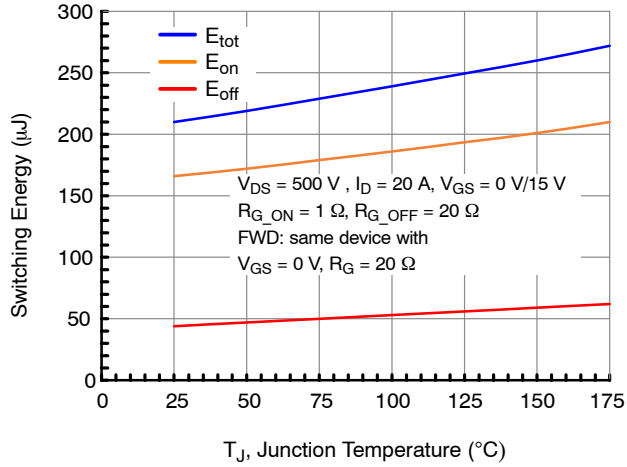


Figure 24. Clamped Inductive Switching Energy vs. JunctionTemperature at V_{DS} = 500 V, and I_D = 20 A

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TYPICAL PERFORMANCE DIAGRAMS (continued)

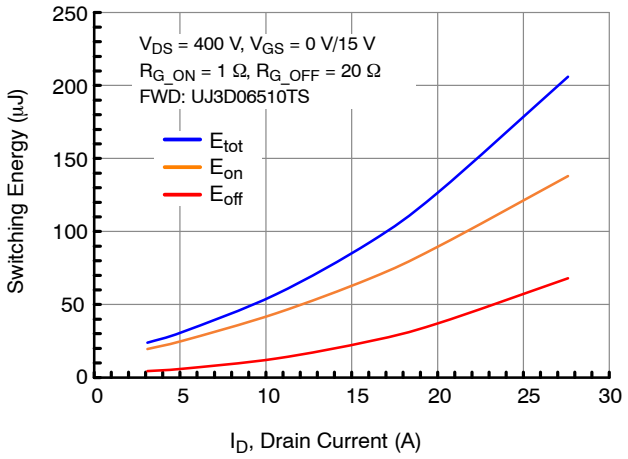


Figure 25. Clamped Inductive Switching Energy vs. Drain Current at V_{DS} = 400 V and T_J = 25 °C

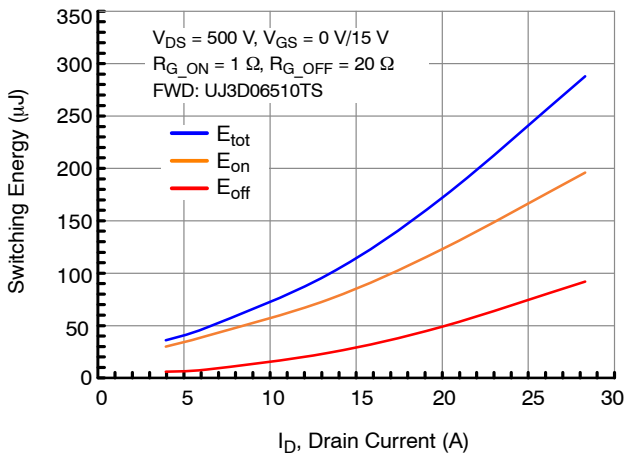


Figure 26. Clamped Inductive Switching Energy vs. Drain Current at V_{DS} = 500 V and T_J = 25 °C

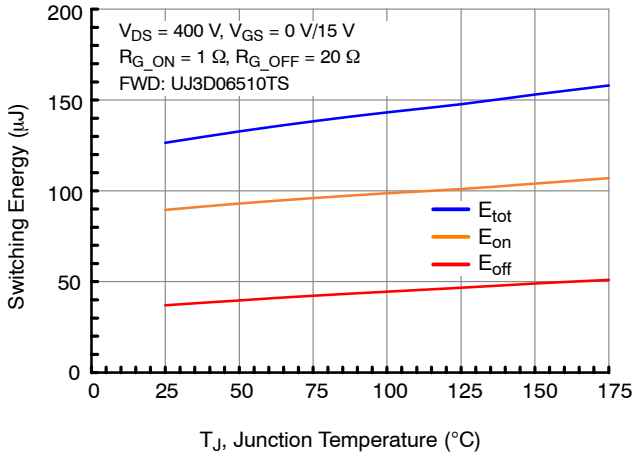


Figure 27. Clamped Inductive Switching Energy vs. Junction Temperature at V_{DS} = 400 V and I_D = 20 A

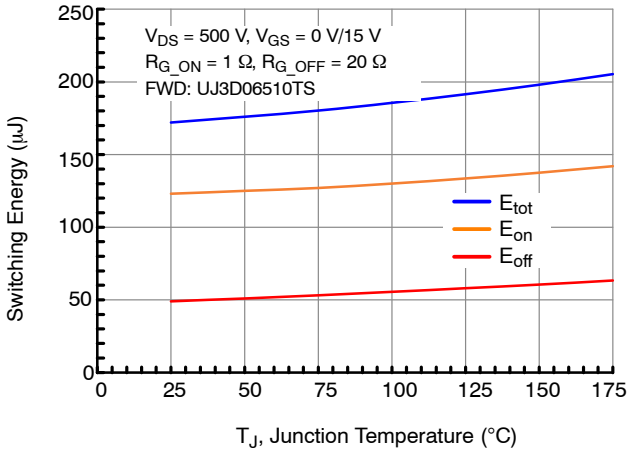


Figure 28. Clamped Inductive Switching Energy vs. Junction Temperature at V_{DS} = 500 V, I_D = 20 A

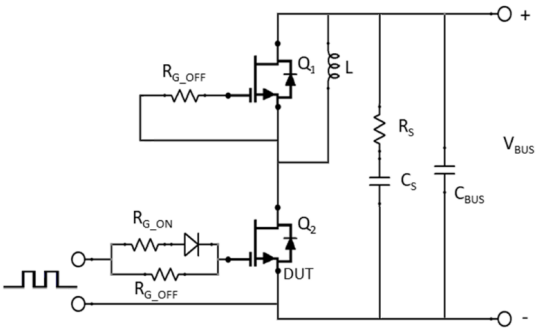


Figure 29. Schematic of the Half-Bridge Mode Switching Test Circuit. Note, a Bus RC Snubber (R_S = 2.5 Ω, C_S = 100 nF) is Used to Reduce the Power Loop High Frequency Oscillations.

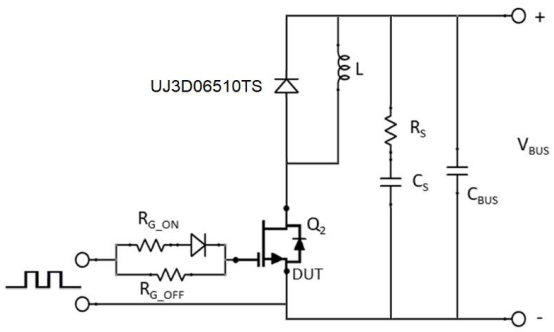


Figure 30. Schematic of the Chopper Mode Switching Test Circuit. Note, a Bus RC Snubber (R_S = 2.5 Ω, C_S = 100 nF) is Used to Reduce the Power Loop High Frequency Oscillations.

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TYPICAL PERFORMANCE DIAGRAMS (continued)

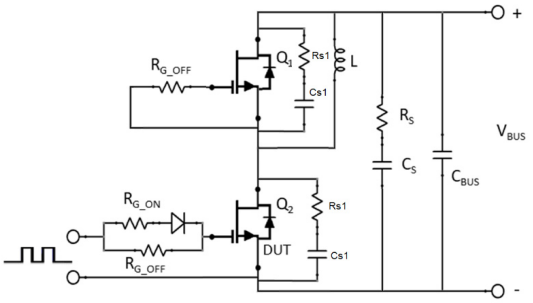


Figure 31. Schematic of the Half-Bridge Mode Switching Test Circuit with device RC Snubber (R_{S1} = 10 Ω, C_{S1} = 95 nF) and a Bus RC Snubber (R_S = 2.5 Ω, C_S = 100 nF).

APPLICATIONS INFORMATION

SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (C_{oss}), gate charge (Q_G), and reverse recovery charge (Q_{rr}) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

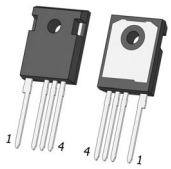
Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see www.onsemi.com.

A snubber circuit with a small $R_{(G)}$, or gate resistor, provides better EMI suppression with higher efficiency compared to using a high $R_{(G)}$ value. There is no extra gate delay time when using the snubber circuitry, and a small $R_{(G)}$ will better control both the turn-off $V_{(DS)}$ peak spike and ringing duration, while a high $R_{(G)}$ will damp the peak spike but result in a longer delay time. In addition, the total switching loss when using a snubber circuit is less than using high $R_{(G)}$, while greatly reducing $E_{(OFF)}$ from mid-to-full load range with only a small increase in $E_{(ON)}$. Efficiency will therefore improve with higher load current. For more information on how a snubber circuit will improve overall system performance, visit the **onsemi** website at www.onsemi.com.

ORDERING INFORMATION

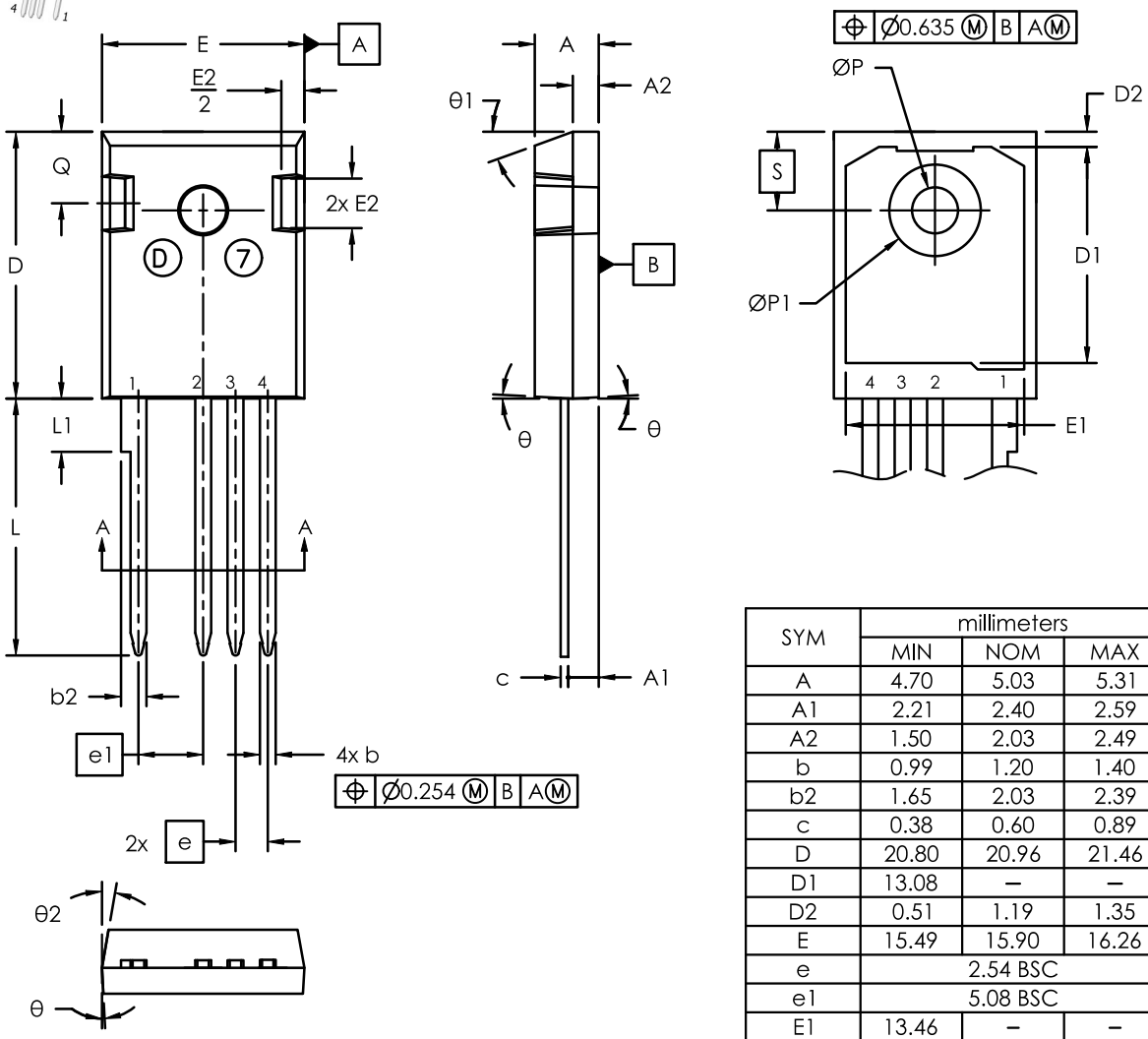
Part Number	Marking	Package	Shipping
UJ4C075060K4S	UJ4C075060K4S	TO247-4 (Pb-Free, Halogen Free)	600 Units / Tube

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TO247−4 15.90x20.96x5.03, 5.44P
CASE 340AN
ISSUE E

DATE 20 JUN 2025



SYM	millimeters		
	MIN	NOM	MAX
A	4.70	5.03	5.31
A1	2.21	2.40	2.59
A2	1.50	2.03	2.49
b	0.99	1.20	1.40
b2	1.65	2.03	2.39
c	0.38	0.60	0.89
D	20.80	20.96	21.46
D1	13.08	–	–
D2	0.51	1.19	1.35
E	15.49	15.90	16.26
e	2.54 BSC		
e1	5.08 BSC		
E1	13.46	–	–
E2	3.43	3.89	5.20
L	19.81	20.17	20.32
L1	–	–	4.50
ØP	3.40	3.60	3.80
ØP1	7.06	7.19	7.39
Q	5.38	5.62	6.20
S	6.17 BSC		
θ	3°		
θ1	20°		
θ2	10°		

NOTE:
1. Dimensioning and tolerancing as per ASME Y14.5 - 2018
2. Controlling dimension : millimeters
3. Package Outline in compliance with JEDEC standard var. AD.
4. Dimensions D & E does not include mold flash.
5. ØP to have max draft angle of 1.7° to the top with max. hole diameter of 3.91mm.
5. Through Hole diameter value = End Hole diameter
6. PCB Through Hole pattern as per IPC-2221/IPC-2222

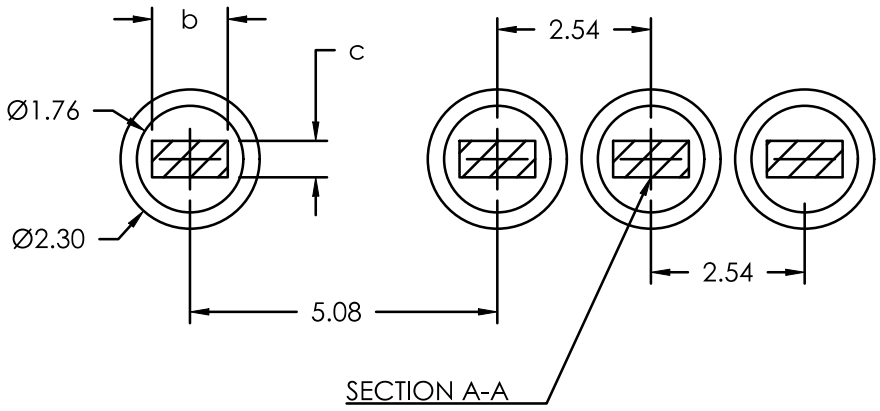
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RECOMMENDED PCB THROUGH HOLE



NOTE: LAND PATTERN AND THROUGH HOLE DIMENSIONS SERVE ONLY AS AN INITIAL GUIDE.
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