# VN0300

## N-Channel Enhancement-Mode Vertical DMOS FET

### Features

- Free from Secondary Breakdown
- Low Power Drive Requirement
- Ease of Paralleling
- Low $C_{ISS}$ and Fast Switching Speeds
- Excellent Thermal Stability
- Integral Source-Drain Diode
- High Input Impedance and High Gain

### Applications

- Motor Controls
- Converters
- Amplifiers
- Switches
- Power Supply Circuits
- Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

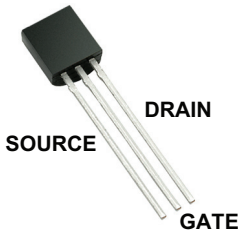
### General Description

The VN0300 Enhancement-mode (normally-off) transistors uses a vertical DMOS structure and a well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally induced secondary breakdown.

Microchip's vertical DMOS FETs are ideally suited for a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance and fast switching speeds are desired.

### Package Type

**3-lead TO-92**
(Top view)




See Table 2-1 for pin information.

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## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings†

Drain-to-Source Voltage ..... $BV_{DSS}$
Drain-to-Gate Voltage ..... $BV_{DGS}$
Gate-to-Source Voltage ..... ±30V
Operating Ambient Temperature, $T_A$ ..... –55°C to +150°C
Storage Temperature, $T_S$ ..... –55°C to +150°C

**† Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS

**Electrical Specifications:** $T_A$ = 25°C unless otherwise specified. All DC parameters are 100% tested at 25°C unless otherwise stated. Pulse test: 300 µs pulse, 2% duty cycle

| Parameter | Sym. | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| Drain-to-Source Breakdown Voltage | $BV_{DSS}$ | 30 | — | — | V | $V_{GS}$ = 0V, $I_D$ = 10 µA |
| Gate Threshold Voltage | $V_{GS(th)}$ | 0.8 | — | 2.5 | V | $V_{GS}$ = $V_{DS}$, $I_D$ = 1 mA |
| Gate Body Leakage Current | $I_{GSS}$ | — | — | 100 | nA | $V_{GS}$ = ± 30V, $V_{DS}$ = 0V |
| Zero-Gate Voltage Drain Current | $I_{DSS}$ | — | — | 10 | µA | $V_{GS}$ = 0V, $V_{DS}$ = Maximum rating |
| | | — | — | 500 | µA | $V_{GS}$ = 0V, $V_{DS}$ = 30V, $T_A$ = 125°C (**Note 1**) |
| On-State Drain Current | $I_{D(ON)}$ | 1 | — | — | A | $V_{GS}$ = 10V, $V_{DS}$ = 10V |
| Static Drain-to-Source On-State Resistance | $R_{DS(ON)}$ | — | — | 3.3 | Ω | $V_{GS}$ = 5V, $I_D$ = 300 mA |
| | | — | — | 1.2 | Ω | $V_{GS}$ = 10V, $I_D$ = 1A |

**Note 1:** Specification is obtained by characterization and is not 100% tested.

## AC ELECTRICAL CHARACTERISTICS

**Electrical Specifications:** $T_A$ = 25°C unless otherwise specified. All AC parameters are not 100% sample tested.

| Parameter | Sym. | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| Forward Transconductance | $G_{FS}$ | 200 | — | — | mmho | $V_{DS}$ = 10V, $I_D$ = 500 mA |
| Input Capacitance | $C_{ISS}$ | — | — | 190 | pF | $V_{GS}$ = 0V, $V_{DS}$ = 20V, f = 1 MHz |
| Common-Source Output Capacitance | $C_{OSS}$ | — | — | 110 | pF | |
| Reverse Transfer Capacitance | $C_{RSS}$ | — | — | 50 | pF | |
| Turn-On Time | $t_{(ON)}$ | — | — | 30 | ns | $V_{DD}$ = 25V, $I_D$ = 1A, $R_{GEN}$ = 25Ω |
| Turn-Off Time | $t_{(OFF)}$ | — | — | 30 | ns | |
| **DIODE PARAMETER** | | | | | | |
| Diode Forward Voltage Drop | $V_{SD}$ | — | 0.9 | — | V | $V_{GS}$ = 0V, $I_{SD}$ = 630 mA (**Note 1**) |

**Note 1:** Unless otherwise stated, all DC parameters are 100% tested at 25°C. Pulse test: 300 µs pulse, 2% duty cycle


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## TEMPERATURE SPECIFICATIONS

| Parameter | Sym. | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| **TEMPERATURE RANGE** | | | | | | |
| Operating Ambient Temperature | $T_A$ | –55 | — | +150 | °C | |
| Storage Temperature | $T_S$ | –55 | — | +150 | °C | |
| **PACKAGE THERMAL RESISTANCE** | | | | | | |
| 3-lead TO-92 | $\theta_{JA}$ | — | 132 | — | °C/W | |

## THERMAL CHARACTERISTICS

| Package | $I_D$ (Note 1) (Continuous) (mA) | $I_D$ (Pulsed) (A) | Power Dissipation at $T_A$ = 25°C (W) | $I_{DR}$ (Note 1) (mA) | $I_{DRM}$ (A) |
|---|---|---|---|---|---|
| 3-lead TO-92 | 640 | 3 | 1 | 640 | 3 |

**Note 1:** $I_D$ (continuous) is limited by maximum rated $T_J$.

## 2.0 PIN DESCRIPTION

The details on the pins of VN0300 are listed in Table 2-1. Refer to **Package Type** for the location of the pins.

**TABLE 2-1: PIN FUNCTION TABLE**

| Pin Number | Pin Name | Description |
|---|---|---|
| 1 | Source | Source |
| 2 | Gate | Gate |
| 3 | Drain | Drain |


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## 3.0 FUNCTIONAL DESCRIPTION

Figure 3-1 illustrates the switching waveforms and test circuit for VN0300.

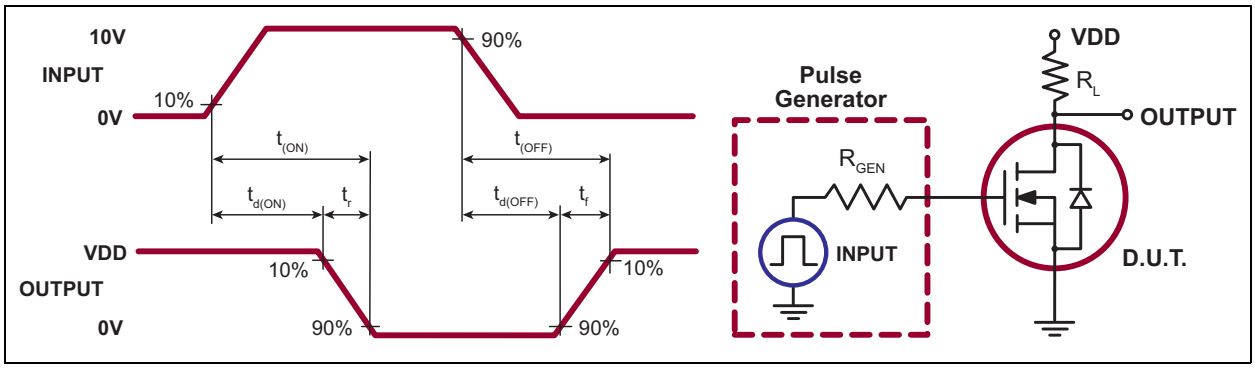


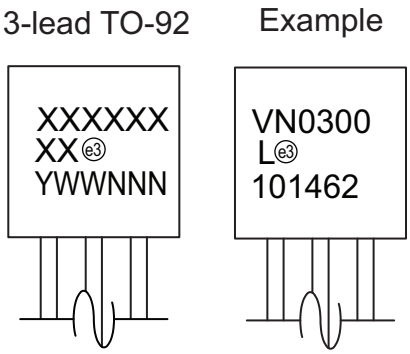

***FIGURE 3-1:*** *Switching Waveforms and Test Circuit.*

**TABLE 3-1: PRODUCT SUMMARY**

| $BV_{DSS}/BV_{DGS}$ (V) | $R_{DS(ON)}$ (Maximum) (Ω) | $I_{DSS}$ (Minimum) (A) |
|---|---|---|
| 30 | 1.2 | 1 |

## 4.0 PACKAGING INFORMATION

### 4.1 Package Marking Information

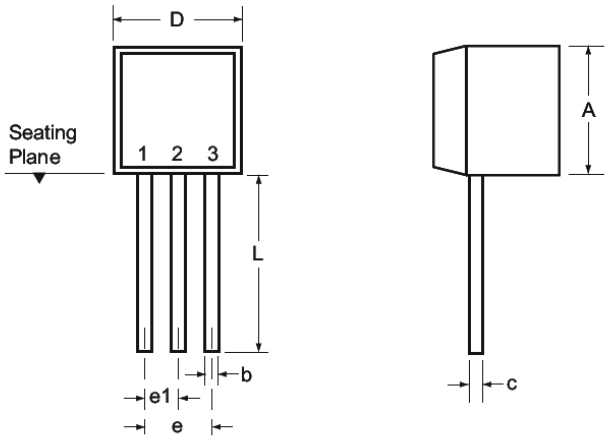


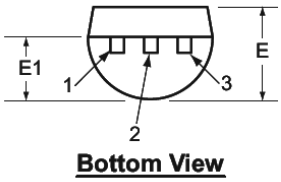

| | | |
|---|---|---|
| **Legend:** | XX...X | Product Code or Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC® designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |

**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.


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## 3-Lead TO-92 Package Outline (L/LL/N3)




Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

| Symbol | | A | b | c | D | E | E1 | e | e1 | L |
|---|---|---|---|---|---|---|---|---|---|---|
| Dimensions (inches) | MIN | .170 | .014† | .014† | .175 | .125 | .080 | .095 | .045 | .500 |
| | NOM | - | - | - | - | - | - | - | - | - |
| | MAX | .210 | .022† | .022† | .205 | .165 | .105 | .105 | .055 | .610* |

*JEDEC Registration TO-92.*
** This dimension is not specified in the JEDEC drawing.*
*† This dimension differs from the JEDEC drawing.*
***Drawings not to scale.***

**NOTES:**


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# APPENDIX A: REVISION HISTORY

## Revision A (July 2021)

- Converted Supertex Doc# DSFP-VN0300 to Microchip DS20005977A
- Added a pin function table
- Changed the package marking format
- Removed the 3-Lead TO-92 L P003, P005, P013, and P014 media types to align packaging specifications with the actual BQM
- Made minor text changes throughout the document

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

| PART NO. | XX | - | X | - | X |
|---|---|---|---|---|---|
| Device | Package Options | | Environmental | | Media Type |

| | | | |
|---|---|---|---|
| Device: | VN0300 | = | N-Channel Enhancement-Mode Vertical DMOS FET |
| Package: | L | = | 3-lead TO-92 |
| Environmental: | G | = | Lead (Pb)-free/RoHS-compliant Package |
| Media Types: | (blank) | = | 1000/Bag for an L package |
| | P002 | = | 2000/Reel (Reverse T/R) for an L Package |

**Examples:**

| | |
|---|---|
| a) VN0300L-G: | N-Channel Enhancement-Mode, Vertical DMOS FET, 3-lead TO-92, 1000/Bag |
| b) VN0300L-G-P002: | N-Channel Enhancement-Mode, Vertical DMOS FET, 3-lead TO-92, 2000/Reel (Reverse T/R) |


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