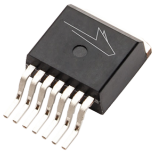
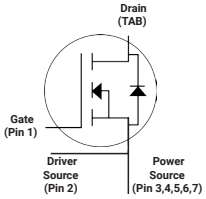
# C3M0045065J1

## Silicon Carbide Power MOSFET
## C3M™ MOSFET Technology
## N-Channel Enhancement Mode



TO-263-7L XL




Package Types: TO-263-7L XL
PN's: C3M0045065J1

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### Features

- 3rd generation SiC MOSFET technology
- Optimized package with separate driver source pin
- High blocking voltage with low on-resistance
- High-speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery ($Q_{rr}$)
- Halogen free, RoHS compliant

### Typical Applications

- Datacenter and telecom power supplies
- EV battery chargers
- High voltage DC/DC converters
- Energy storage systems
- Solar inverters

### Benefits

- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Reduce cooling requirements
- Increase power density
- Increase system switching frequency

### Key Parameters

| Parameter | Symbol | Min. | Typ. | Max | Unit | Conditions | Note |
|---|---|---|---|---|---|---|---|
| Drain - Source Voltage | $V_{DS}$ | | | 650 | | $T_C$ = 25°C | |
| Maximum Gate - Source Voltage | $V_{GS(max)}$ | -8 | | +19 | V | Transient | |
| Operational Gate-Source Voltage | $V_{GS\ op}$ | | -4/15 | | | Static | Note 1 |
| DC Continuous Drain Current | $I_D$ | | | 47 | A | $V_{GS}$ = 15 V, $T_C$ = 25 °C, $T_J$ ≤150 °C | Fig. 19 Note 2 |
| | | | | 31 | | $V_{GS}$ = 15 V, $T_C$ = 100 °C, $T_J$ ≤150 °C | |
| Pulsed Drain Current | $I_{DM}$ | | | 132 | | $t_{Pmax}$ limited by $T_{jmax}$ $V_{GS}$ = 15V, $T_C$ = 25 °C | Fig. 22 |
| Power Dissipation | $P_D$ | | | 147 | W | $T_C$ = 25 °C, $T_J$ = 150 °C | Fig. 20 |
| Operating Junction Temperature | $T_J$ | | | -40 to +175 | °C | | |
| Case and Storage Temperature | $T_c$ , $T_{stg}$ | | | -40 to 150 | | | |
| Solder Temperature | $T_L$ | | | 260 | | According to JEDEC J-STD-020 | |

Note (1): Recommended turn-on gate voltage is 15V with ±5% regulation tolerance, see Application Note PRD-04814 for additional details
Note (2): Verified by design



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## Electrical Characteristics ($T_C$ = 25 °C Unless Otherwise Specified)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test Conditions | Note |
|---|---|---|---|---|---|---|---|
| Drain-Source Breakdown Voltage | $V_{(BR)DSS}$ | 650 | | | V | $V_{GS}$ = 0 V, $I_D$ = 100 µA | |
| Gate Threshold Voltage | $V_{GS(th)}$ | 1.8 | 2.6 | 3.6 | | $V_{DS}$ = $V_{GS}$, $I_D$ = 4.84 mA | Fig. 11 |
| | | | 2.3 | | | $V_{DS}$ = $V_{GS}$, $I_D$ = 4.84 mA, $T_J$ = 150 °C | |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | | 1 | 50 | µA | $V_{DS}$ = 650 V, $V_{GS}$ = 0 V | |
| Gate-Source Leakage Current | $I_{GSS}$ | | 10 | 250 | nA | $V_{GS}$ = 15 V, $V_{DS}$ = 0 V | |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | | 45 | 60 | mΩ | $V_{GS}$ = 15 V, $I_D$ = 17.6 A | Fig. 4, 5, 6 |
| | | | 54 | | | $V_{GS}$ = 15 V, $I_D$ = 17.6 A, $T_J$ = 150 °C | |
| Transconductance | $g_{fs}$ | | 12 | | S | $V_{DS}$ = 20 V, $I_{DS}$ = 17.6 A | Fig. 7 |
| | | | 11 | | | $V_{DS}$ = 20 V, $I_{DS}$ = 17.6 A, $T_J$ = 150 °C | |
| Input Capacitance | $C_{iss}$ | | 1621 | | pF | $V_{GS}$ = 0 V, $V_{DS}$ = 0 V to 400 V<br>f = 1 MHz<br>$V_{AC}$ = 25 mV | Fig. 17, 18 |
| Output Capacitance | $C_{oss}$ | | 101 | | | | |
| Reverse Transfer Capacitance | $C_{rss}$ | | 8 | | | | |
| Effective Output Capacitance (Energy Related) | $C_{o(er)}$ | | 126 | | | $V_{GS}$ = 0 V, $V_{DS}$ = 0 V to 400 V | Note: 2 |
| Effective Output Capacitance (Time Related) | $C_{o(tr)}$ | | 178 | | | | Note: 2 |
| $C_{oss}$ Stored Energy | $E_{oss}$ | | 10 | | µJ | $V_{DS}$ = 400 V, f = 1 MHz | Fig. 16 |
| Turn-On Switching Energy (Body Diode) | $E_{ON}$ | | 36 | | µJ | $V_{DS}$ = 400 V, $V_{GS}$ = -4 V/15 V, $I_D$ = 17.6 A,<br>$R_{G(ext)}$ = 2.5 Ω, L = 99 µH, $T_J$ = 25 °C<br>FWD = Internal Body Diode of MOSFET | Fig. 25 |
| Turn-Off Switching Energy (Body Diode) | $E_{OFF}$ | | 7 | | | | |
| Turn-On Delay Time | $t_{d(on)}$ | | 8 | | ns | $V_{DD}$ = 400 V, $V_{GS}$ = -4 V/15 V, $I_D$ = 17.6 A,<br>$R_{G(ext)}$ = 2.5 Ω, L = 99 µH<br>Timing Relative to $V_{DS}$<br>Inductive Load | Fig. 26 |
| Rise Time | $t_r$ | | 10 | | | | |
| Turn-Off Delay Time | $t_{d(off)}$ | | 19 | | | | |
| Fall Time | $t_f$ | | 6 | | | | |
| Internal Gate Resistance | $R_{G(int)}$ | | 3 | | Ω | f = 1 MHz, $V_{AC}$ = 25 mV | |
| Gate to Source Charge | $Q_{gs}$ | | 21 | | nC | $V_{DS}$ = 400 V, $V_{GS}$ = -4 V/15 V<br>$I_D$ = 17.6 A<br>Per IEC60747-8-4 pg 21 | Fig. 12 |
| Gate to Drain Charge | $Q_{gd}$ | | 16 | | | | |
| Total Gate Charge | $Q_g$ | | 61 | | | | |

Note (2): $C_{o(er)}$, a lumped capacitance that gives same stored energy as coss while $V_{DS}$ is rising from 0 to 400 V.
$C_{o(tr)}$, a lumped capacitance that gives same charging time as coss while $V_{DS}$ is rising from 0 to 400 V.


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## Reverse Diode Characteristics ($T_C$ = 25 °C Unless Otherwise Specified)

| Parameter | Symbol | Typ. | Max. | Unit | Test Conditions | Note |
|---|---|---|---|---|---|---|
| Diode Forward Voltage | $V_{SD}$ | 4.8 | | V | $V_{GS}$ = -4 V, $I_{SD}$ = 8.8 A, $T_J$ = 25 °C | Fig. 8, 9, 10 |
| | | 4.2 | | | $V_{GS}$ = -4 V, $I_{SD}$ = 8.8 A, $T_J$ = 150 °C | |
| Continuous Diode Forward Current | $I_S$ | | 26 | A | $V_{GS}$ = -4 V, $T_C$ = 25 °C | |
| Diode Pulse Current | $I_{S, pulse}$ | | 132 | | $V_{GS}$ = -4 V, Pulse Width $t_P$ Limited by $T_{jmax}$ | |
| Reverse Recovery Time | $t_{rr}$ | 10 | | ns | $V_{GS}$ = -4 V, $I_{SD}$ = 17.6 A , $V_R$ = 400 V dif/dt = 5420 A/µs, $T_J$ = 25 °C | |
| Reverse Recovery Charge | $Q_{rr}$ | 206 | | nC | | |
| Peak Reverse Recovery Current | $I_{rrm}$ | 36 | | A | | |
| Reverse Recovery Time | $t_{rr}$ | 13 | | ns | $V_{GS}$ = -4 V, $I_{SD}$ = 17.6 A , $V_R$ = 400 V dif/dt = 1915 A/µs, $T_J$ = 25 °C | |
| Reverse Recovery Charge | $Q_{rr}$ | 103 | | nC | | |
| Peak Reverse Recovery Current | $I_{rrm}$ | 14 | | A | | |

## Thermal Characteristics

| Parameter | Symbol | Typ. | Unit | Test Conditions | Note |
|---|---|---|---|---|---|
| Thermal Resistance from Junction to Case | $R_{\theta JC}$ | 0.85 | °C/W | | Fig. 21 |
| Thermal Resistance from Junction to Ambient | $R_{\theta JA}$ | 40 | | | |



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## Typical Performance

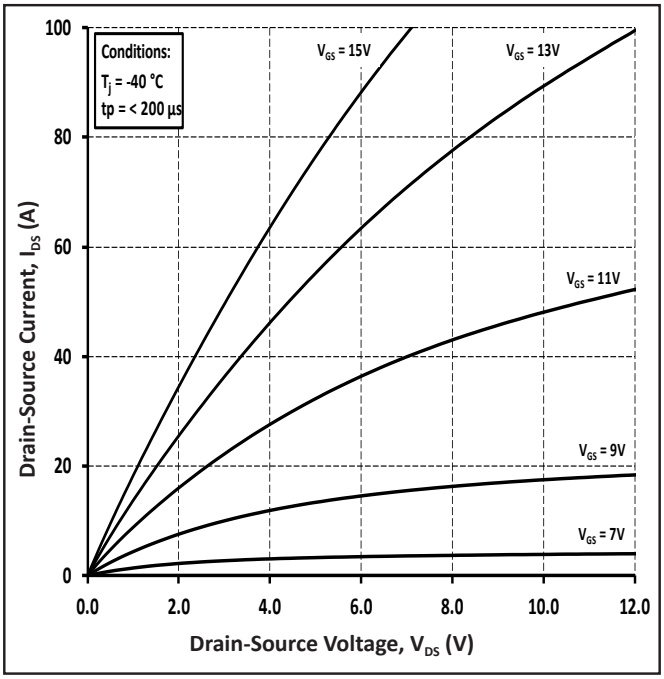



Figure 1. Output Characteristics $T_J$ = -40 °C

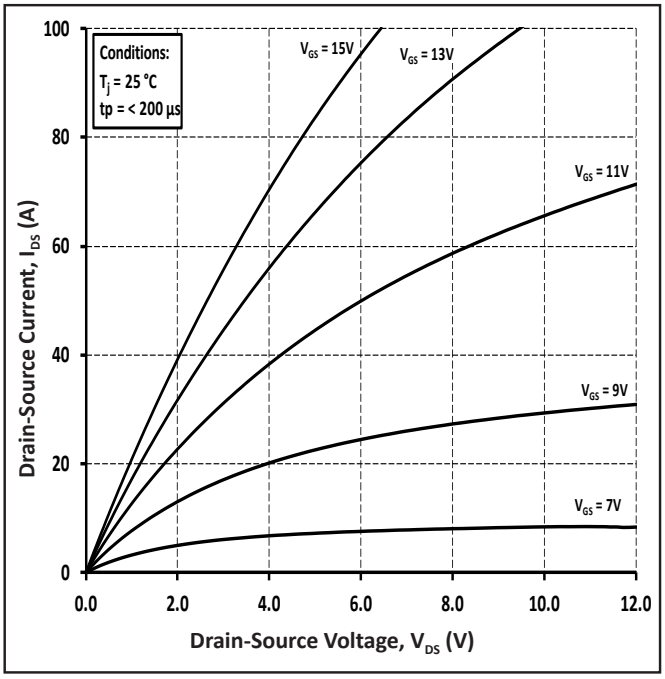



Figure 2. Output Characteristics $T_J$ = 25 °C

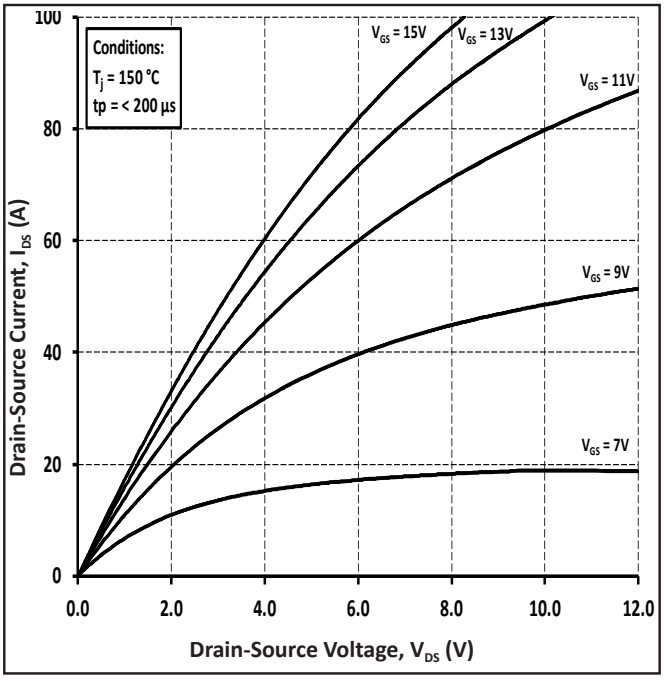



Figure 3. Output Characteristics $T_J$ = 150 °C

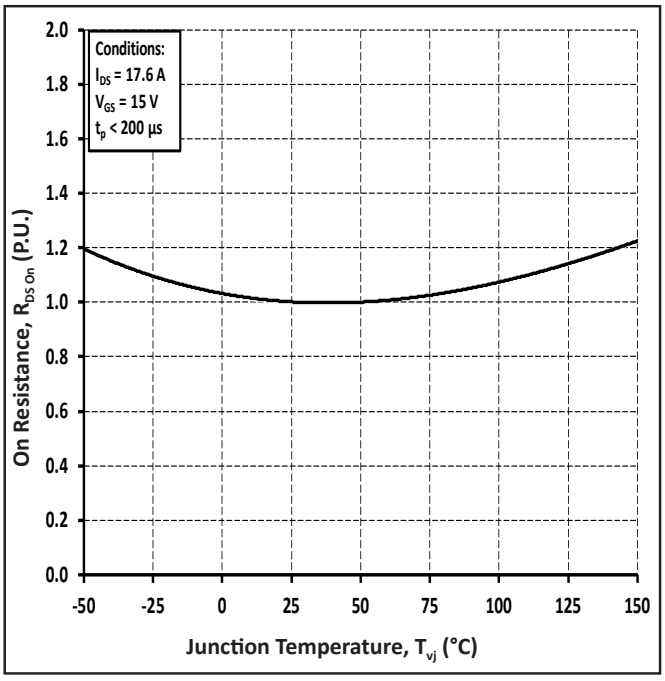



Figure 4. Normalized On-Resistance vs Temperature



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## Typical Performance

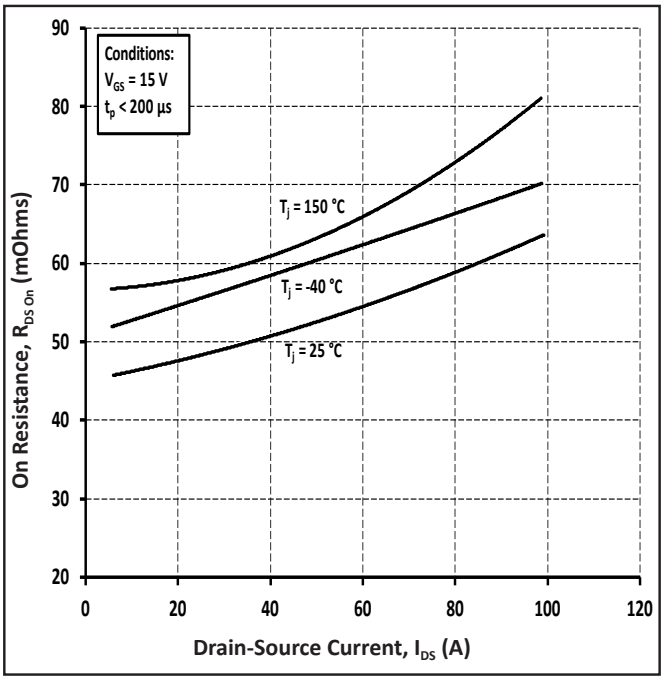



Figure 5. On-Resistance vs Drain Current for Various Temperatures

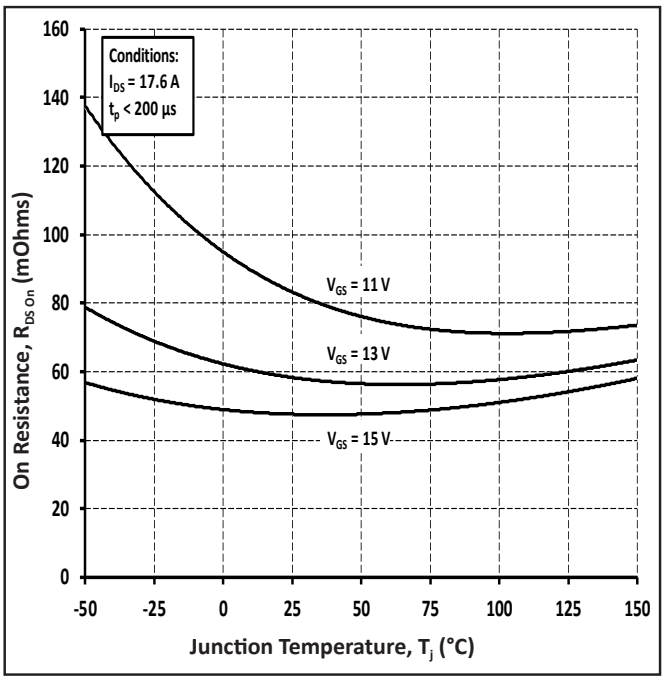



Figure 6. On-Resistance vs Temperature for Various Gate Voltage

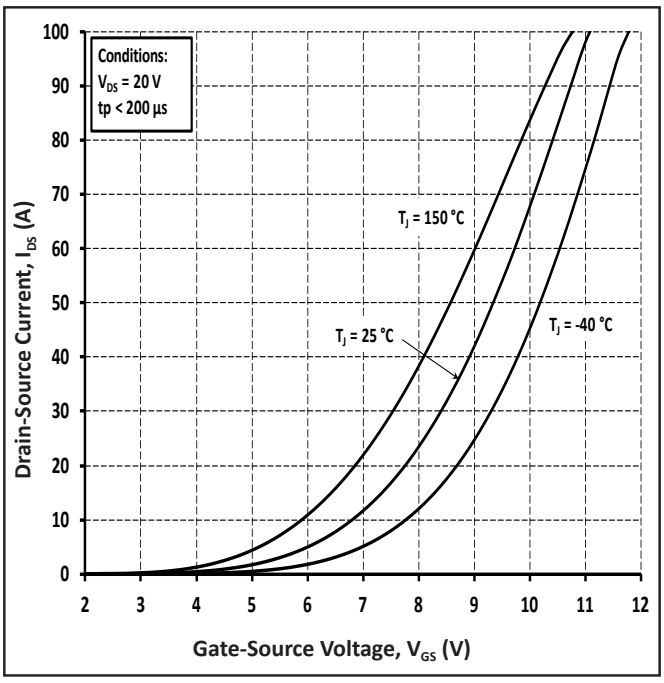



Figure 7. Transfer Characteristic for Various Junction Temperatures

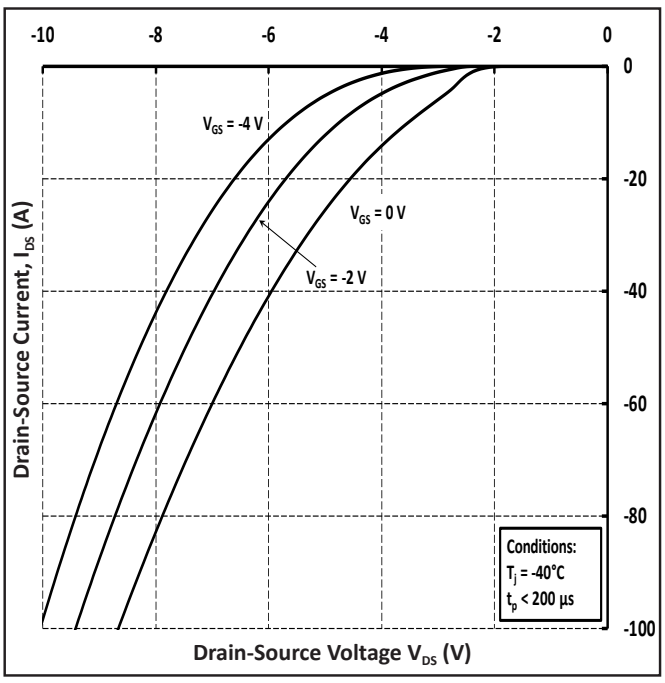



Figure 8. Body Diode Characteristic at -40 °C


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## Typical Performance

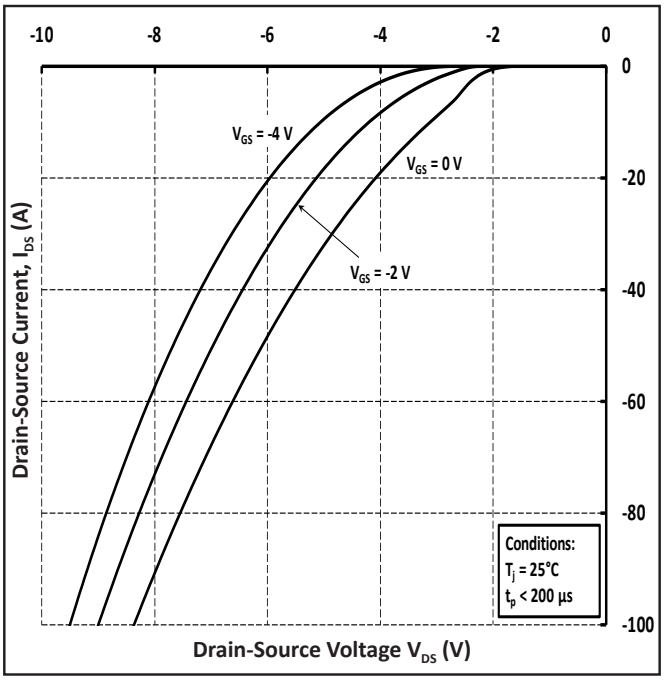



Figure 9. Body Diode Characteristic at 25 °C

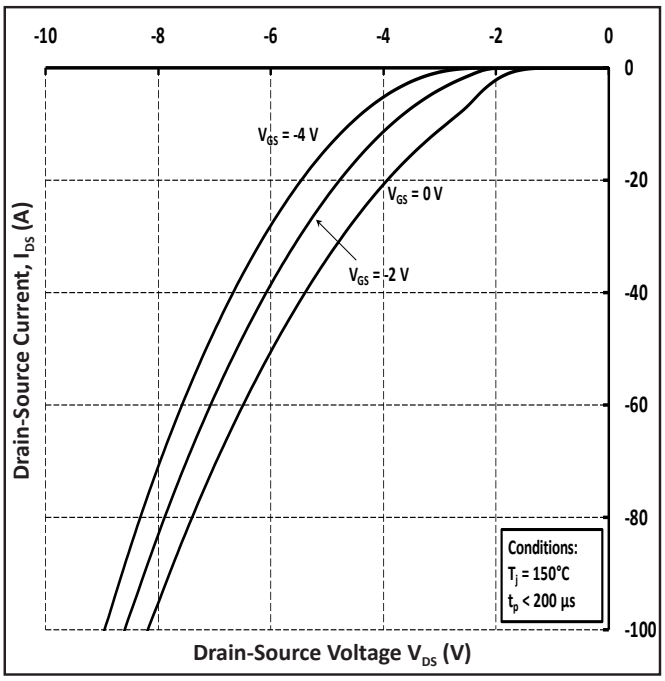



Figure 10. Body Diode Characteristic at 150 °C

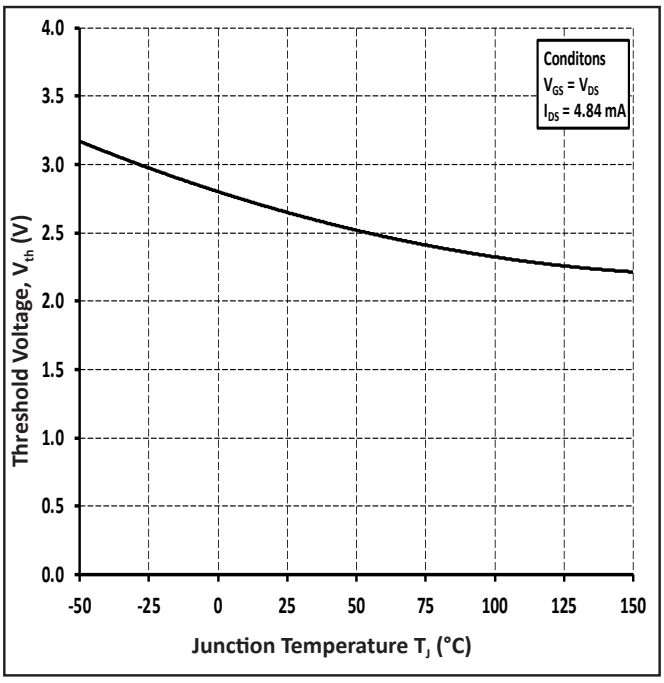



Figure 11. Threshold Voltage vs Temperature

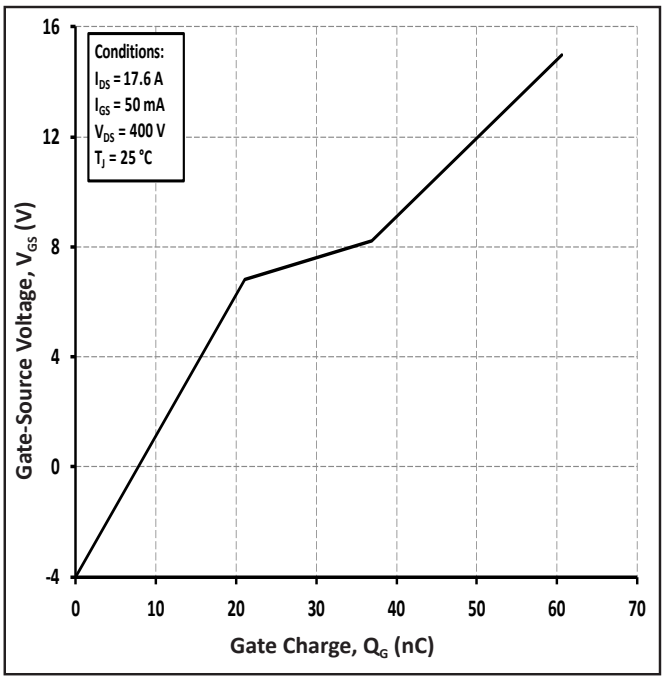



Figure 12. Gate Charge Characteristic


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## Typical Performance

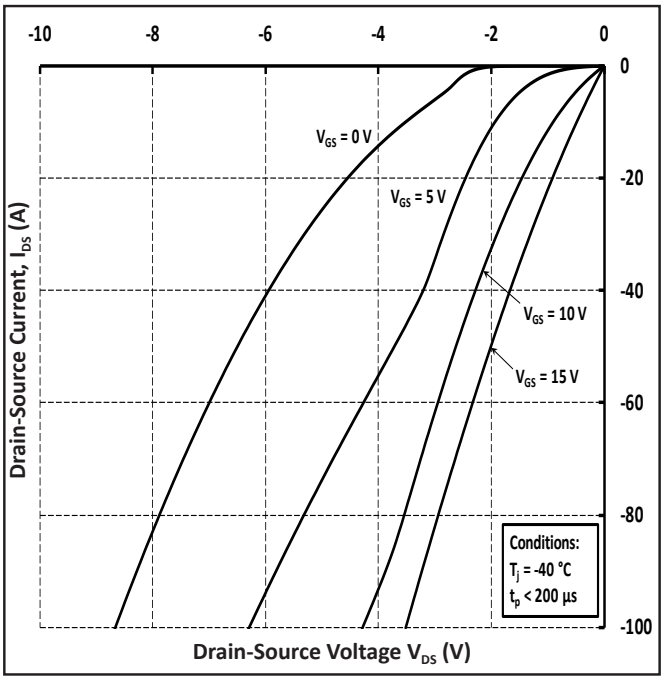



Figure 13. 3rd Quadrant Characteristic at -40 °C

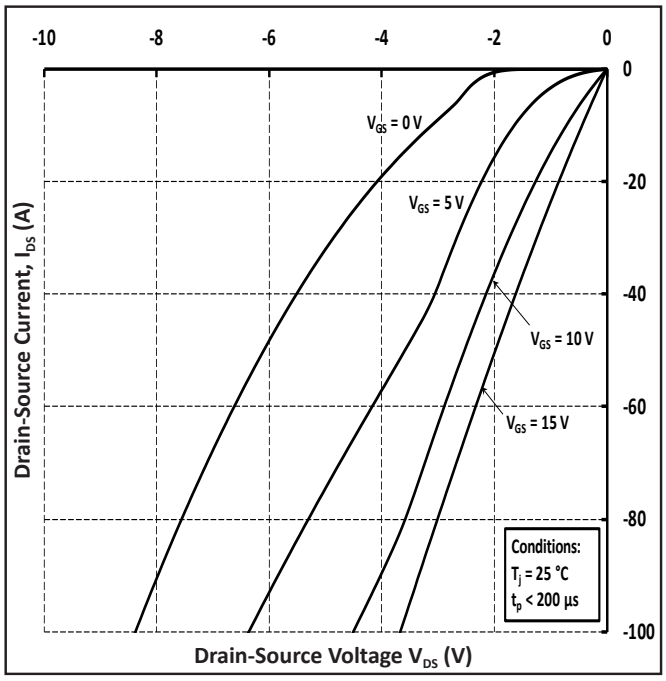



Figure 14. 3rd Quadrant Characteristic at 25 °C

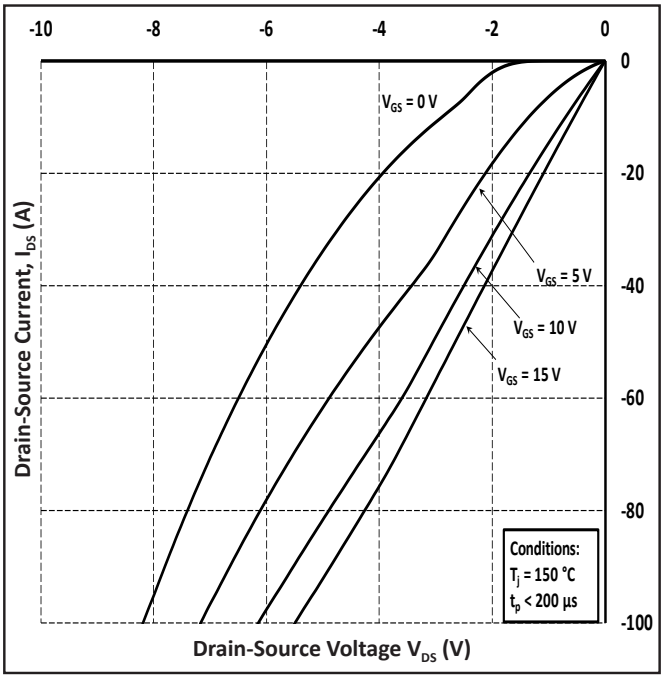



Figure 15. 3rd Quadrant Characteristic at 150 °C

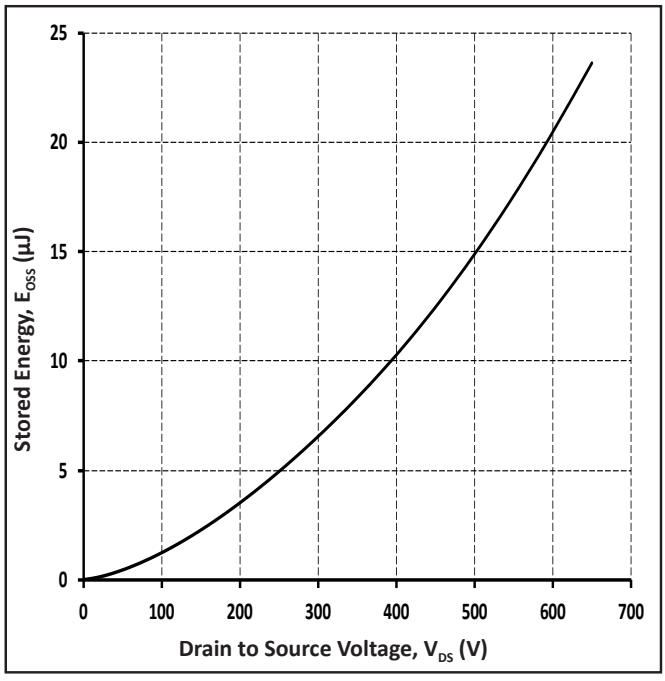



Figure 16. Output Capacitor Stored Energy


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## Typical Performance

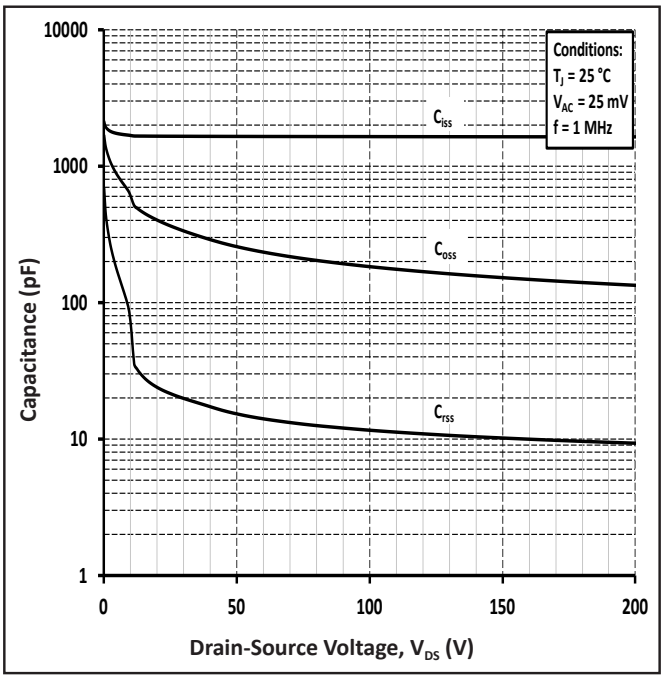



Figure 17. Capacitances vs Drain-Source Voltage (0-200 V)

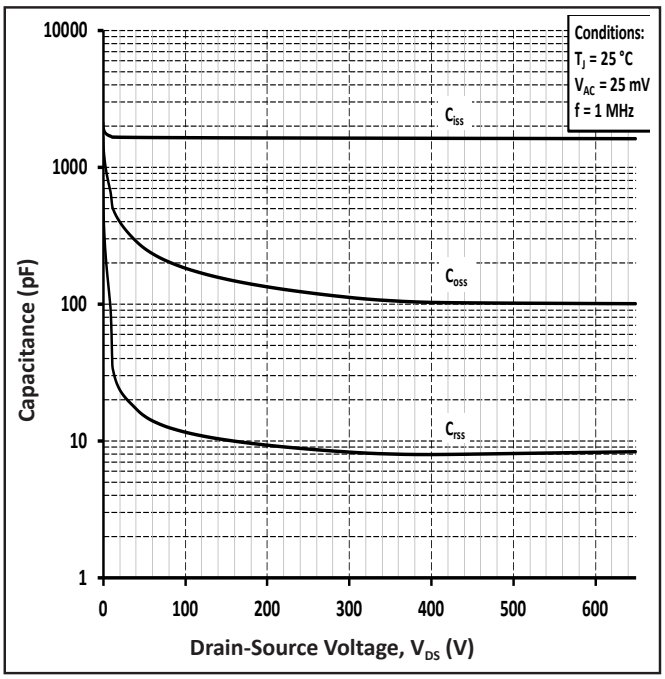



Figure 18. Capacitances vs Drain-Source Voltage (0-600 V)

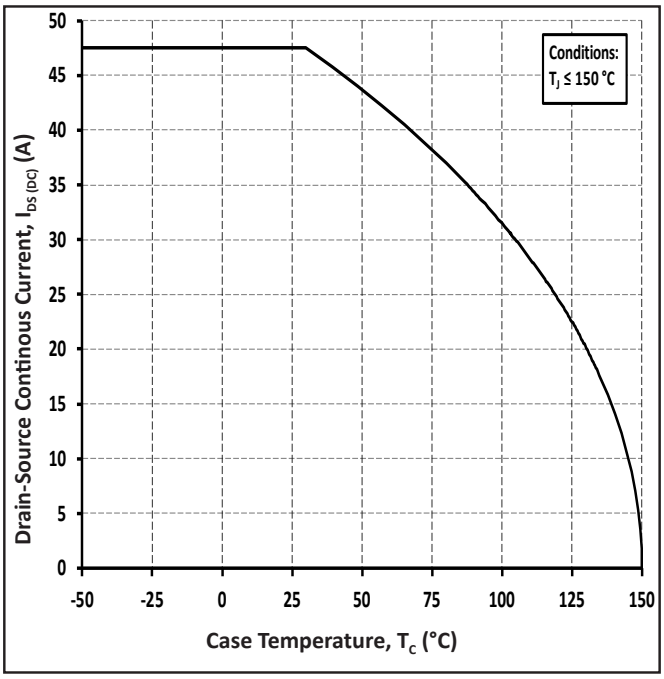



Figure 19. Continuous Drain Current Derating vs Case Temperature

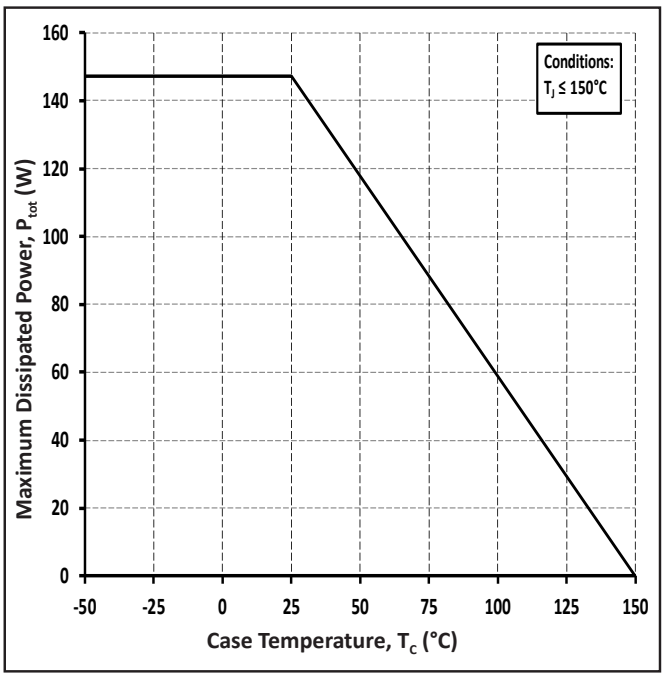



Figure 20. Maximum Power Dissipation Derating vs Case Temperature



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## Typical Performance

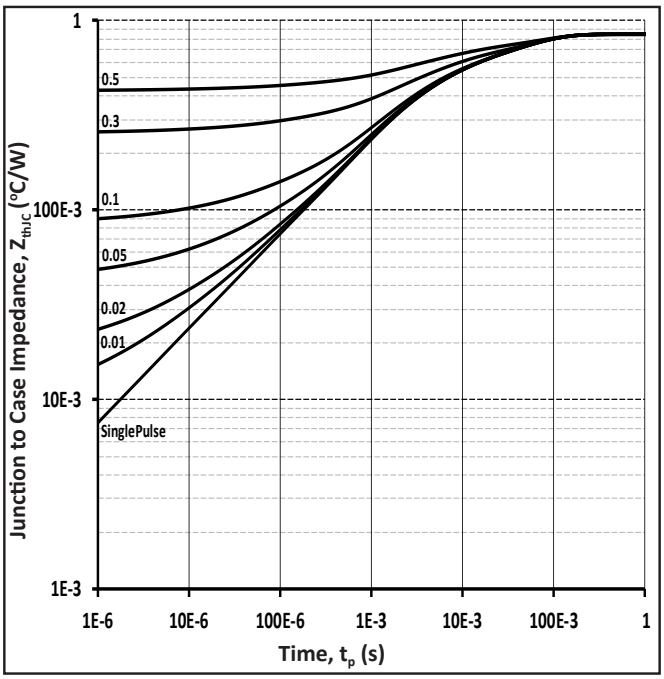



Figure 21. Transient Thermal Impedance (Junction - Case)

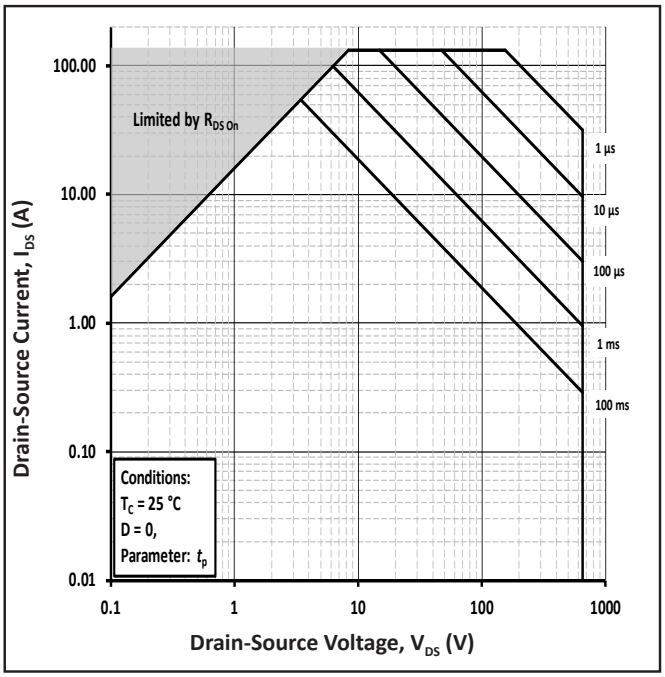



Figure 22. Safe Operating Area

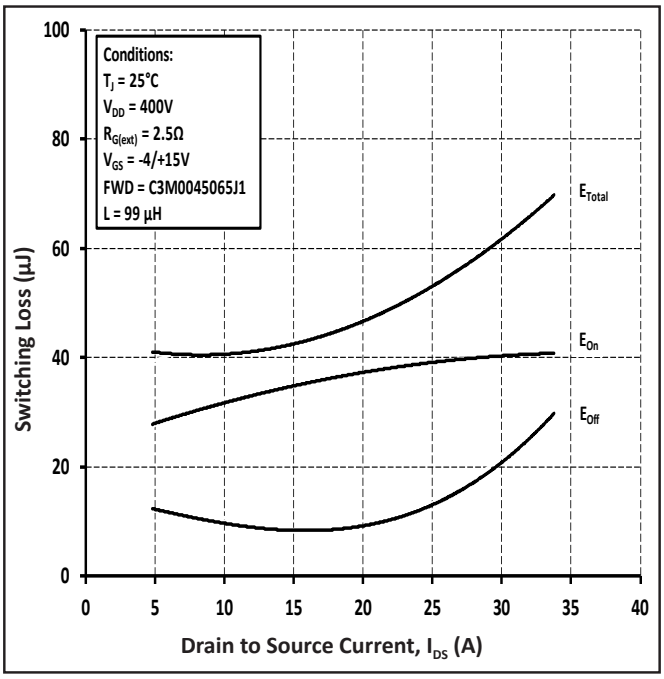



Figure 23. Clamped Inductive Switching Energy vs Drain Current ($V_{DD}$ = 400 V)

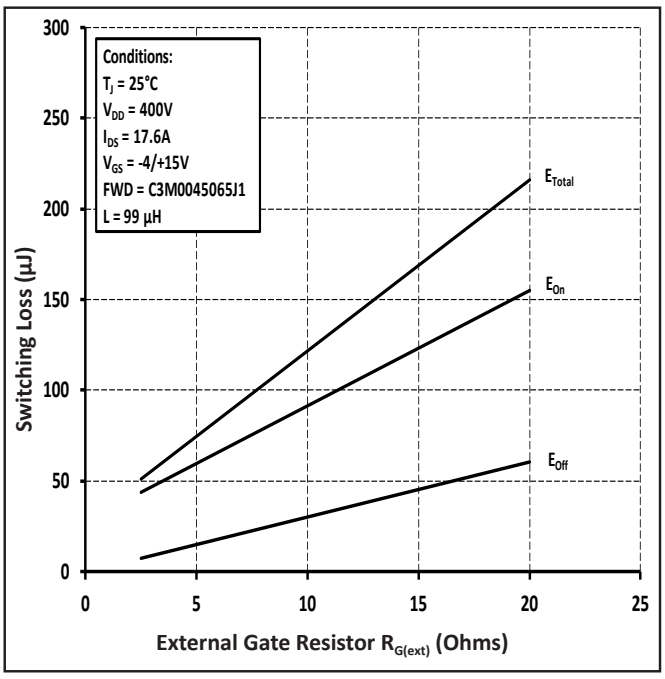



Figure 24. Clamped Inductive Switching Energy vs $R_{G(ext)}$


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## Typical Performance

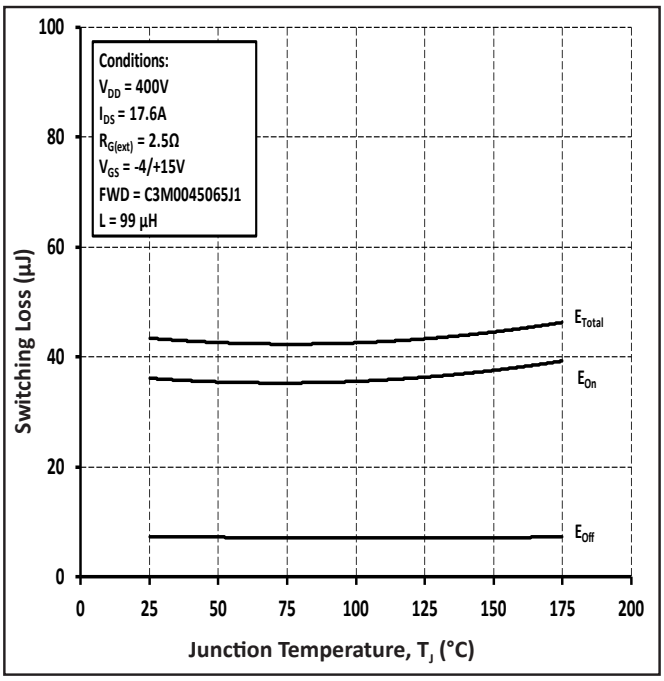



Figure 25. Clamped Inductive Switching Energy vs Temperature

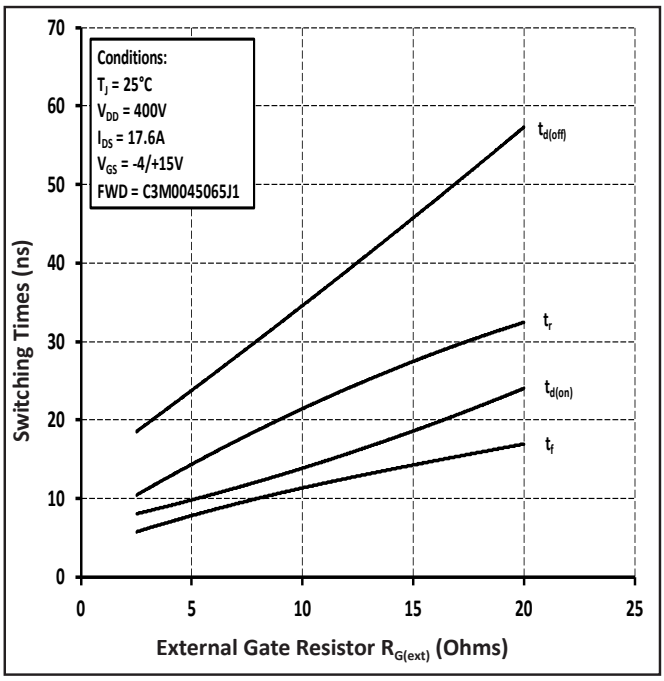



Figure 26. Switching Times vs $R_{G(ext)}$

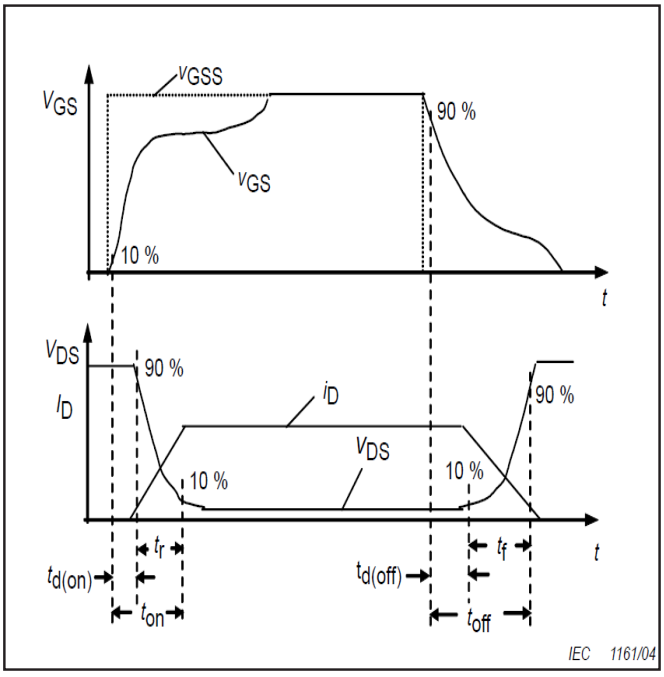



Figure 27. Switching Times Definition


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## Test Circuit Schematic

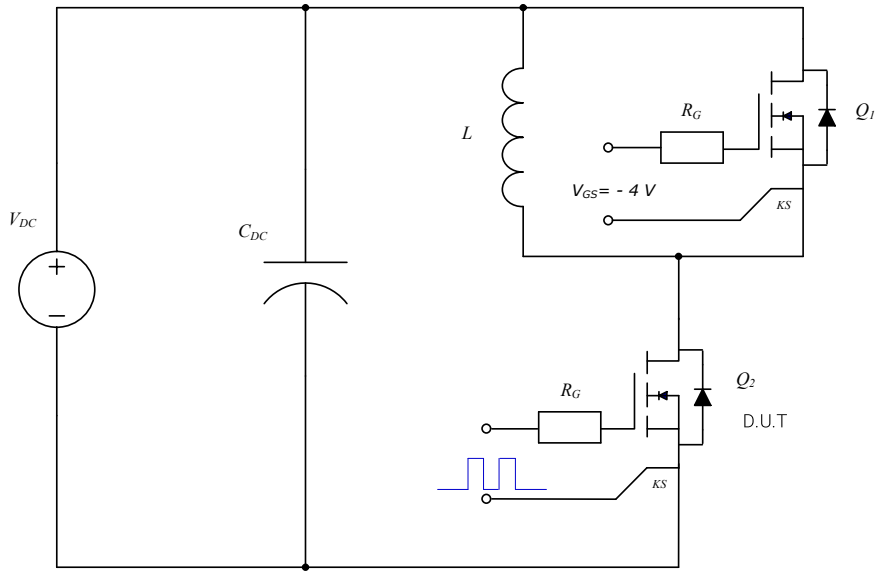


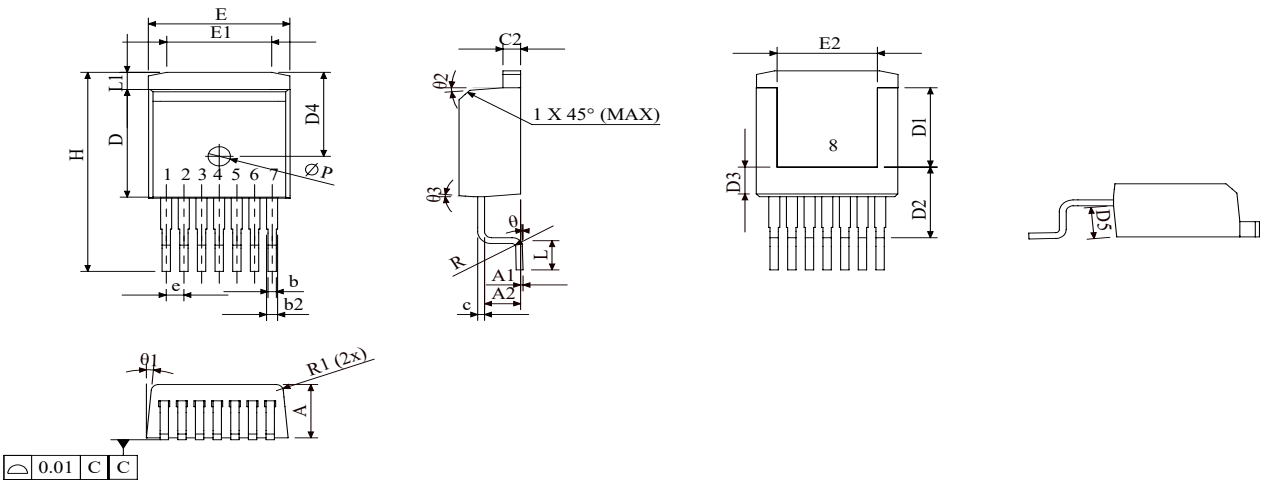

Figure 28. Clamped Inductive Switching Waveform Test Circuit

Note (3): Turn-off and Turn-on switching energy and timing values measured using SiC MOSFET body diode as shown above.


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## Package Dimensions

Package: TO-263-7L XL




| SYMBOL | MIN (mm) | MAX (mm) |
|---|---|---|
| A | 4.30 | 4.57 |
| A1 | 0.00 | 0.25 |
| A2 | 2.595 REF | |
| b | 0.50 | 0.70 |
| b2 | 0.60 | 1.00 |
| c | 0.281 | 0.481 |
| C2 | 1.17 | 1.37 |
| D | 9.025 | 9.125 |
| D1 | 6.50 | 6.70 |
| D2 | 5.39 REF | |
| D3 | 2.148 | --- |
| D4 | 7.000 REF | |
| D5 | 2.555 | --- |
| A2 | 2.595 REF | |
| E | 10.13 | 10.23 |
| E1 | 6.50 | 8.60 |
| E2 | 6.778 | 7.665 |
| e | 1.27 TYP | |
| H | 15.043 | 17.313 |
| L | 2.324 | 2.700 |
| L1 | 0.968 | 1.868 |
| R | 0.506 REF | |
| R1 | 0.500 REF | |
| P | 1.60 REF | |
| θ | 0° | 8° |
| θ1 | 4.5° | 5.5° |
| θ2 | 4° | 6° |
| θ3 | 4° | 6° |

| | |
|---|---|
| 1 | GATE |
| 2 | KELVIN |
| 3 | SOURCE |
| 4 | |
| 5 | |
| 6 | |
| 7 | |
| 8 | DRAIN |

NOTE
1. ALL METAL SURFACES ARE TIN PLATED (MATTE), EXCEPT AREA OF CUT.
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
3. ALL DIMENSIONS ARE LISTED IN MILLIMETERS. ANGLES ARE IN DEGREES.
4. PACKAGE BURR FLASH SIZE (0.5 mm) IS NOT INCLUDED IN THE DIMENSIONS

Wolfspeed

TITLE:
PACKAGE OUTLINE DRAWING:
TO 263-7L J1

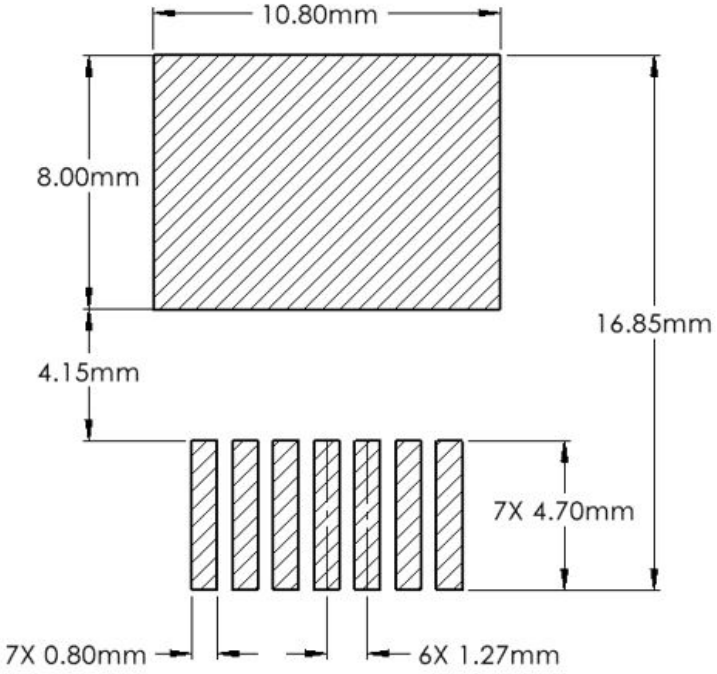
REVISION NO. 01 | A4

Date: 04/13/22 | SCALE:1:1 | SHEET 1 OF 1



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## Recommended Solder Pad Layout




## Revision History

| Current Revision | Date of Release | Description of Changes |
|---|---|---|
| 0 | October-2021 | N/A |
| 1 | November-2023 | Updated Wolfspeed branding, package drawing, package image, solder pad layout, added revision history |
| 2 | December - 2024 | Legal Disclaimer Updated |


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