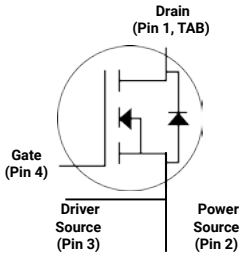
C3M0045065K

Silicon Carbide Power MOSFET C3M™ MOSFET Technology
N-Channel Enhancement Mode





RoHS

Halogen-Free

Features

- C3M™ Silicon Carbide (SiC) MOSFET technology
- Optimized package with separate driver source pin
- 8mm of creepage distance between drain and source
- High blocking voltage with low on-resistance
- High-speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery (Q_{rr})
- Halogen free, RoHS compliant

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Ordering Part Number	Package	Marking
C3M0045065K	TO 247-4	C3M0045065K

Typical Applications

- EV chargers
- Server & Telecom PSU
- UPS
- Solar inverters
- SMPS
- DC/DC converters

Benefits

- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Reduce cooling requirements
- Increase power density
- Increase system switching frequency

Key Parameters

Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions	Note
Drain - Source Voltage	V_{DS}			650	v	T_C = 25°C	
Maximum Gate - Source Voltage	$V_{GS(max)}$	-8		+19		Transient	
Operational Gate-Source Voltage	$V_{GS\ op}$		-4/15			Static	Note 1
DC Continuous Drain Current	I_D			49	A	V_{GS} = 15 V, T_C = 25 °C, T_J ≤175 °C	Fig. 19 Note 2
				35		V_{GS} = 15 V, T_C = 100 °C, T_J ≤175 °C	
Pulsed Drain Current	I_{DM}			132		t_{Pmax} limited by T_{jmax} V_{GS} = 15V, T_C = 25 °C	Fig. 22
Power Dissipation	P_D			176	W	T_C = 25 °C, T_J = 175 °C	Fig. 20
Operating Junction and Storage Temperature	T_J, T_{stg}			-40 to +175	°C		
Solder Temperature	T_L			260		According to JEDEC J-STD-020	
Mounting Torque	M_D			1 8.8	Nm lbf-in	M3 or 6-32 screw	

Note (1): Recommended turn-on gate voltage is 15V with ±5% regulation tolerance, see Application Note PRD-04814 for additional details
Note (2): Verified by design

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Electrical Characteristics (T_C = 25℃ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Note
Gate Threshold Voltage	$V_{GS(th)}$	1.8	2.6	3.6	V	V_{DS} = $V_{GS,}$ I_D = 4.84 mA	Fig. 11
		—	2.2	—		V_{DS} = $V_{GS,}$ I_D = 4.84 mA, T_J = 175°C	
Zero Gate Voltage Drain Current	I_{DSS}	—	1	50	µA	V_{DS} = 650 V, V_{GS} = 0 V	
Gate-Source Leakage Current	I_{GSS}	—	10	250	nA	V_{GS} = 15 V, V_{DS} = 0 V	
Drain-Source On-State Resistance	$R_{DS(on)}$	—	45	60	mΩ	V_{GS} = 15 V, I_D = 17.6 A	Fig. 4, 5, 6
		—	61	—		V_{GS} = 15 V, I_D = 17.6 A, T_J = 175°C	
Transconductance	g_{fs}	—	12	—	S	V_{DS} = 20 V, I_{DS} = 17.6 A	Fig. 7
			11			V_{DS} = 20 V, I_{DS} = 17.6 A, T_J = 175°C	
Input Capacitance	C_{iss}	—	1621	—	pF	V_{GS} = 0 V, V_{DS} = 0 V to 600 V f = 1 Mhz V_{AC} = 25 mV	Fig. 17, 18
Output Capacitance	C_{oss}	—	101	—			
Reverse Transfer Capacitance	C_{rss}	—	8	—			
Effective Output Capacitance (Energy Related)	$C_{o(er)}$	—	126	—		V_{GS} = 0 V, V_{DS} = 0 V to 400 V	Note 3
Effective Output Capacitance (Time Related)	$C_{o(tr)}$	—	178	—			
Output Capacitance Stored Energy	E_{oss}	—	20	—	µJ	V_{DS} = 600 V, f = 1 Mhz	Fig. 16
Turn-On Switching Energy (Body Diode)	E_{on}	—	57	—		V_{DS} = 400 V, V_{GS} = -4 V/15 V, I_D = 17.6 A, $R_{G(ext)}$ = 2.5 Ω, L= 99 µH, T_J = 175°C FWD = Internal Body Diode of MOSFET	Fig. 25
Turn Off Switching Energy (Body Diode)	E_{off}	—	14	—			
Turn-On Switching Energy (External Diode)	E_{on}	—	44	—		V_{DS} = 400 V, V_{GS} = -4 V/15 V, I_D = 17.6 A, $R_{G(ext)}$ = 2.5 Ω, L= 99 µH, T_J = 175°C FWD = External SiC DIODE	
Turn Off Switching Energy (External Diode)	E_{off}	-	14	—			
Turn-On Delay Time	$t_{d(on)}$	—	9	—	ns	V_{DD} = 400 V, V_{GS} = -4 V/15 V I_D = 17.6 A, $R_{G(ext)}$ = 2.5 Ω, L= 99 µH Timing relative to V_{DS} Inductive load	Fig. 26
Rise Time	t_r	—	12	—			
Turn-Off Delay Time	$t_{d(off)}$	—	18	—			
Fall Time	t_f	—	6	—			
Internal Gate Resistance	$R_{G(int)}$	—	3	—	Ω	f = 1 MHz, V_{AC} = 25 mV	
Gate to Source Charge	Q_{gs}	—	21	—	nC	V_{DS} = 400 V, V_{GS} = -4 V/15 V I_D = 17.6 A Per IEC60747-8-4 pg 21	Fig. 12
Gate to Drain Charge	Q_{gd}	—	18	—			
Total Gate Charge	Q_g	—	63	—			

Note:
[3] $C_{o(er)}$, a lumped capacitance that gives same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V
$C_{o(tr)}$, a lumped capacitance that gives same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

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Reverse Diode Characteristics (T_C = 25°C unless otherwise specified)

Parameter	Symbol	Typ.	Max.	Unit	Test Conditions	Notes
Diode Forward Voltage	V_F	4.8	—	V	V_{GS} = -4 V, I_{SD} = 8.8 A, T_J = 25°C	Fig. 8, 9, 10
		4.2	—		V_{GS} = -4 V, I_{SD} = 8.8 A, T_J = 175°C	
Continuous Diode Forward Current	I_S	—	29	A	V_{GS} = -4 V, T_C = 25°C	
Diode Pulse Current	I_{SM}	—	132		V_{GS} = -4 V, pulse width t_P limited by $T_{j\,max}$	
Reverse Recovery Time,	t_{rr}	13	—	ns	V_{GS} = -4 V, I_{SD} = 17.6 A, V_R = 400 V di_F/dt = 5215 A/µs, T_J = 175°C	
Reverse Recovery Charge	Q_{rr}	247	—	nC		
Peak Reverse Recovery Current	I_{RRM}	36	—	A		
Reverse Recovery Time,	t_{rr}	18	—	ns	V_{GS} = -4 V, I_{SD} = 17.6 A, V_R = 400 V di_F/dt = 1775 A/µs, T_J = 175°C	
Reverse Recovery Charge	Q_{rr}	171	—	nC		
Peak Reverse Recovery Current	I_{RRM}	16	—	A		

Thermal Characteristics

Parameter	Symbol	Typ.	Unit	Note
Thermal Resistance from Junction to Case	$R_{\theta JC}$	0.85	°C/W	Fig. 21
Thermal Resistance From Junction to Ambient	$R_{\theta JA}$	40		

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Typical Performance

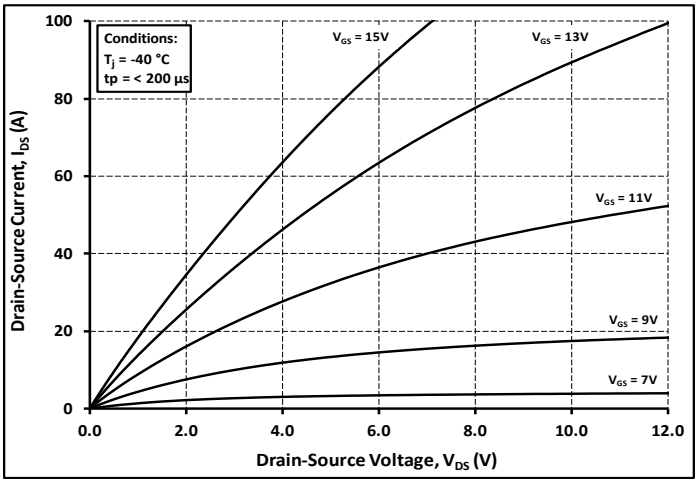


Figure 1. Output Characteristics T_J = -40°C

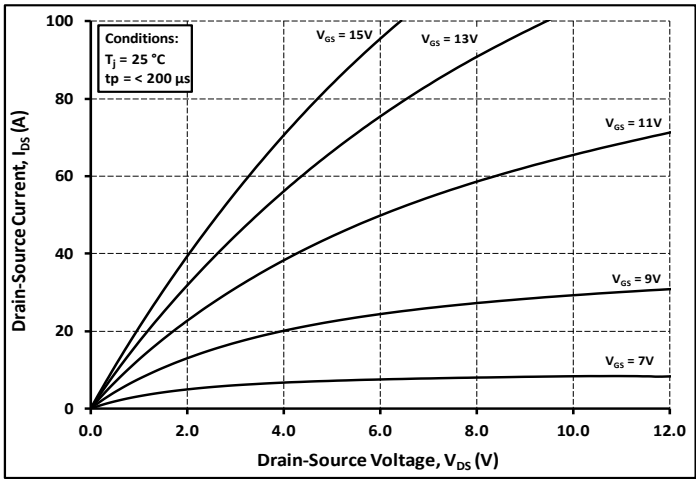


Figure 2. Output Characteristics T_J = 25°C

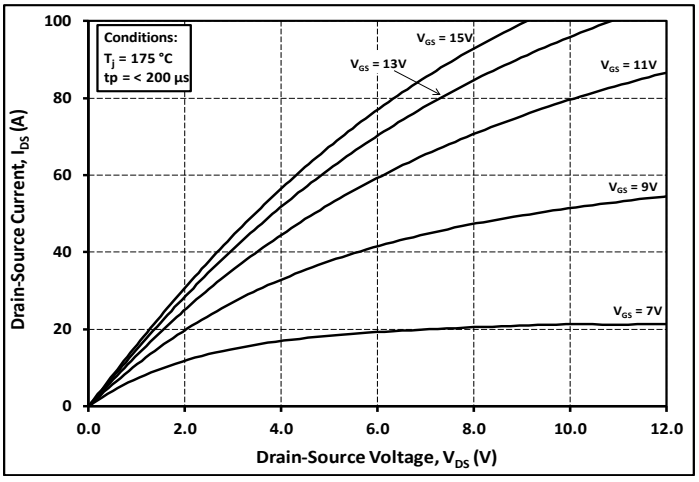


Figure 3. Output Characteristics T_J = 175°C

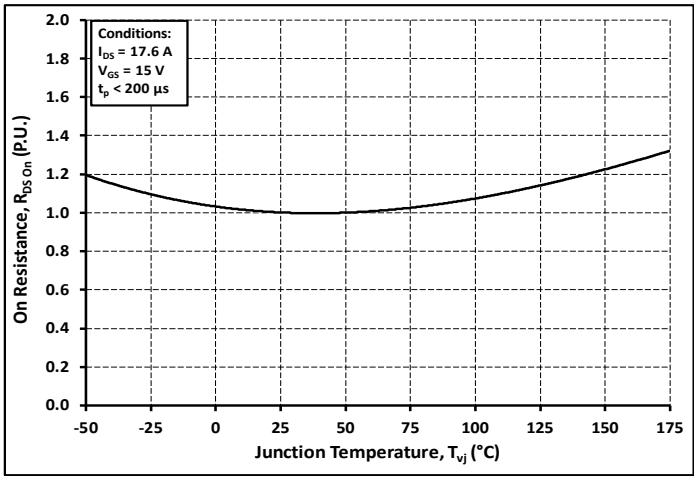


Figure 4. Normalized On-Resistance vs. Temperature

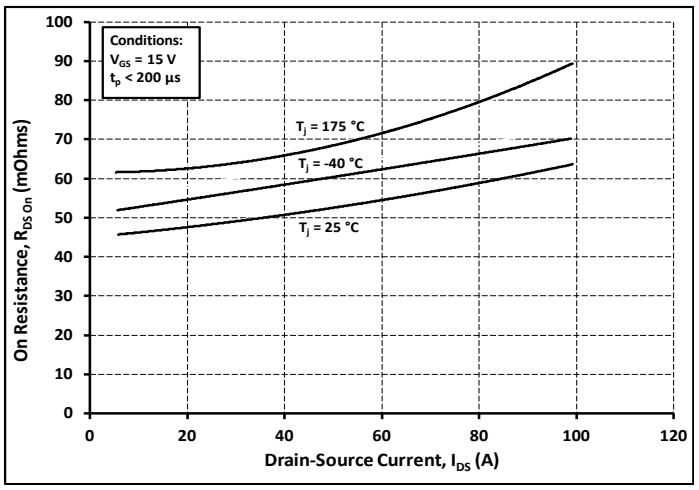


Figure 5. On-Resistance vs. Drain Current For Various Temperatures

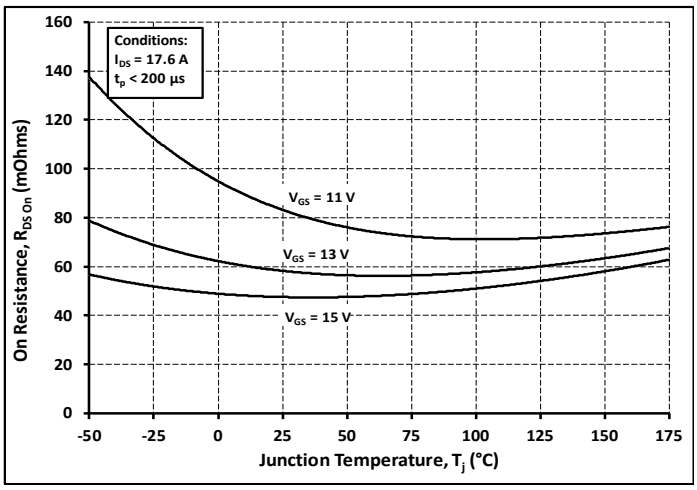


Figure 6. On-Resistance vs. Temperature For Various Gate Voltage

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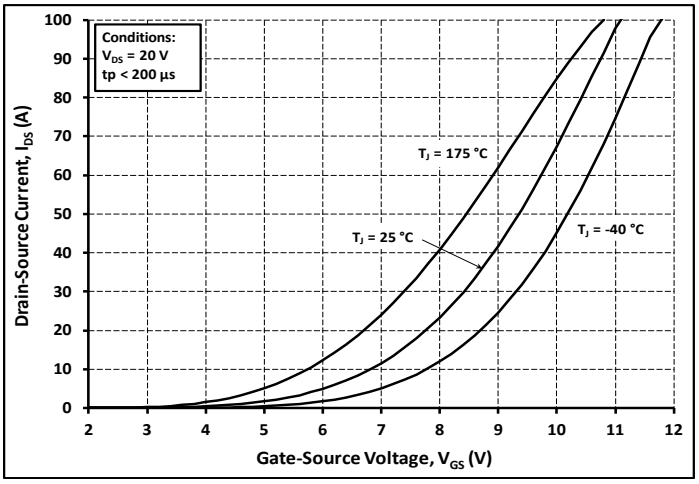


Figure 7. Transfer Characteristic for Various Junction Temperatures

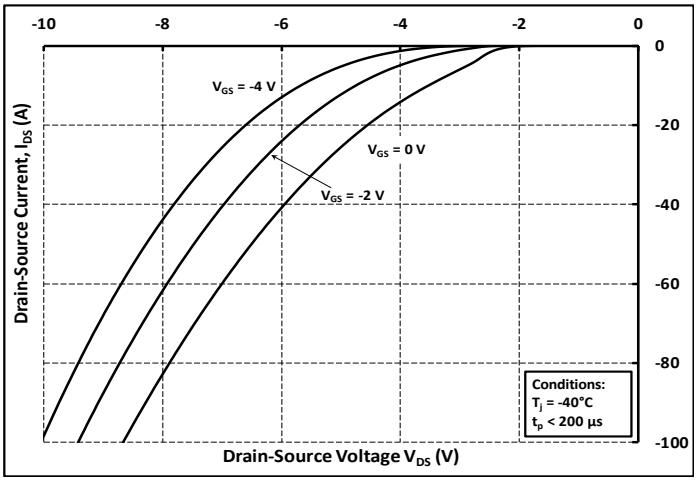


Figure 8. Body Diode Characteristic at -40°C

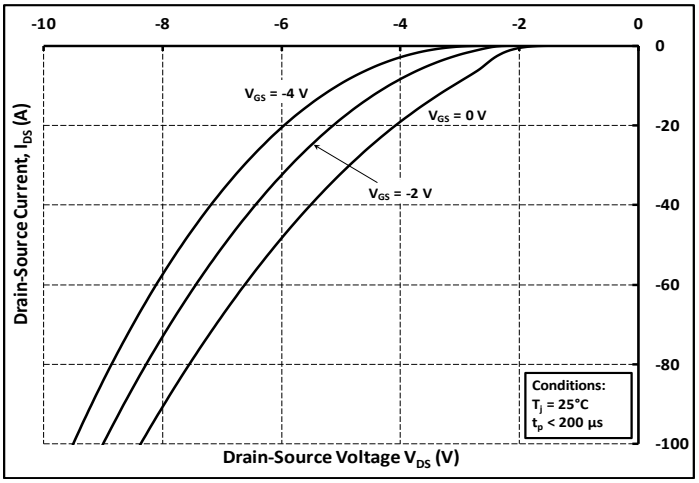


Figure 9. Body Diode Characteristic at 25°C

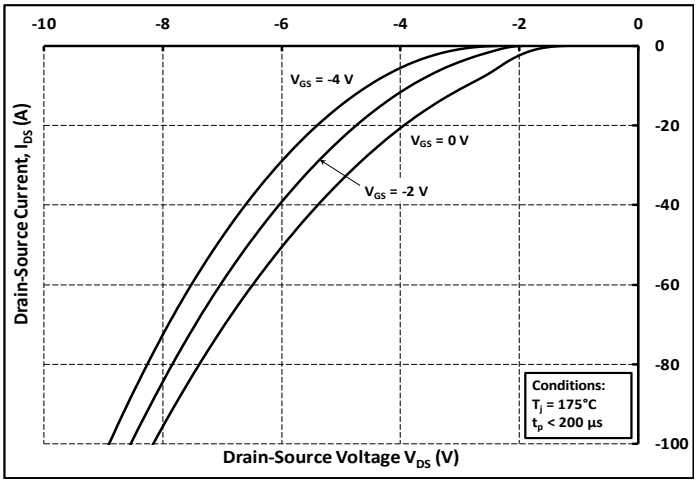


Figure 10. Body Diode Characteristic at 175°C

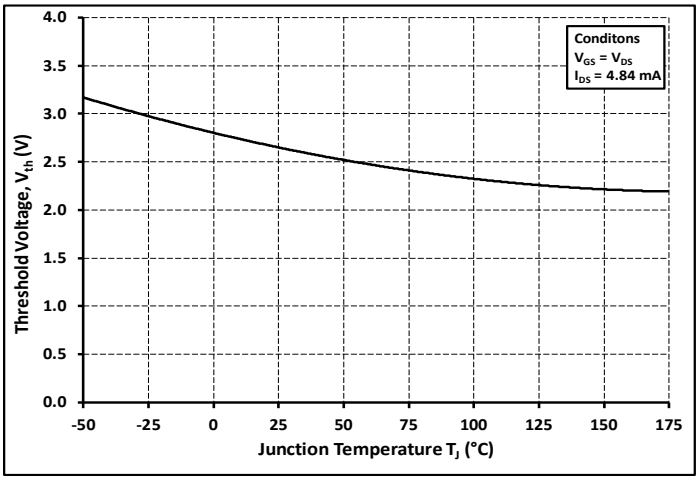


Figure 11. Threshold Voltage vs. Temperature

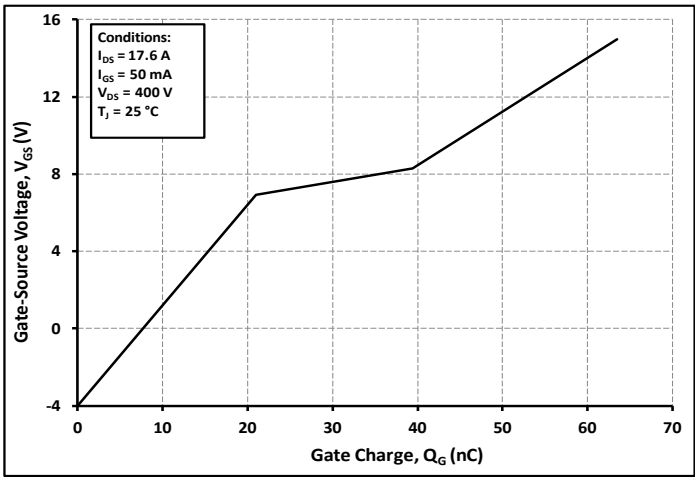


Figure 12. Gate Charge Characteristics

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Typical Performance

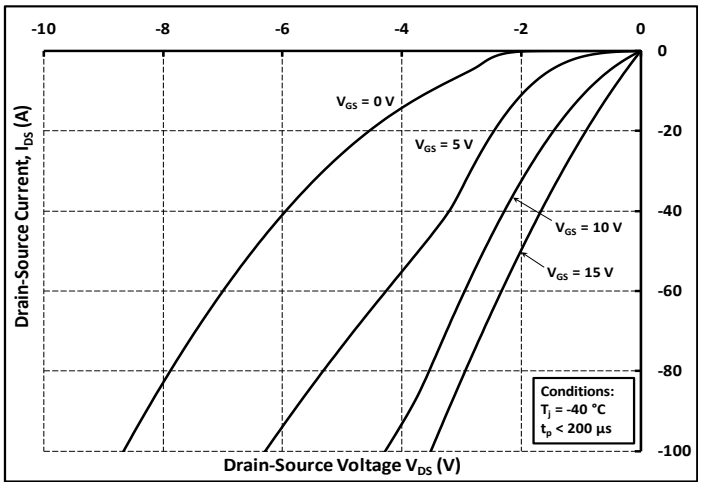


Figure 13. 3rd Quadrant Characteristic at -40°C

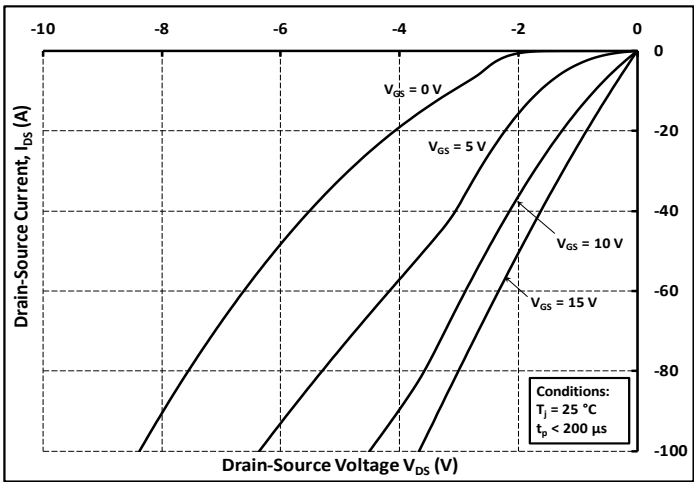


Figure 14. 3rd Quadrant Characteristic at 25°C

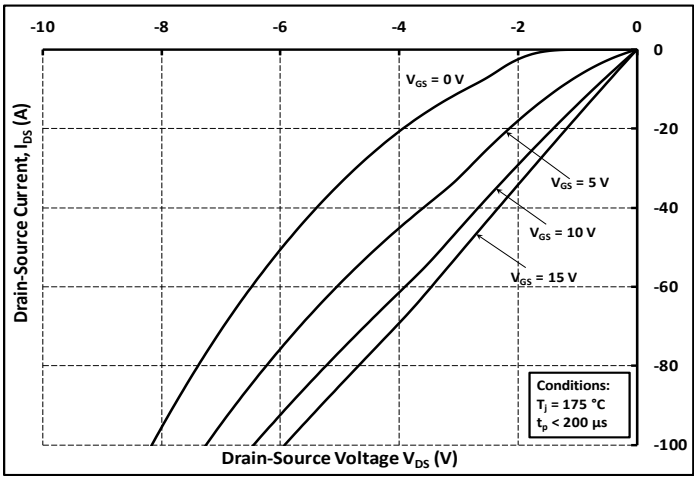


Figure 15. 3rd Quadrant Characteristic at 175°C

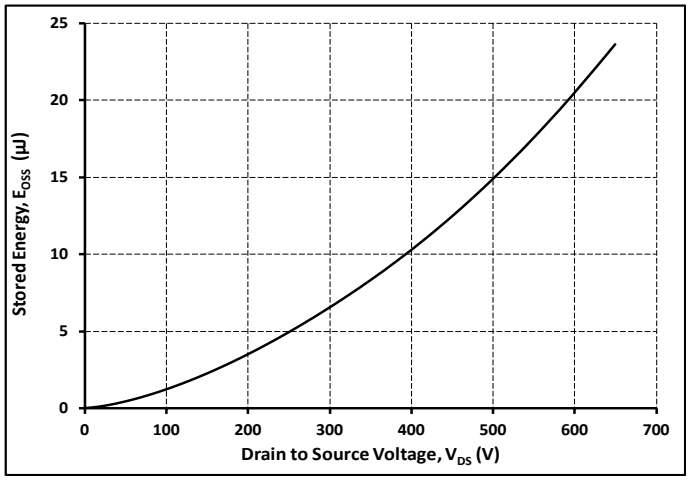


Figure 16. Output Capacitor Stored Energy

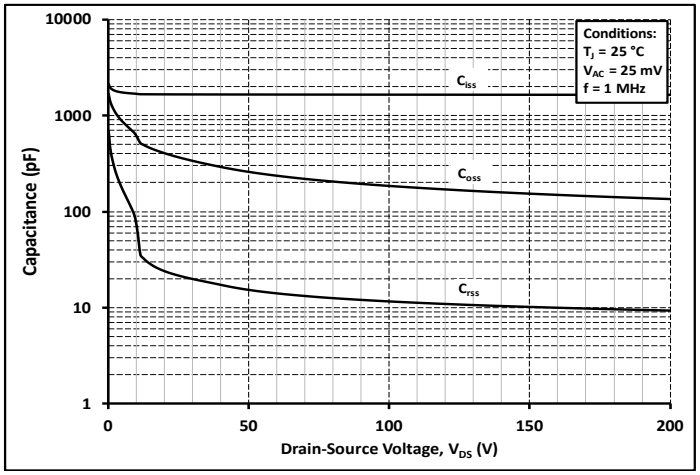


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

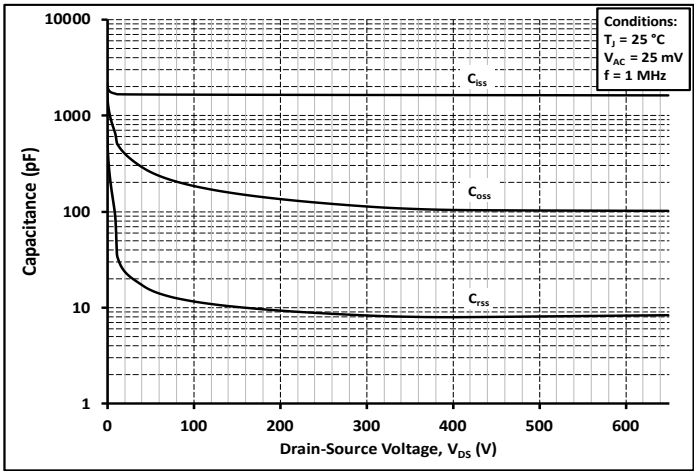


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 650V)

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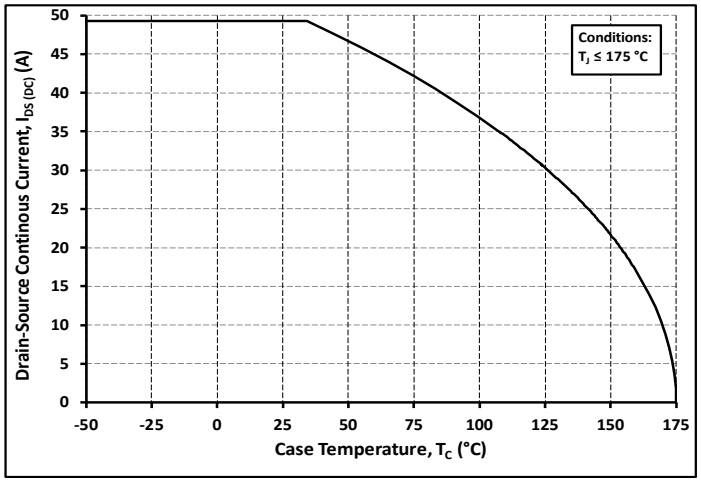


Figure 19. Continuous Drain Current Derating vs. Case Temperature

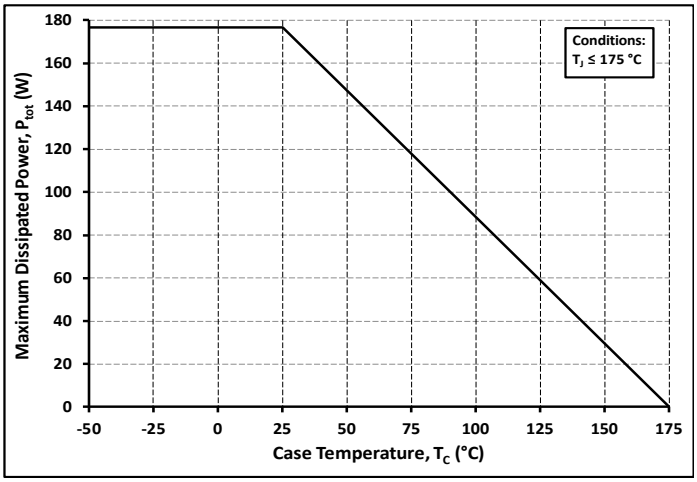


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

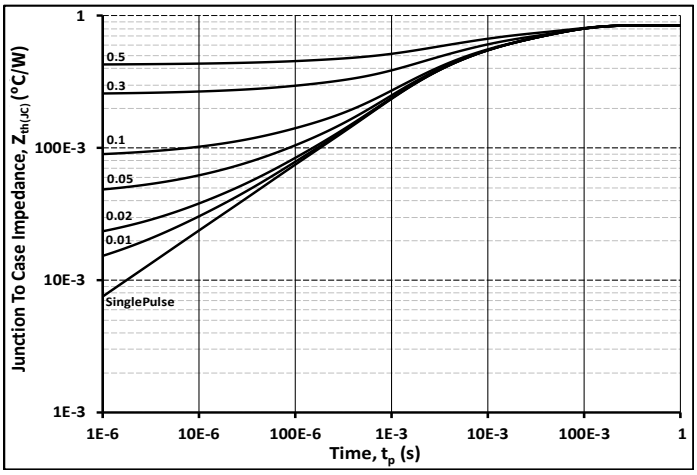


Figure 21. Transient Thermal Impedance (Junction - Case)

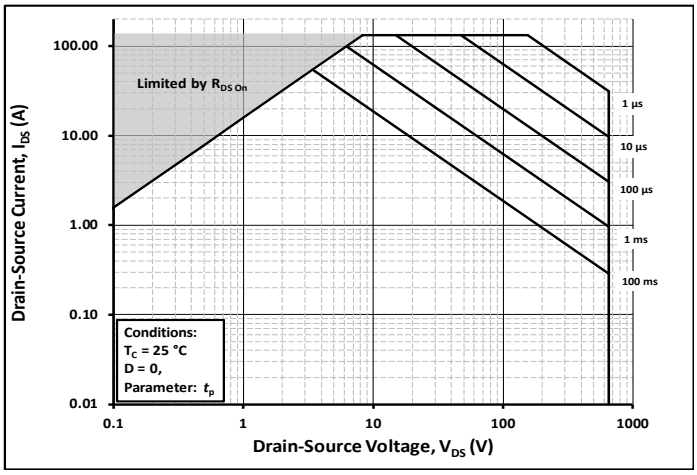


Figure 22. Safe Operating Area

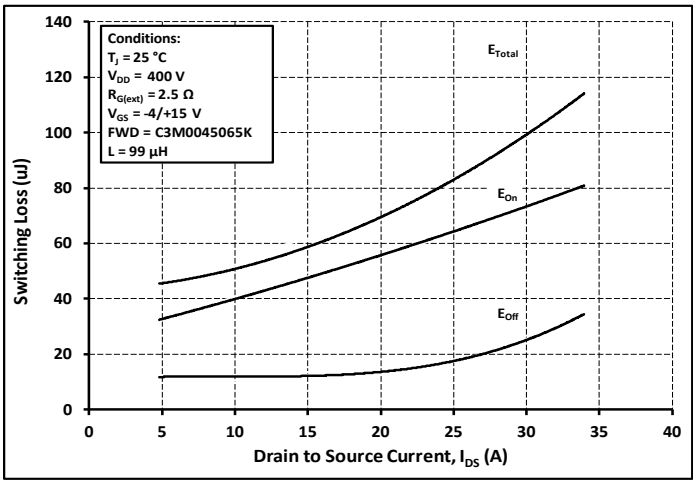


Figure 23. Clamped Inductive Switching Energy vs. Drain Current (V_{DD} = 400V)

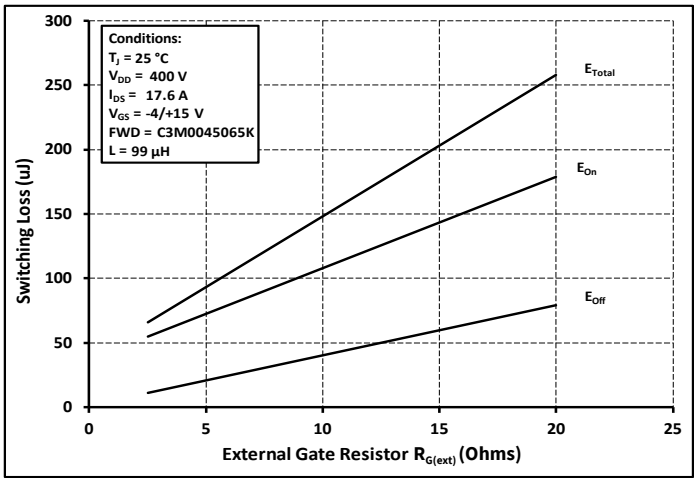


Figure 24. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

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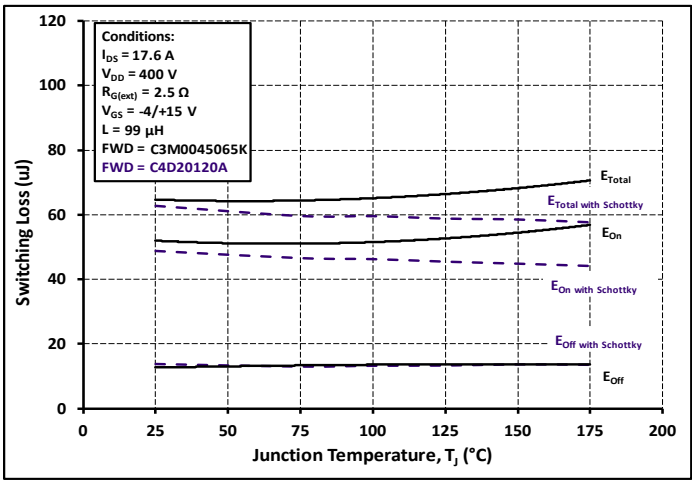


Figure 25. Clamped Inductive Switching Energy vs. Temperature

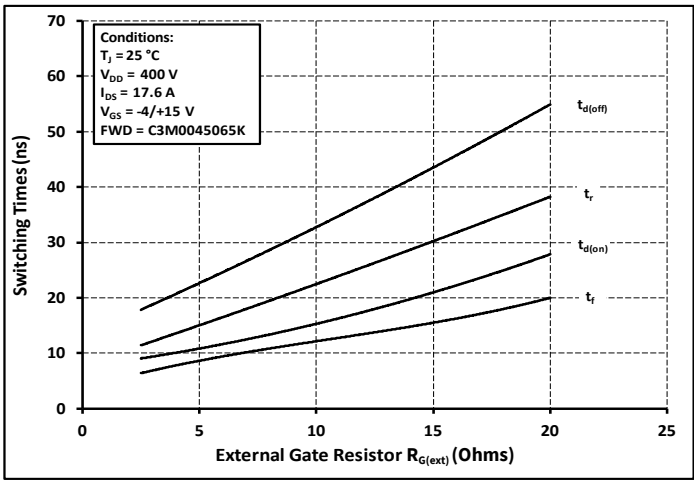


Figure 26. Switching Times vs. $R_{G(ext)}$

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Test Circuit Schematic

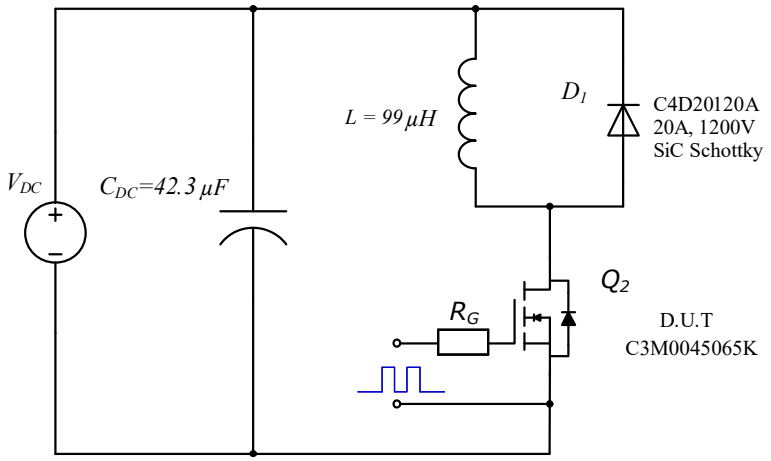


Figure 27. Clamped Inductive Switching Waveform Test Circuit

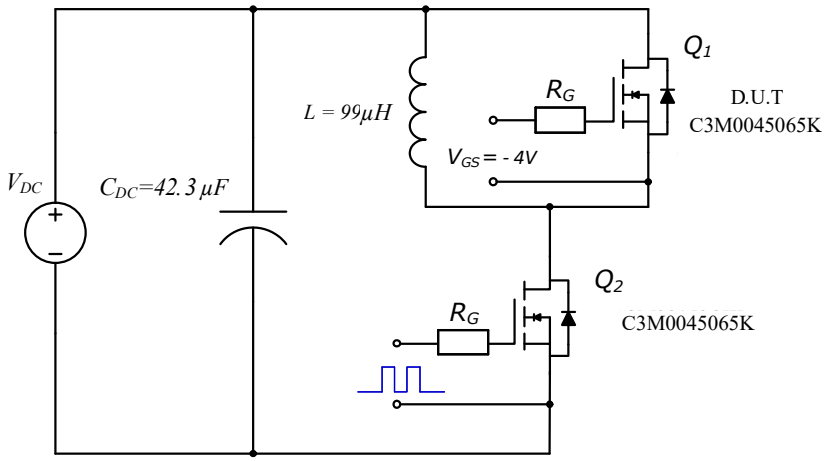
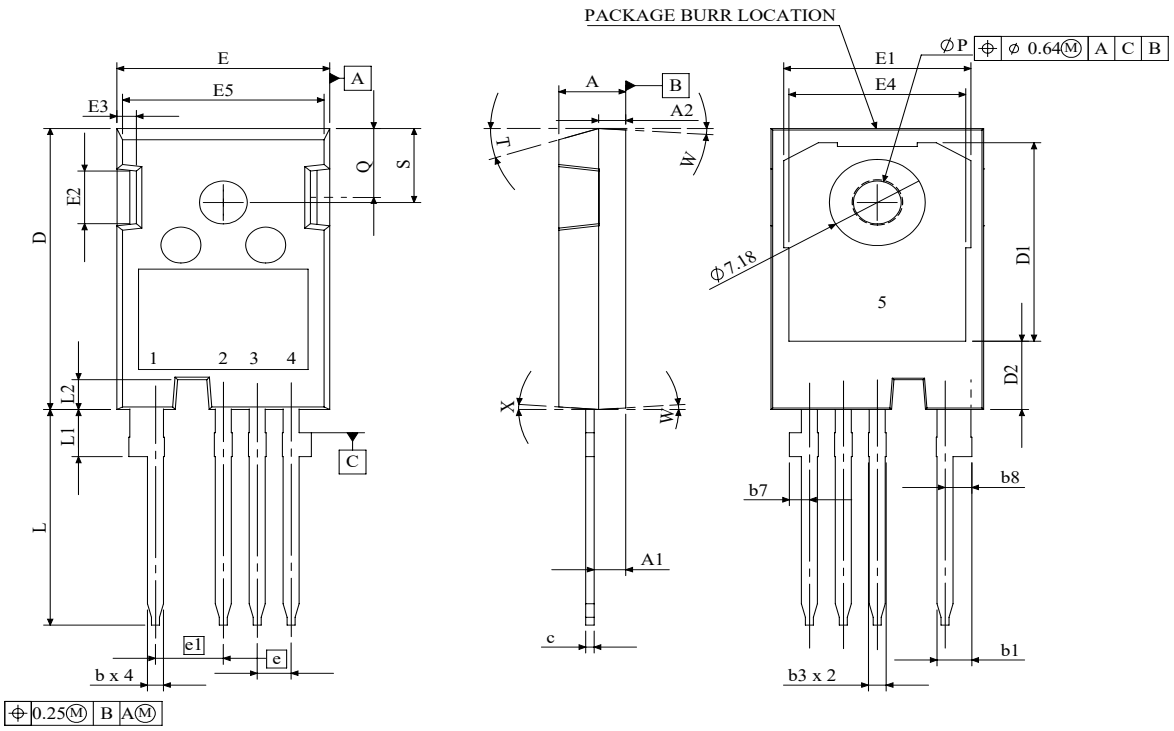


Figure 28. Body Diode Recovery Test Circuit

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Package Dimensions – Package TO-247-4L



SYMBOL	MIN (mm)	MAX (mm)
A	4.83	5.21
A1	2.23	2.54
A2	1.91	2.16
b	1.07	1.33
b1	2.39	2.94
b3	1.07	1.60
b7	1.30	1.70
b8	1.80	2.20
c	0.55	0.68
D	23.30	23.63
D1	16.25	17.65
D2	5.55	5.95
E	15.75	16.13
E1	13.1	14.15
E2	3.68	5.10
E3	1.00	1.90
E4	12.38	13.43
E5	14.65	15.05
e1	5.08 BSC	
L	17.31	17.82
L1	3.97	4.37
L2	2.35	2.65
ϕP	3.51	3.65
Q	5.49	6.00
S	6.04	6.30
T	17.5° REF.	
W	3.5° REF.	
X	4° REF.	

1	DRAIN
2	SOURCE
3	DRIVER SOURCE
4	GATE
5	DRAIN

NOTE:
1. ALL METAL SURFACES ARE TIN PLATED (MATTE), EXCEPT AREA OF CUT.
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
3. ALL DIMENSIONS ARE LISTED IN MILLIMETERS. ANGLES ARE IN DEGREES.
4. BURR OR MOLD FLASH SIZE (0.5 mm) IS NOT INCLUDED IN THE DIMENSIONS

Wolfspeed

TITLE: PACKAGE OUTLINE DRAWING: TO-247-4L

Date: 3/4/24

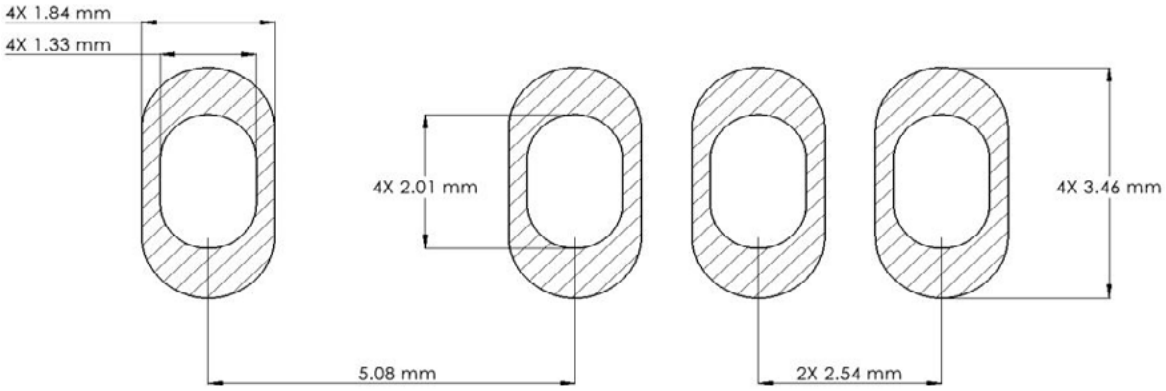
REVISION NO. 02

A4

PRD 05966 SCALE:1:1 SHEET 1 OF 1

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Recommended Solder Pad Layout



Revision History

Current Revision	Date of Release	Description of Changes
1	December-2020	N/A
2	November-2023	Not Released
3	December-2023	Updated Wolfspeed branding, package drawing, package image, and solder pad layout, added Revision History Table, Table 1 layout revised
4	September - 2024	Legal Disclaimer, POD, Diode Pulse Current Symbol

Related Links

- SPICE Models
- SiC MOSFET Isolated Gate Driver reference design
- SiC MOSFET Evaluation Board

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