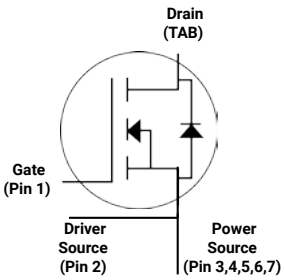
C3M0060065J

Silicon Carbide Power MOSFET C3M™ MOSFET Technology
N-Channel Enhancement Mode





RoHS

Halogen-Free

Features

- 3rd Generation SiC MOSFET technology
- Low inductance package with driver source pin
- 7mm of creepage distance between drain and source
- High blocking voltage with low on-resistance
- High speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery (Q_{rr})
- Halogen free, RoHS compliant

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Ordering Part Number	Package	Marking
C3M0060065J	TO-263-7	C3M0060065J

Typical Applications

- EV charging
- Server power supplies
- Solar PV inverters
- UPS
- DC/DC converters

Benefits

- Higher system efficiency
- Reduced cooling requirements
- Increased power density
- Increased system switching frequency
- Easy to parallel and simple to drive
- Enable new hard switching PFC topologies (Totem-Pole)

Key Parameters

Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions	Note
Drain - Source Voltage	V_{DS}			650	v	T_C = 25°C	
Maximum Gate - Source Voltage	$V_{GS(max)}$	-8		+19		Transient	
Operational Gate-Source Voltage	$V_{GS\ op}$		-4/15			Static	Note 1
DC Continuous Drain Current	I_D			36	A	V_{GS} = 15 V, T_C = 25 °C, T_J ≤175 °C	Fig. 19 Note 2
				26		V_{GS} = 15 V, T_C = 100 °C, T_J ≤175 °C	
Pulsed Drain Current	I_{DM}			99		t_{Pmax} limited by T_{jmax} V_{GS} = 15V, T_C = 25 °C	Fig. 22
Power Dissipation	P_D			136	W	T_C = 25 °C, T_J = 175 °C	Fig. 20
Operating Junction and Storage Temperature	T_J, T_{stg}			-40 to +175	°C		
Solder Temperature	T_L			260		According to JEDEC J-STD-020	

Note (1): Recommended turn-on gate voltage is 15V with ±5% regulation tolerance, see Application Note PRD-04814 for additional details
Note (2): Verified by design

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Electrical Characteristics (T_C = 25℃ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Note
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	650	—	—	V	V_{GS} = 0 V, I_D = 100 µA	
Gate Threshold Voltage	$V_{GS(th)}$	1.8	2.3	3.6	V	V_{DS} = V_{GS}, I_D = 5 mA	Fig. 11
		—	1.9	—		V_{DS} = V_{GS}, I_D = 5 mA, T_J = 175℃	
Zero Gate Voltage Drain Current	I_{DSS}	—	1	50	µA	V_{DS} = 650 V, V_{GS} = 0 V	
Gate-Source Leakage Current	I_{GSS}	—	10	250	nA	V_{GS} = 15 V, V_{DS} = 0 V	
Drain-Source On-State Resistance	$R_{DS(on)}$	—	60	79	mΩ	V_{GS} = 15 V, I_D = 13.2 A	Fig. 4, 5, 6
		—	80	—		V_{GS} = 15 V, I_D = 13.2 A, T_J = 175°C	
Transconductance	g_{fs}	—	10	—	S	V_{DS} = 20 V, I_{DS} = 13.2 A	Fig. 7
			9			V_{DS} = 20 V, I_{DS} = 13.2 A, T_J = 175°C	
Input Capacitance	C_{iss}	—	1020	—	pF	V_{GS} = 0 V, V_{DS} = 600 V f = 1 Mhz V_{AC} = 25 mV	Fig. 17, 18
Output Capacitance	C_{oss}	—	80	—			
Reverse Transfer Capacitance	C_{rss}	—	9	—			
Effective Output Capacitance (Energy Related)	$C_{o(er)}$	—	95	—		V_{GS} = 0 V, V_{DS} = 0 V to 400 V	Note 3
Effective Output Capacitance (Time Related)	$C_{o(tr)}$	—	132	—			
C_{oss} Stored Energy	E_{oss}	—	15	—	µJ	V_{DS} = 600 V, f = 1 Mhz	Fig. 16
Turn-On Switching Energy (Body Diode)	E_{on}	—	41	—		V_{DS} = 400 V, V_{GS} = -4 V/15 V, I_D = 13.2 A, $R_{G(ext)}$ = 2.5 Ω, L= 135 µH, T_J = 175°C FWD = Internal Body Diode of MOSFET	Fig. 25
Turn Off Switching Energy (Body Diode)	E_{off}	—	5	—			
Turn-On Delay Time	$t_{d(on)}$	—	9	—	ns	V_{DD} = 400 V, V_{GS} = -4 V/15 V I_D = 13.2 A, $R_{G(ext)}$ = 2.5 Ω, L= 135 µH Timing relative to V_{DS} Inductive load	Fig. 26
Rise Time	t_r	—	8	—			
Turn-Off Delay Time	$t_{d(off)}$	—	17	—			
Fall Time	t_f	—	6	—			
Internal Gate Resistance	$R_{G(int)}$	—	3	—	Ω	f = 1 MHz, V_{AC} = 25 mV	
Gate to Source Charge	Q_{gs}	—	14	—	nC	V_{DS} = 400 V, V_{GS} = -4 V/15 V I_D = 13.2 A Per IEC60747-8-4 pg 21	Fig. 12
Gate to Drain Charge	Q_{gd}	—		—			
Total Gate Charge	Q_g	—	46	—			

Note:
[3] $C_{o(er)}$, a lumped capacitance that gives same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V
$C_{o(tr)}$, a lumped capacitance that gives same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

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Reverse Diode Characteristics (T_C = 25°C unless otherwise specified)

Parameter	Symbol	Typ.	Max.	Unit	Test Conditions	Notes
Diode Forward Voltage	V_{SD}	5.1	—	V	V_{GS} = -4 V, I_{SD} = 6.6 A, T_J = 25°C	Fig. 8, 9, 10
		4.8	—		V_{GS} = -4 V, I_{SD} = 6.6 A, T_J = 175°C	
Continuous Diode Forward Current	I_S	—	21	A	V_{GS} = -4 V, T_C = 25°C	
Diode pulse Current	$I_{S,\ pulse}$	—	99		V_{GS} = -4 V, pulse width t_P limited by T_{jmax}	
Reverse Recovery Time	t_{rr}	8	—	ns	V_{GS} = -4 V, I_{SD} = 13.2 A, V_R = 400 V di_F/dt = 3600 A/µs, T_J = 175°C	
Reverse Recovery Charge	Q_{rr}	75	—	nC		
Peak Reverse Recovery Current	I_{RRM}	15	—	A		
Reverse Recovery Time	t_{rr}	10	—	ns	V_{GS} = -4 V, I_{SD} = 13.2 A, V_R = 400 V di_F/dt = 2300 A/µs, T_J = 175°C	
Reverse Recovery Charge	Q_{rr}	62	—	nC		
Peak Reverse Recovery Current	I_{RRM}	10	—	A		

Thermal Characteristics

Parameter	Symbol	Typ.	Unit	Note
Thermal Resistance from Junction to Case	$R_{\theta JC}$	1.1	°C/W	Fig. 21
Thermal Resistance From Junction to Ambient	$R_{\theta JA}$	40		

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Typical Performance

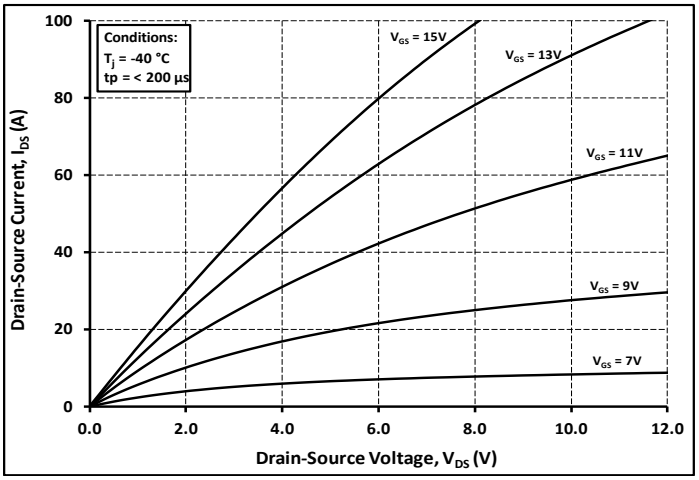


Figure 1. Output Characteristics T_J = -40°C

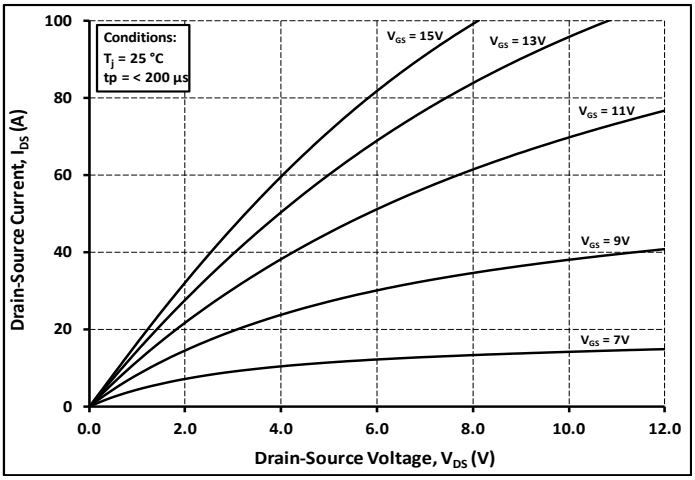


Figure 2. Output Characteristics T_J = 25°C

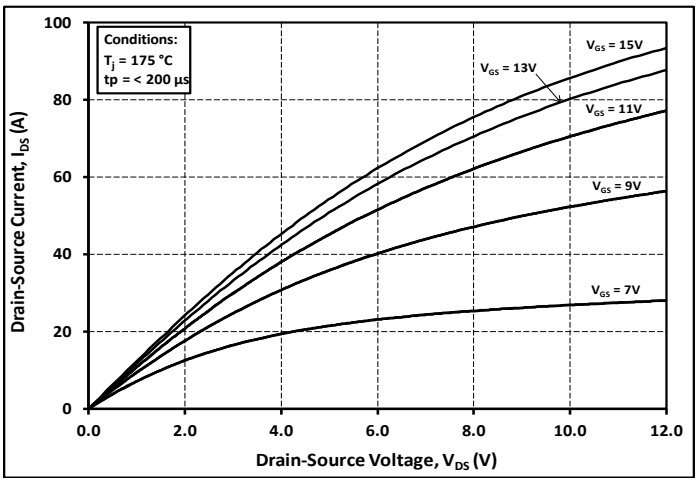


Figure 3. Output Characteristics T_J = 175°C

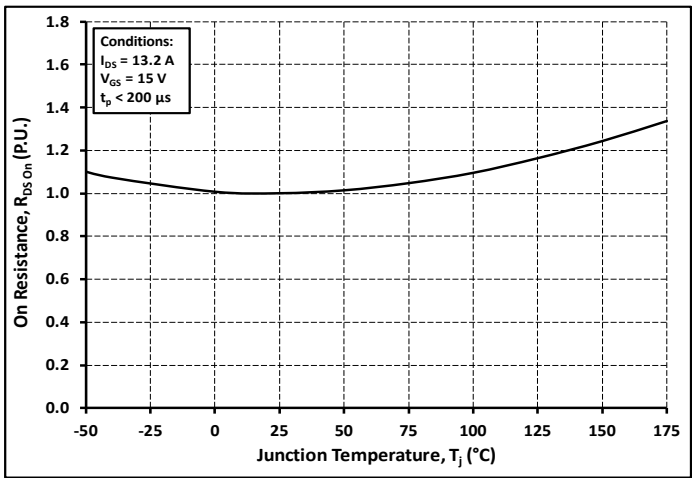


Figure 4. Normalized On-Resistance vs. Temperature

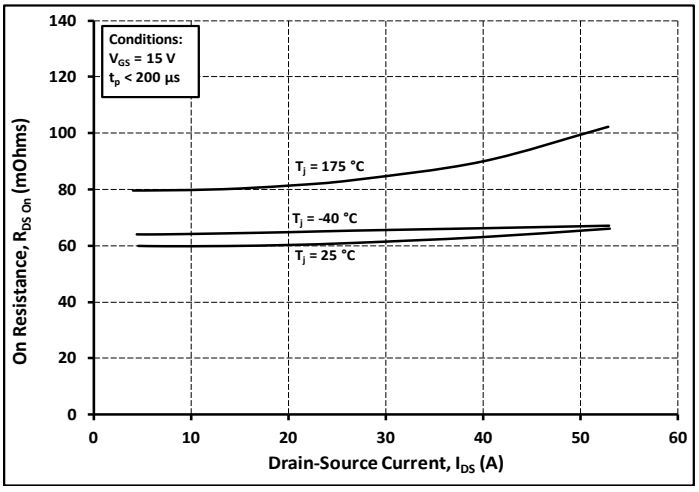


Figure 5. On-Resistance vs. Drain Current
For Various Temperatures

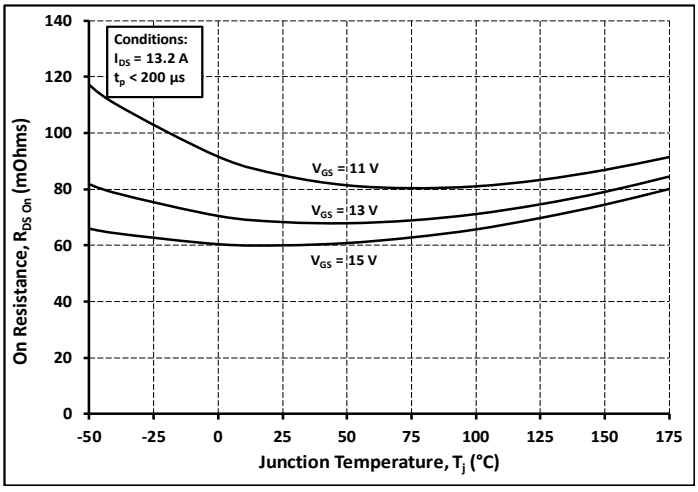


Figure 6. On-Resistance vs. Temperature
For Various Gate Voltage

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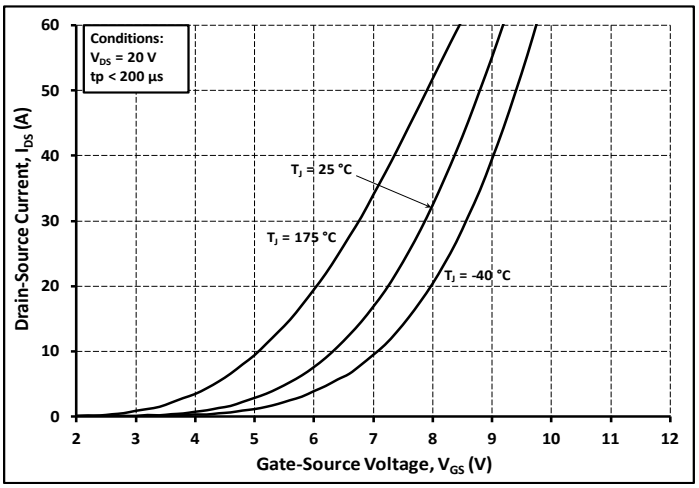


Figure 7. Transfer Characteristic for Various Junction Temperatures

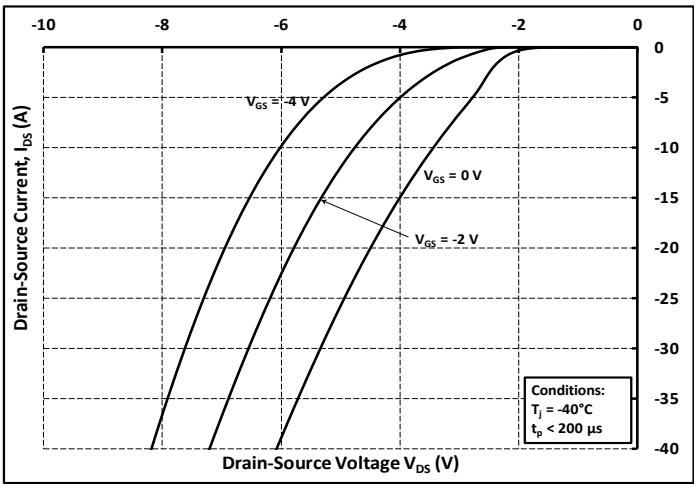


Figure 8. Body Diode Characteristic at -40°C

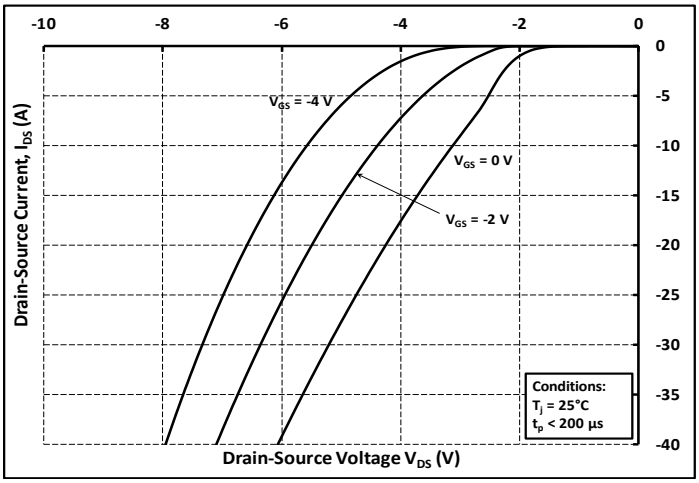


Figure 9. Body Diode Characteristic at 25°C

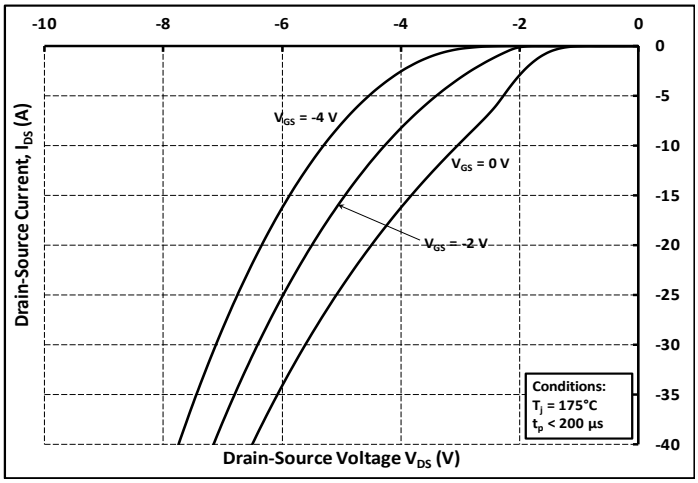


Figure 10. Body Diode Characteristic at 175°C

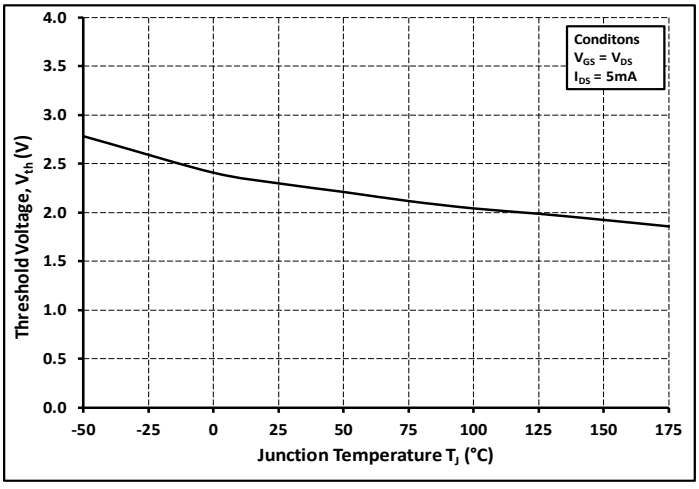


Figure 11. Threshold Voltage vs. Temperature

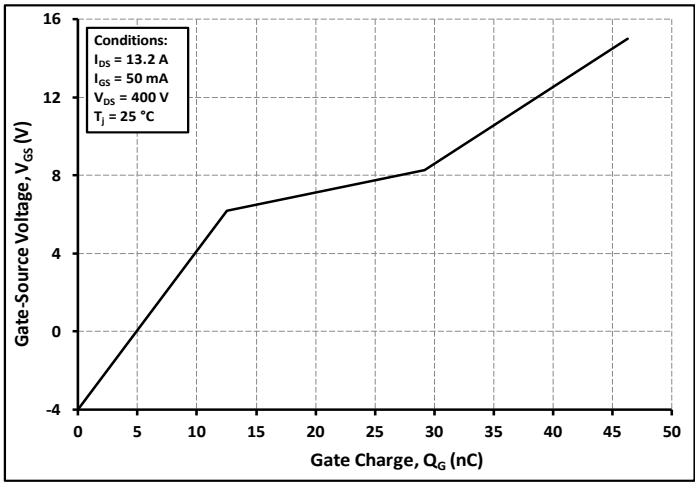


Figure 12. Gate Charge Characteristics

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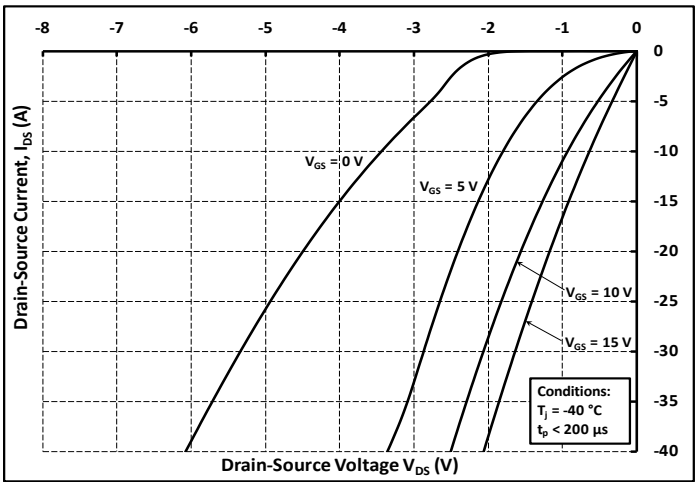


Figure 13. 3rd Quadrant Characteristic at -40°C

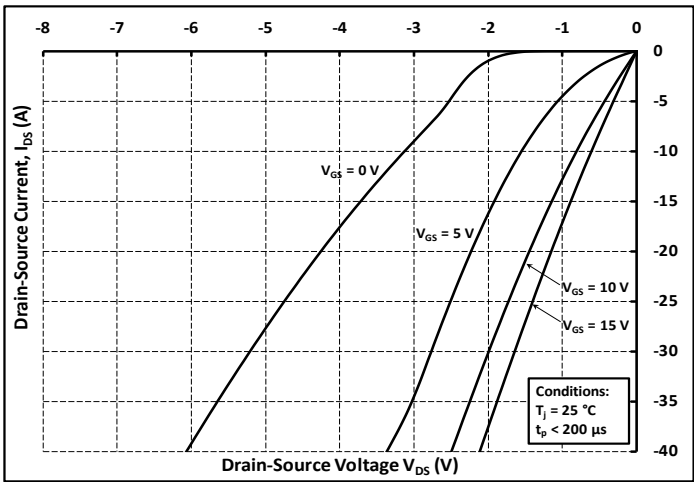


Figure 14. 3rd Quadrant Characteristic at 25°C

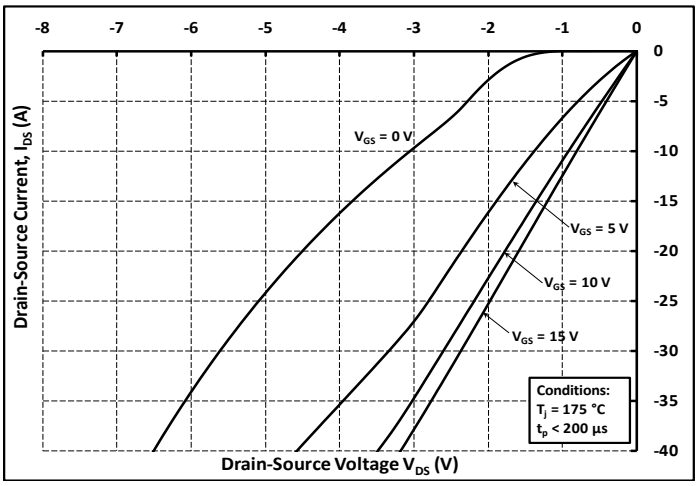


Figure 15. 3rd Quadrant Characteristic at 175°C

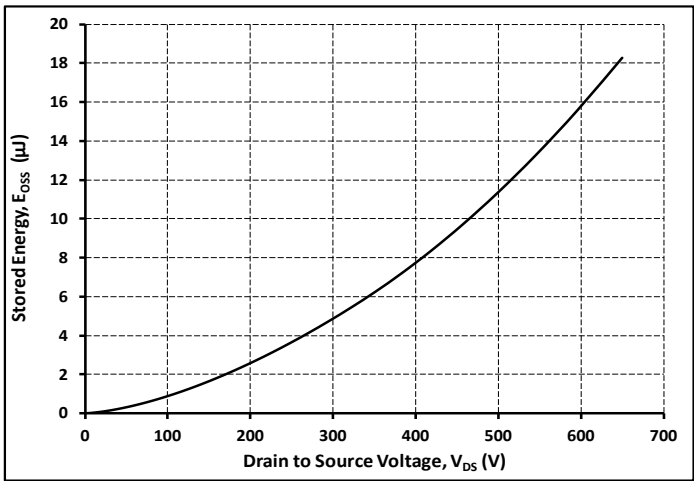


Figure 16. Output Capacitor Stored Energy

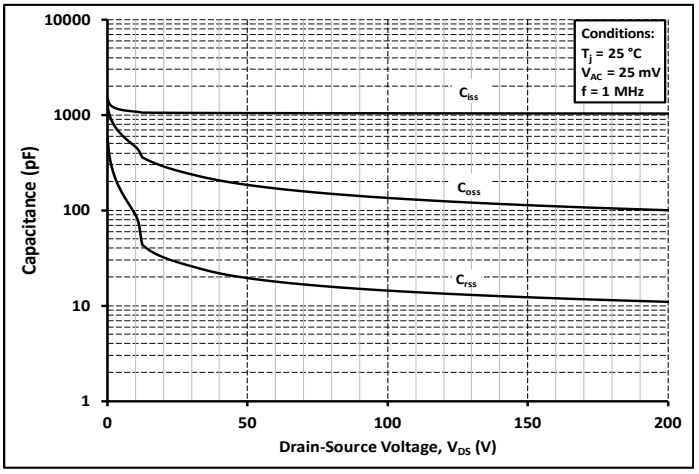


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200 V)

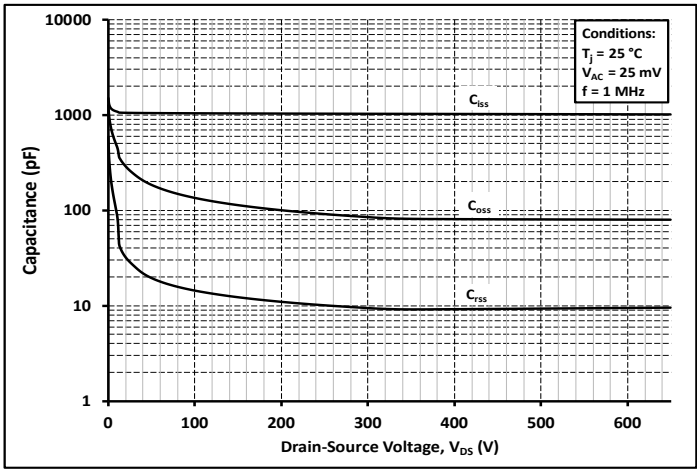


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 650 V)

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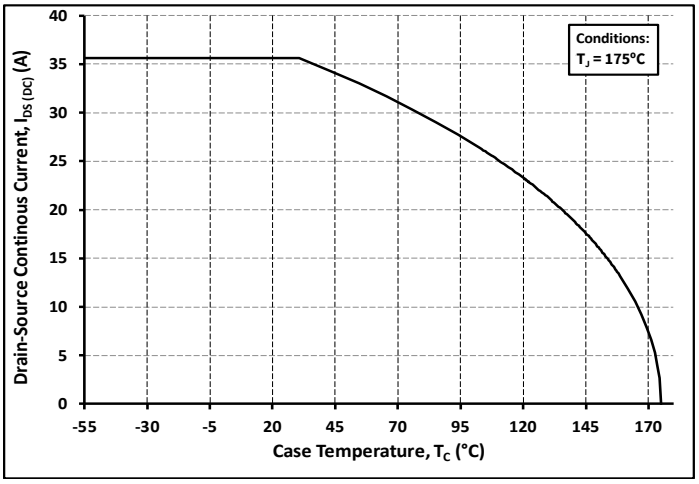


Figure 19. Continuous Drain Current Derating vs. Case Temperature

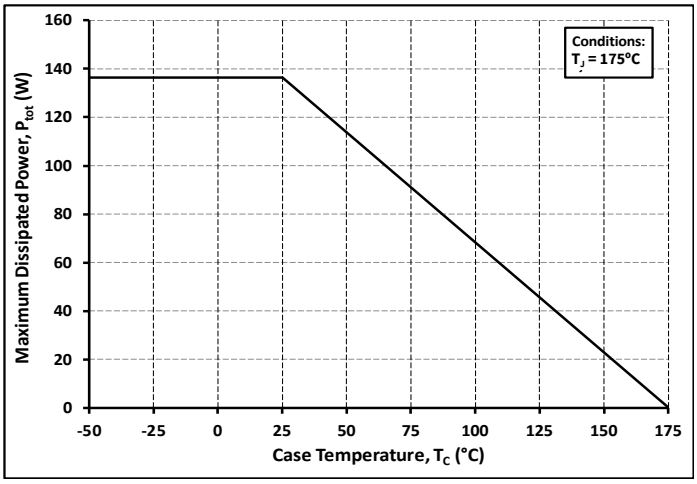


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

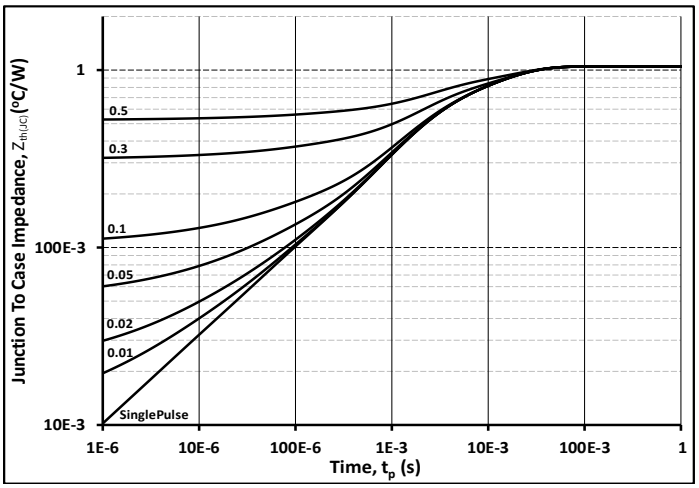


Figure 21. Transient Thermal Impedance (Junction - Case)

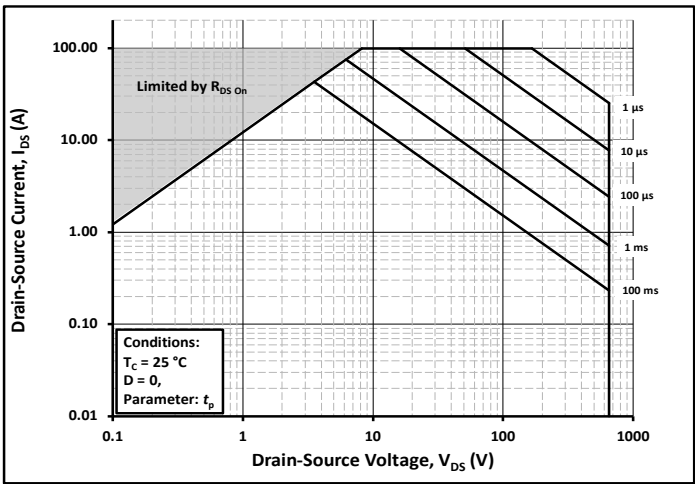


Figure 22. Safe Operating Area

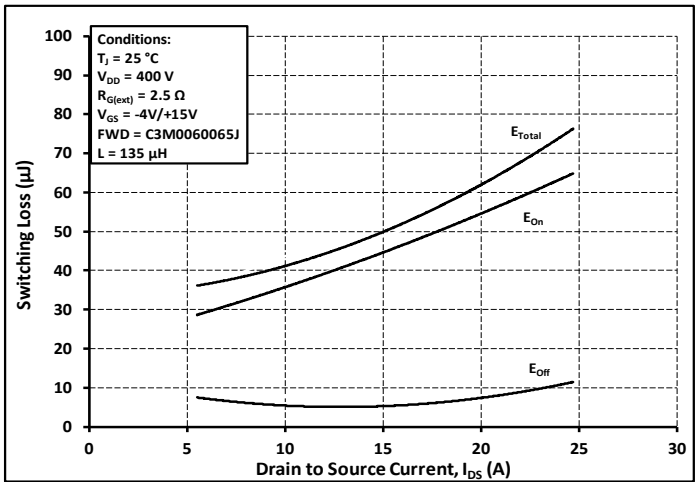


Figure 23. Clamped Inductive Switching Energy vs. Drain Current (V_{DD} = 400 V)

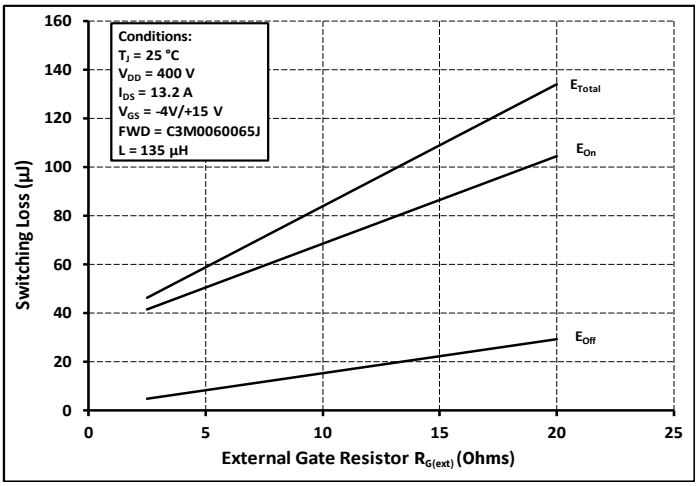


Figure 24. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

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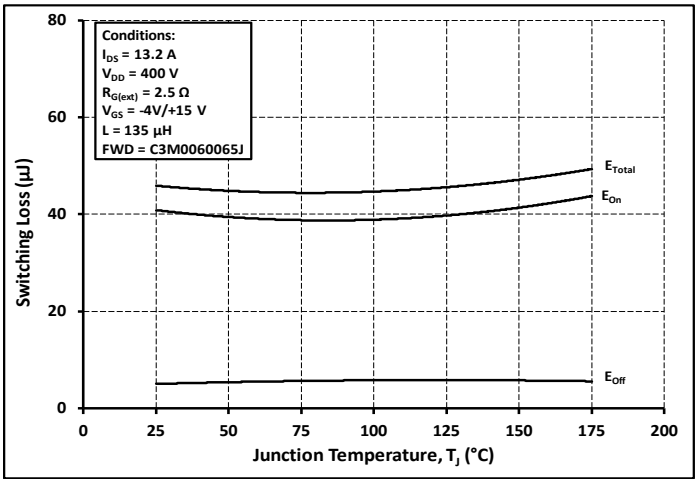


Figure 25. Clamped Inductive Switching Energy vs. Temperature

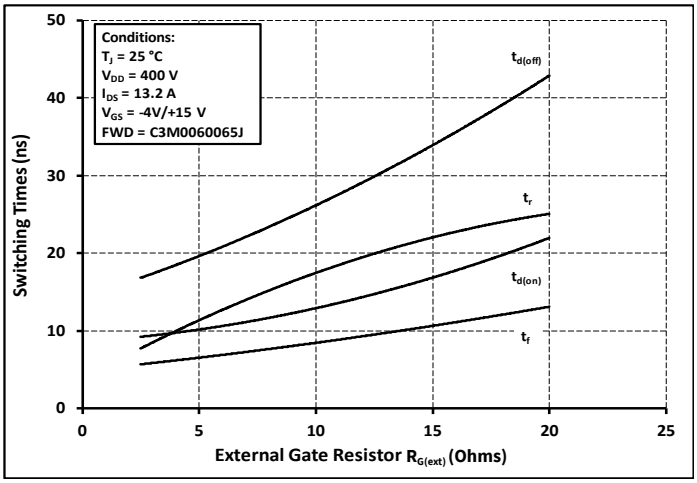


Figure 26. Switching Times vs. $R_{G(ext)}$

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Test Circuit Schematic

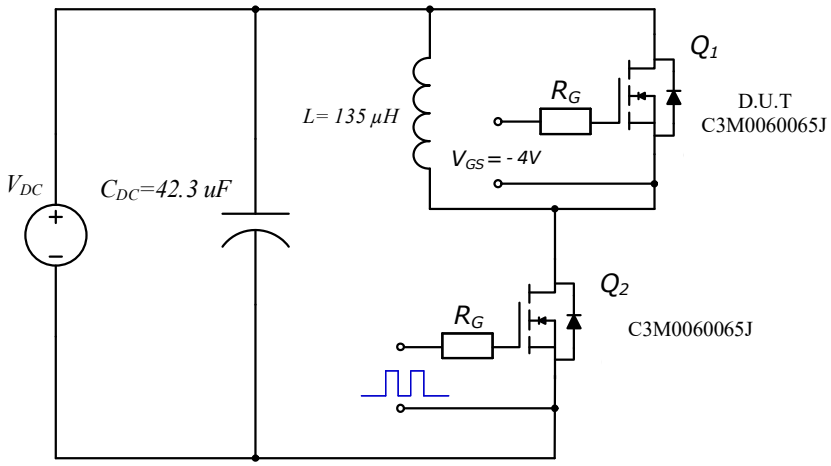
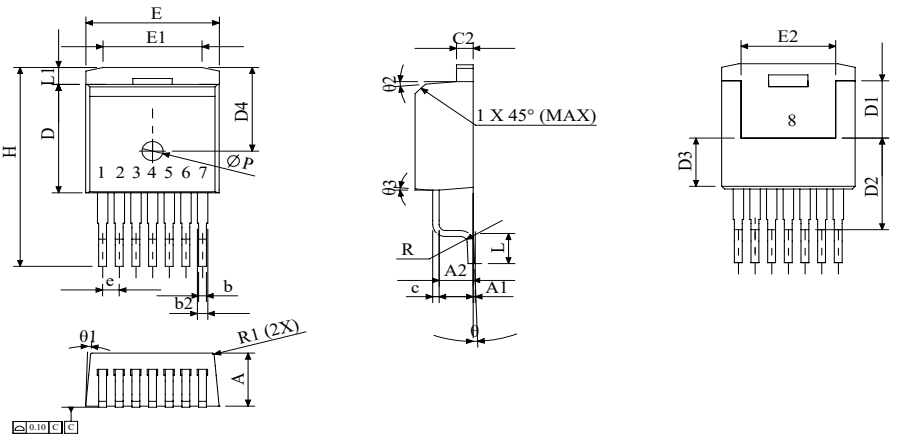


Figure 27. Clamped Inductive Switching Waveform Test Circuit

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Package Dimensions – TO-247-7L D2PAK



SYMBOL	MIN (mm)	MAX (mm)
A	4.30	4.57
A1	0.00	0.25
b	0.50	0.70
b2	0.60	1.00
c	0.33	0.65
C2	1.17	1.40
D	9.025	9.125
D1	4.70	4.90
D2	7.170 REF	
D3	4.000 REF	
D4	7.000 REF	
A2	2.595 REF	
E	10.13	10.23
E1	6.50	8.60
E2	6.778	7.665
e	1.27 TYP	
H	15.043	17.313
L	2.324	2.700
L1	0.968	1.868
R	0.506 REF	
R1	0.500 REF	
θ	0°	8°
θ1	4.5°	5.5°
θ2	4°	6°
θ3	4°	6°

1	GATE
2	KELVIN
3	SOURCE
4	
5	
6	
7	
8	DRAIN

NOTE
1. ALL METAL SURFACES ARE TIN PLATED (MATTE), EXCEPT AREA OF CUT.
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
3. ALL DIMENSIONS ARE LISTED IN MILLIMETERS. ANGLES ARE IN DEGREES.
4. PACKAGE BURR FLASH SIZE (0.5 mm) IS NOT INCLUDED IN THE DIMENSIONS

Wolfspeed

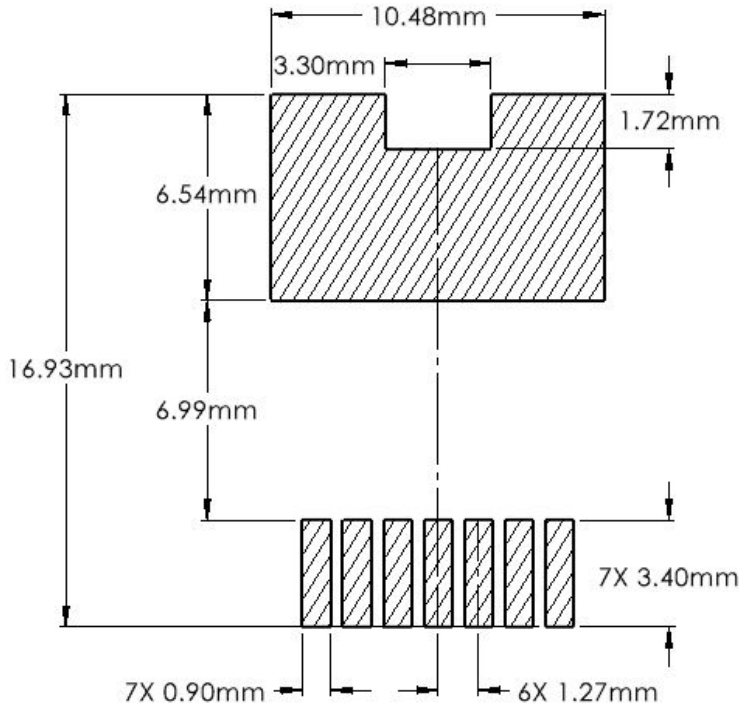
TITLE: PACKAGE OUTLINE DRAWING: TO 263-7L J

REVISION NO. 02 | A4

Date: 08/12/25 | PRD-05972 | SCALE:1:1 | SHEET 1 OF 1

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Recommended Solder Pad Layout



Revision History

Current Revision	Date of Release	Description of Changes
3	July-2020	N/A
4	December-2023	Updated Wolfspeed branding, package drawing, package image, solder pad layout, added Rev history, Table 1 layout revised
5	March-2024	RDSON LSL Removed
6	December - 2024	Legal Disclaimer Updated
7	September - 2025	Package drawing updated to correct dimension D1

Related Links

- SPICE Models
- SiC MOSFET Isolated Gate Driver reference design
- SiC MOSFET Evaluation Board

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