C3M0060075K1

Silicon Carbide Power MOSFET
N-Channel Enhancement Mode

Features

- Optimized package with separate driver source pin
- Lower profile TO-247-4 package body
- High blocking voltage with low on-resistance
- High-speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery (Q_{rr})
- Halogen free, RoHS compliant

Benefits

- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Reduce cooling requirements
- Increase power density
- Increase system switching frequency

Typical Applications

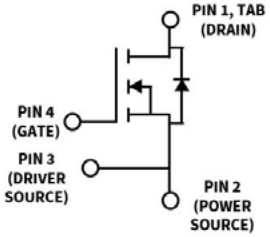
- Motor Control
- EV Battery Chargers
- High Voltage DC/DC Converters
- Solar/ESS
- UPS
- Battery Voltage Range 400V-550V
- Enterprise PSU

Package



Halogen-Free

RoHS compliant



Part Number	Package	Marking
C3M0060075K1	TO-247-4L LP	C3M0060075K1

Key Parameters

Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions	Note
Drain - Source Voltage	V_{DS}			750	v	T_C = 25°C	
Maximum Gate - Source Voltage	$V_{GS(max)}$	-8		+19		Transient	
Operational Gate-Source Voltage	$V_{GS\,op}$		-4/15			Static	Note 1
DC Continuous Drain Current	I_D			35	A	V_{GS} = 15 V, T_C = 25 °C, T_J ≤175 °C	Fig. 19 Note 2
				26		V_{GS} = 15 V, T_C = 100 °C, T_J ≤175 °C	
Pulsed Drain Current	I_{DM}			101		t_{Pmax} limited by T_{jmax} V_{GS} = 15V, T_C = 25 °C	Fig. 22
Power Dissipation	P_D			126	W	T_C = 25 °C, T_J = 175 °C	Fig. 20
Operating Junction and Storage Temperature	T_J, T_{stg}			-40 to +175	°C		
Solder Temperature	T_L			260		According to JEDEC J-STD-020	
Mounting Torque	M_D			1 8.8	Nm lbf-in	M3 or 6-32 screw	

Note (1): Recommended turn-on gate voltage is 15V with ±5% regulation tolerance, see Application Note PRD-04814 for additional details
Note (2): Verified by design

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Electrical Characteristics (T_C = 25˚C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	750			V	V_{GS} = 0 V, I_D = 100 µA	
$V_{GS(th)}$	Gate Threshold Voltage	1.8	2.6	3.8	V	V_{DS} = V_{GS}, I_D = 3.67 mA	Fig. 11
			2.1		V	V_{DS} = V_{GS}, I_D = 3.67 mA, T_J = 175ºC	
I_{DSS}	Zero Gate Voltage Drain Current		1	50	µA	V_{DS} = 750 V, V_{GS} = 0 V	
I_{GSS}	Gate-Source Leakage Current		10	250	nA	V_{GS} = 15 V, V_{DS} = 0 V	
$R_{DS(on)}$	Drain-Source On-State Resistance		60	78	mΩ	V_{GS} = 15 V, I_D = 13.4 A	Fig. 4, 5, 6
			87			V_{GS} = 15 V, I_D = 13.4 A, T_J = 175ºC	
g_{fs}	Transconductance		10		S	V_{DS}= 20 V, I_{DS}= 13.4 A	Fig. 7
			8			V_{DS}= 20 V, I_{DS}= 13.4 A, T_J = 175ºC	
C_{iss}	Input Capacitance		1203		pF	V_{GS} = 0 V, V_{DS} = 0V to 500 V F = 100 kHz V_{AC} = 25 mV	Fig. 17, 18
C_{oss}	Output Capacitance		69				
C_{rss}	Reverse Transfer Capacitance		7				
E_{oss}	C_{oss} Stored Energy		10		µJ		Fig. 16
$C_{o(er)}$	Effective Output Capacitance (Energy Related)		90		pF	V_{GS} = 0 V, V_{DS} = 0... 500V	Note: 3
$C_{o(tr)}$	Effective Output Capacitance (Time Related)		129		pF		
E_{ON}	Turn-On Switching Energy (External Diode)		52		µJ	V_{DS}= 500 V, V_{GS}= -4 V/15 V, I_D= 13.4 A, $R_{G(ext)}$ = 2.5 Ω, L= 135 µH, T_J = 175ºC FWD = External SiC DIODE	Fig. 26, 28
E_{OFF}	Turn Off Switching Energy (External Diode)		16				
E_{ON}	Turn-On Switching Energy (Body Diode FWD)		56		µJ	V_{DS}= 500 V, V_{GS}= -4 V/15 V, I_D= 13.4 A, $R_{G(ext)}$ = 2.5 Ω, L= 135 µH, T_J = 175ºC FWD = Internal Body Diode	Fig. 26, 28
E_{OFF}	Turn-Off Switching Energy (Body Diode FWD)		16				
$t_{d(on)}$	Turn-On Delay Time		8		ns	V_{DD} = 500 V, V_{GS} = -4 V/15 V I_D = 13.4 A, $R_{G(ext)}$ = 2.5 Ω, Timing relative to V_{DS} Inductive load	Fig. 27, 28
t_r	Rise Time		9				
$t_{d(off)}$	Turn-Off Delay Time		16				
t_f	Fall Time		9				
$R_{G(int)}$	Internal Gate Resistance		3.0		Ω	f = 1 MHz, V_{AC} = 25 mV	
Q_{gs}	Gate to Source Charge		14		nC	V_{DS} = 500 V, V_{GS} = -4 V/15 V I_D = 13.4 A Per IEC60747-8-4 pg 21	Fig. 12
Q_{gd}	Gate to Drain Charge		18				
Q_g	Total Gate Charge		52				

Note (3): $C_{o(er)}$, a lumped capacitance that gives same stored energy as Coss while Vds is rising from 0 to 500V
$C_{o(tr)}$, a lumped capacitance that gives same charging time as Coss while Vds is rising from 0 to 500V

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Reverse Diode Characteristics (T_C = 25˚C unless otherwise specified)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	4.8		V	V_{GS} = -4 V, I_{SD} = 6.7 A, T_J = 25 °C	Fig. 8, 9, 10
		4.2		V	V_{GS} = -4 V, I_{SD} = 6.7 A, T_J = 175 °C	
I_S	Continuous Diode Forward Current		22	A	V_{GS} = -4 V, T_C = 25˚C	
I_{SM}	Diode pulse Current		101	A	V_{GS} = -4 V, pulse width t_P limited by T_{jmax}	
t_{rr}	Reverse Recover time	14		ns	V_{GS} = -4 V, I_{SD} = 13.4 A, V_R = 500 V dif/dt = 6160 A/µs, T_J = 175 °C	
Q_{rr}	Reverse Recovery Charge	327		nC		
I_{rrm}	Peak Reverse Recovery Current	40		A		
t_{rr}	Reverse Recover time	23		ns	V_{GS} = -4 V, I_{SD} = 13.4 A, V_R = 500 V dif/dt = 2150 A/µs, T_J = 175 °C	
Q_{rr}	Reverse Recovery Charge	220		nC		
I_{rrm}	Peak Reverse Recovery Current	18		A		

Thermal Characteristics

Symbol	Parameter	Typ.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	0.91	°C/W		Fig. 21

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Typical Performance

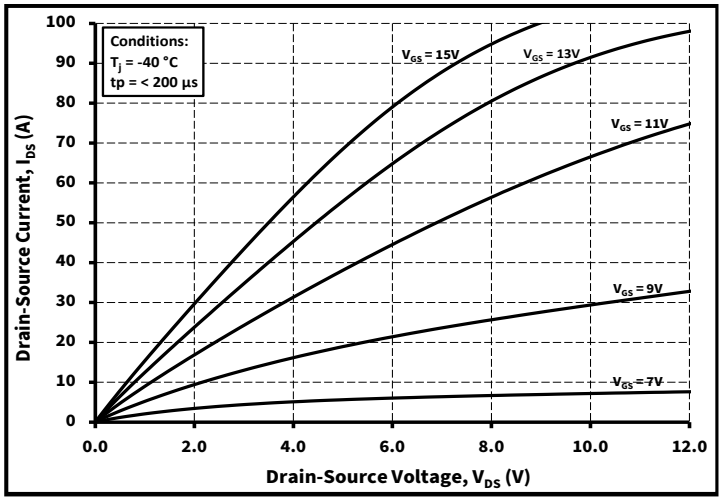


Figure 1. Output Characteristics T_J = -40 ºC

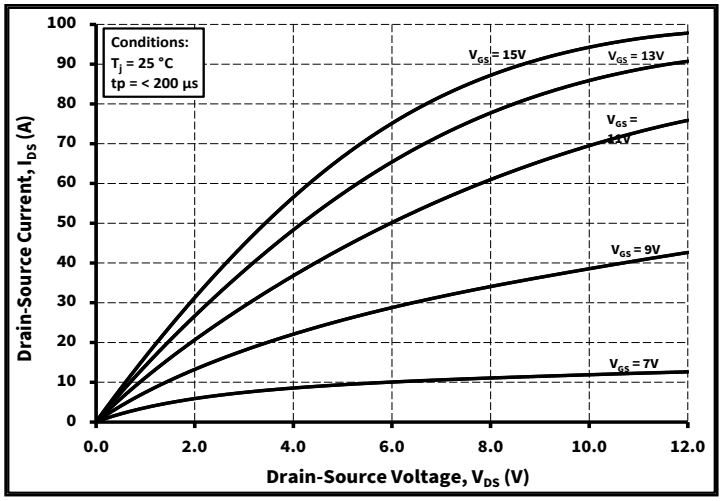


Figure 2. Output Characteristics T_J = 25 ºC

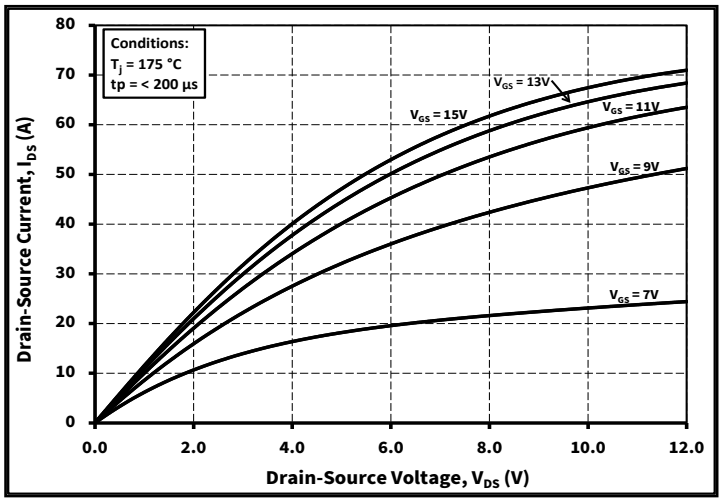


Figure 3. Output Characteristics T_J = 175 ºC

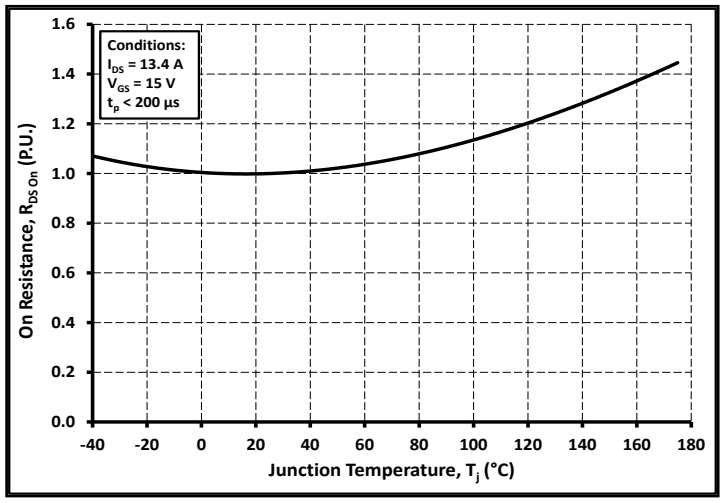


Figure 4. Normalized On-Resistance vs. Temperature

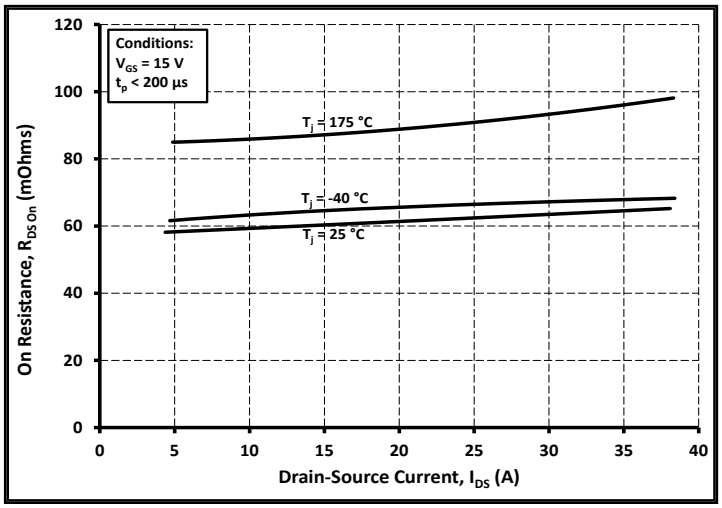


Figure 5. On-Resistance vs. Drain Current
For Various Temperatures

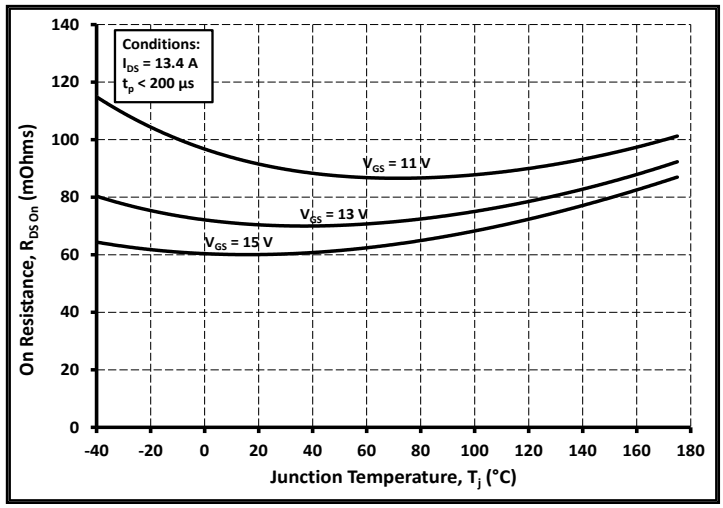


Figure 6. On-Resistance vs. Temperature
For Various Gate Voltage

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Typical Performance

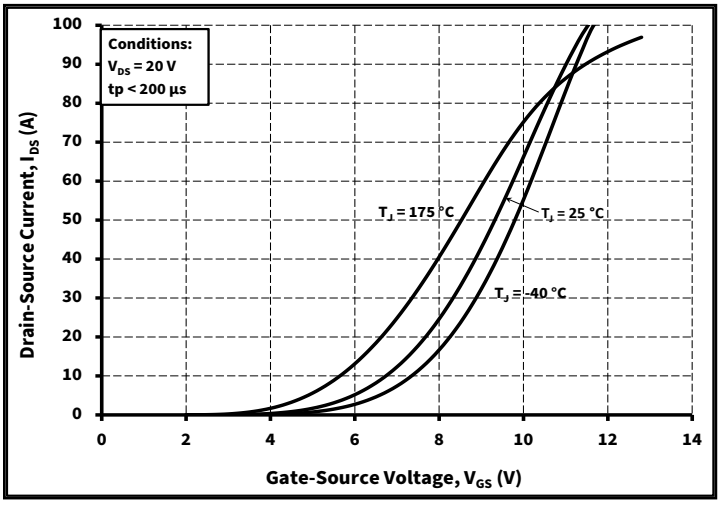


Figure 7. Transfer Characteristic for Various Junction Temperatures

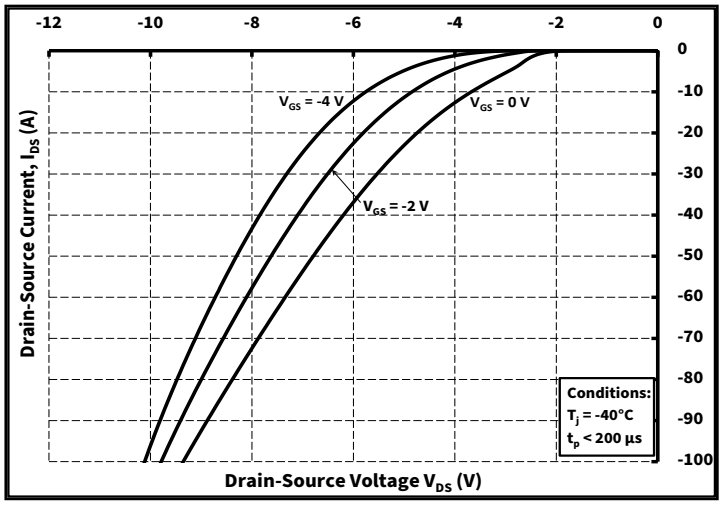


Figure 8. Body Diode Characteristic at -40 °C

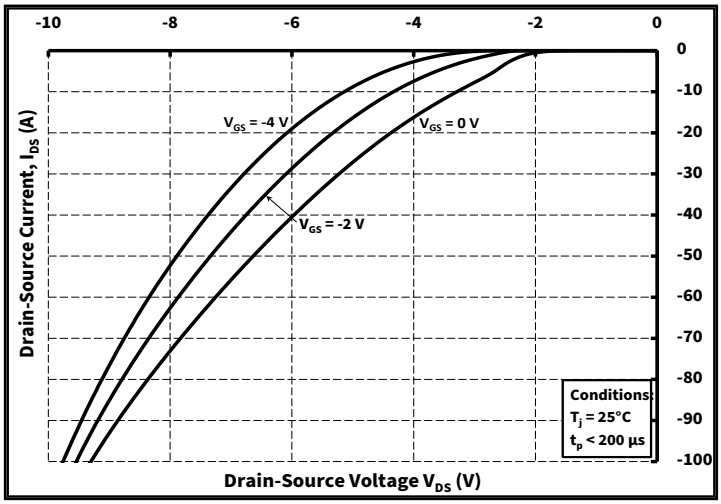


Figure 9. Body Diode Characteristic at 25 °C

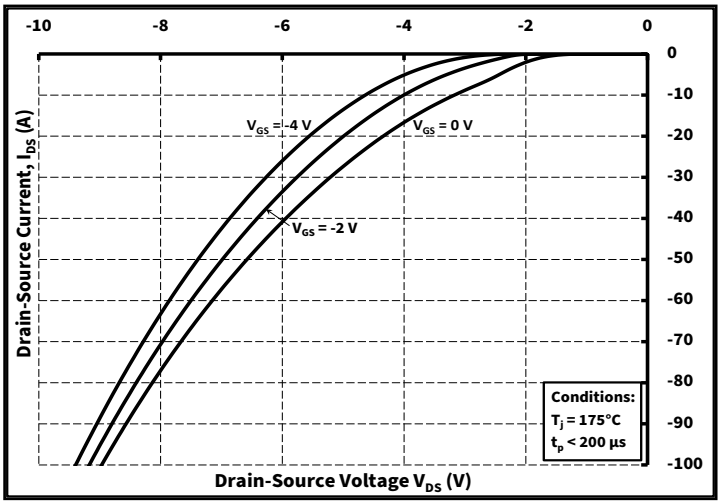


Figure 10. Body Diode Characteristic at 175 °C

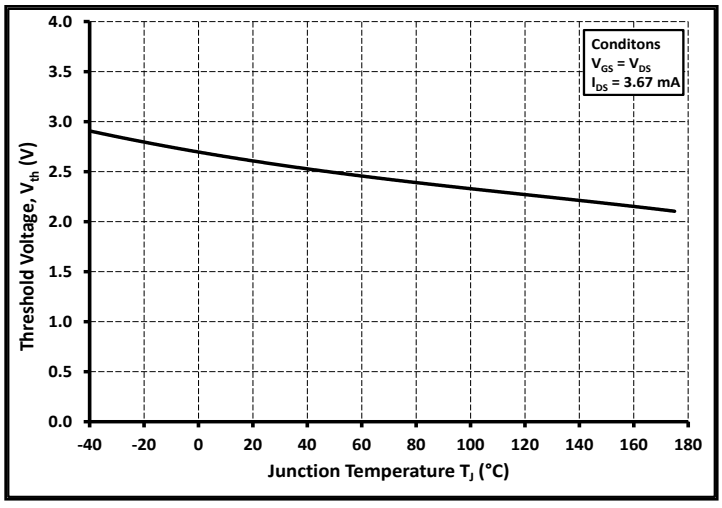


Figure 11. Threshold Voltage vs. Temperature

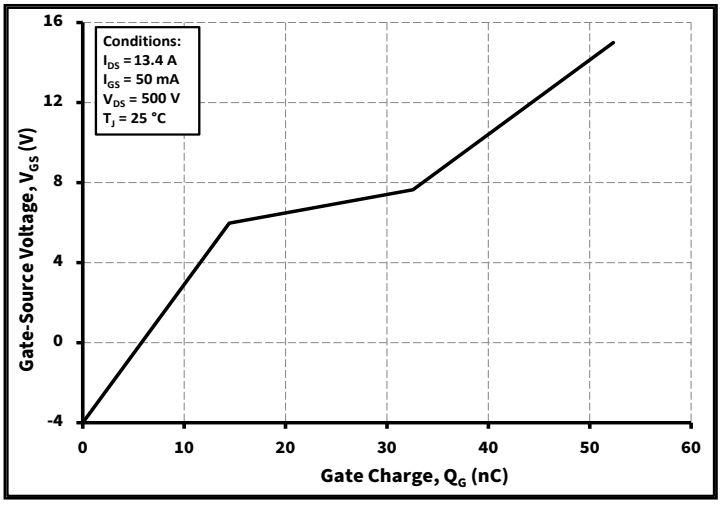


Figure 12. Gate Charge Characteristics

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Typical Performance

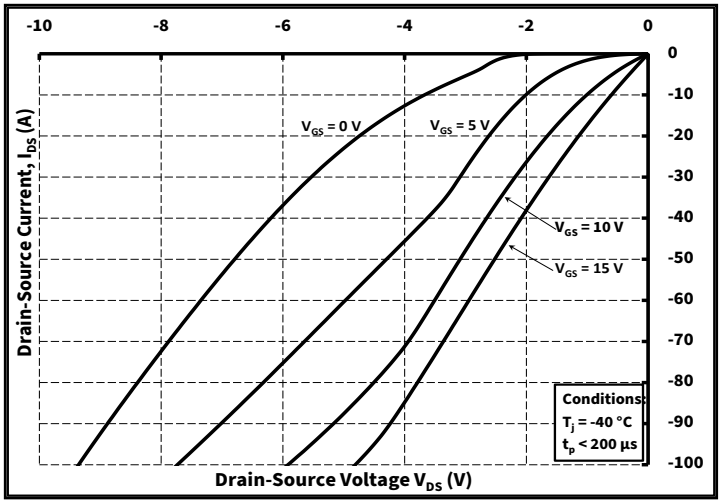


Figure 13. 3rd Quadrant Characteristic at -40 ºC

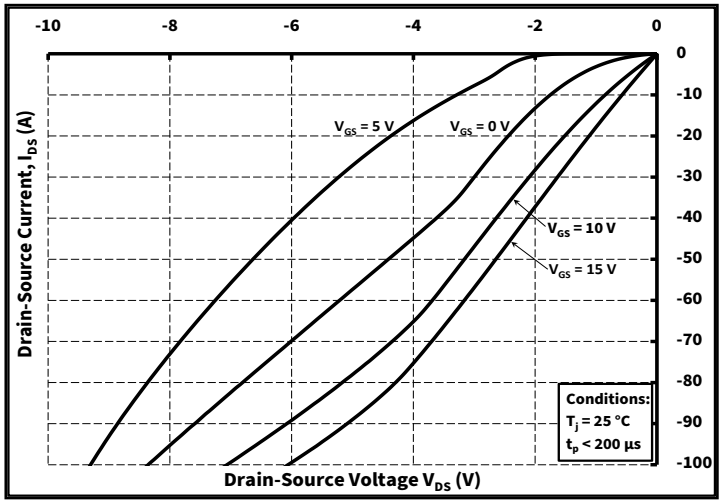


Figure 14. 3rd Quadrant Characteristic at 25 ºC

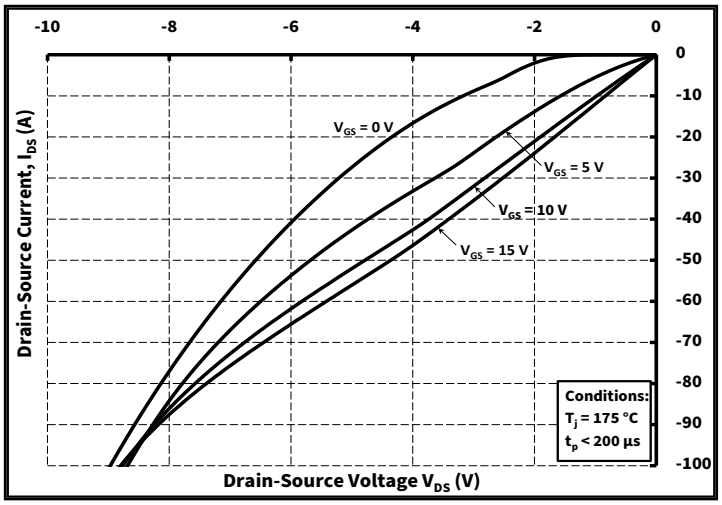


Figure 15. 3rd Quadrant Characteristic at 175 ºC

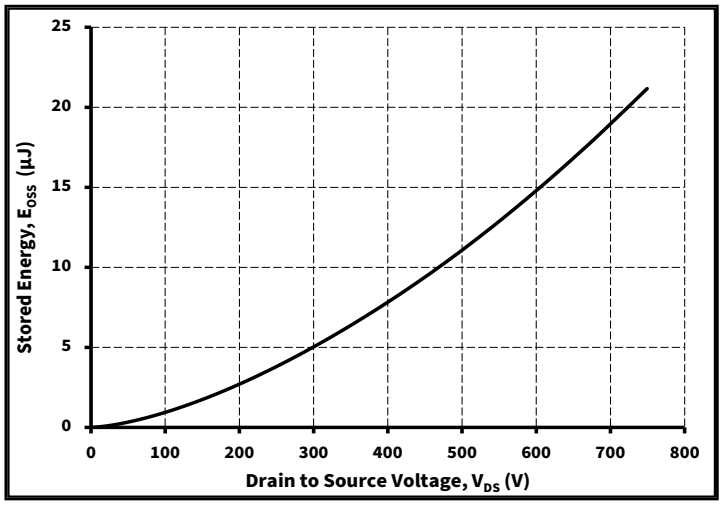


Figure 16. Output Capacitor Stored Energy

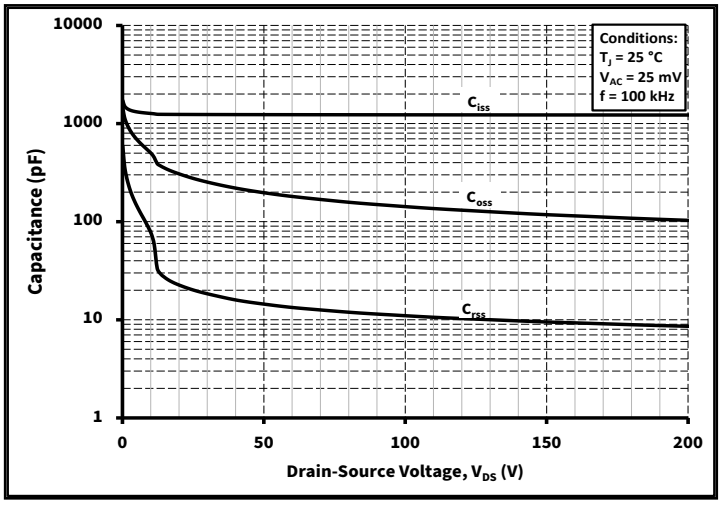


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

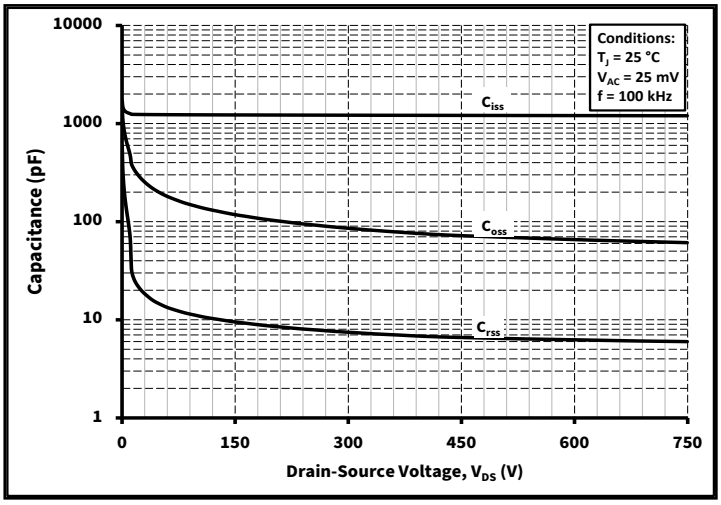


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 750V)

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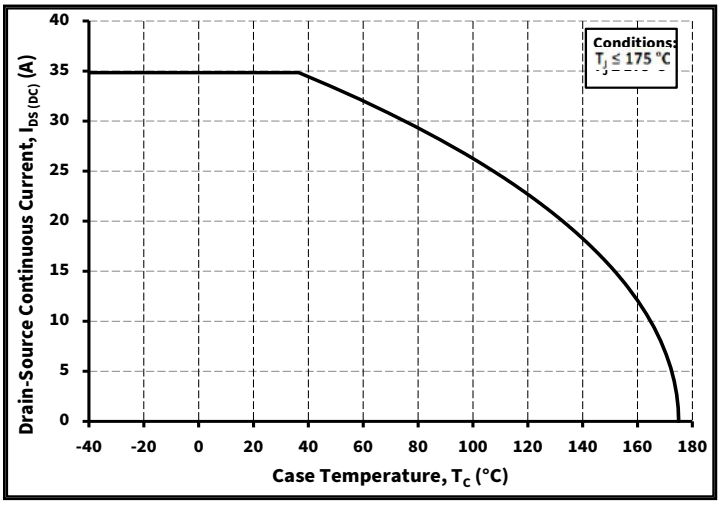


Figure 19. Continuous Drain Current Derating vs. Case Temperature

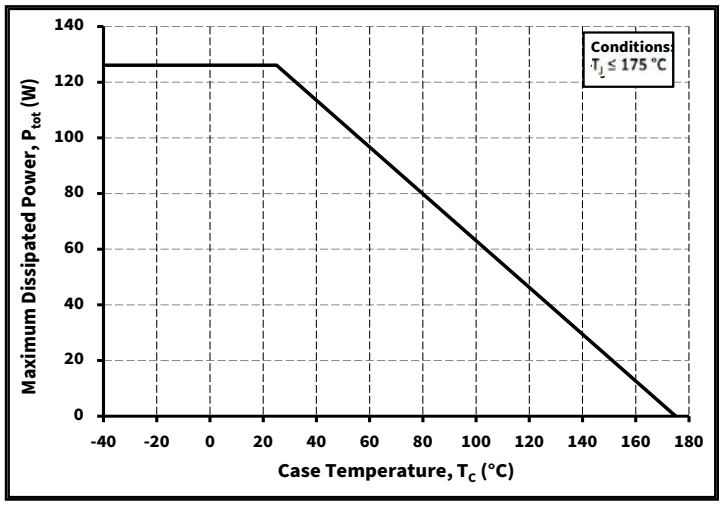


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

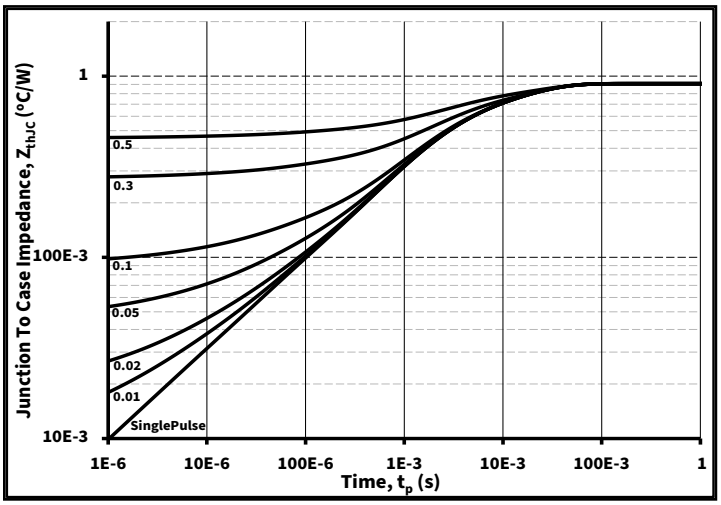


Figure 21. Transient Thermal Impedance (Junction - Case)

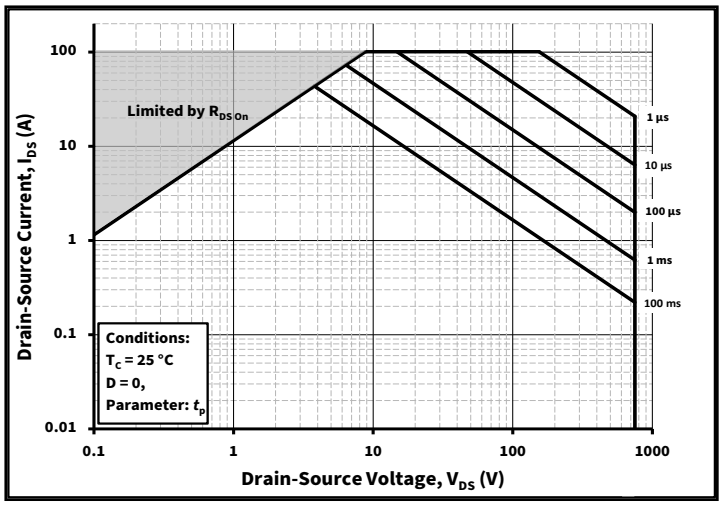


Figure 22. Safe Operating Area

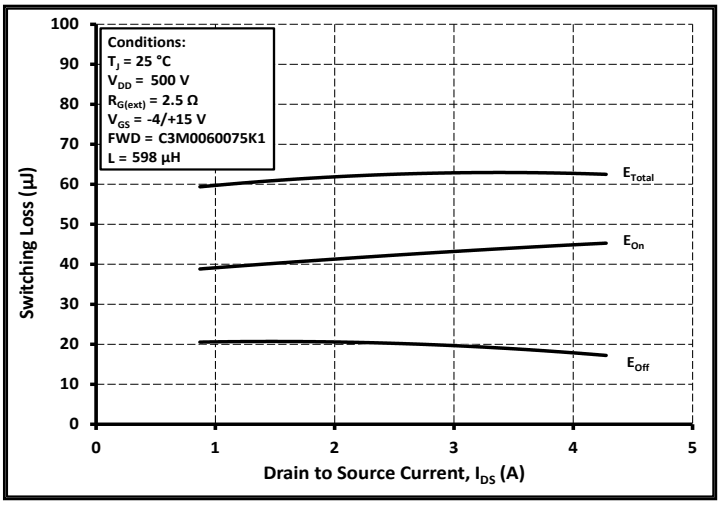


Figure 23. Clamped Inductive Switching Energy vs. Drain Current (V_{DD} = 500V)

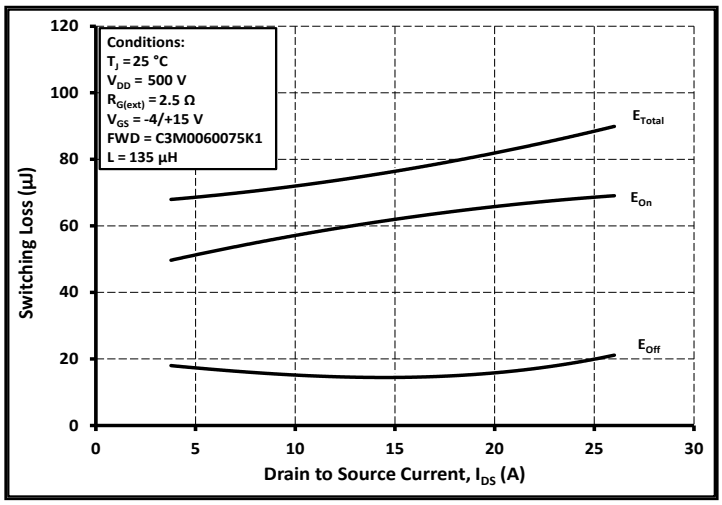


Figure 24. Clamped Inductive Switching Energy vs. Drain Current (V_{DD} = 500V)

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Typical Performance

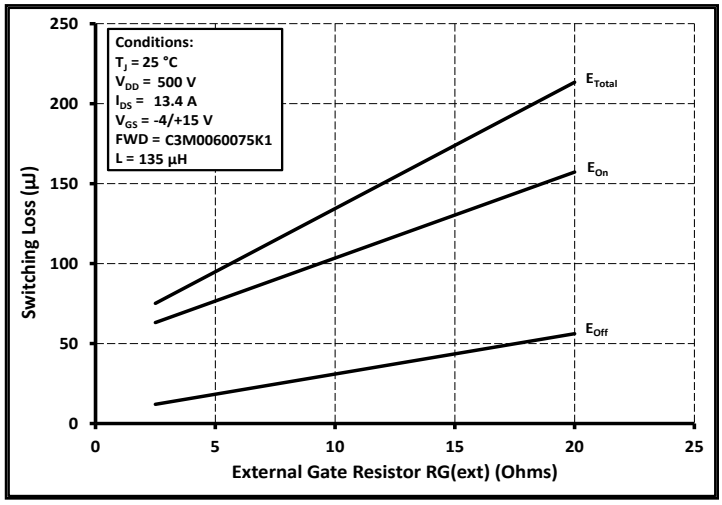


Figure 25. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

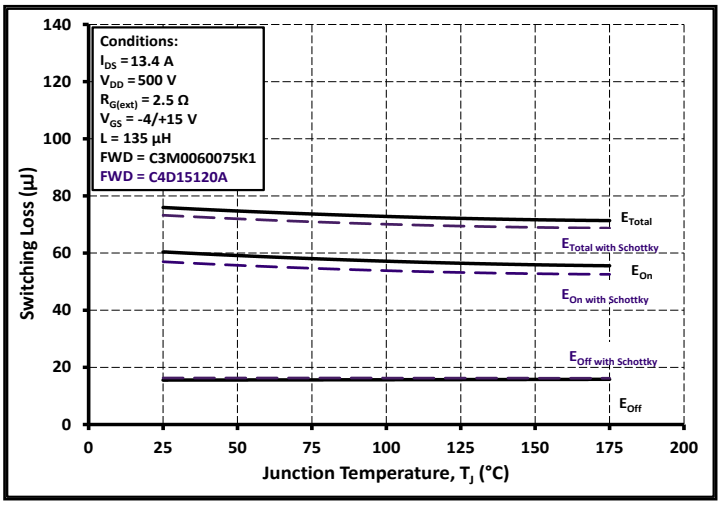


Figure 26. Clamped Inductive Switching Energy vs. Temperature

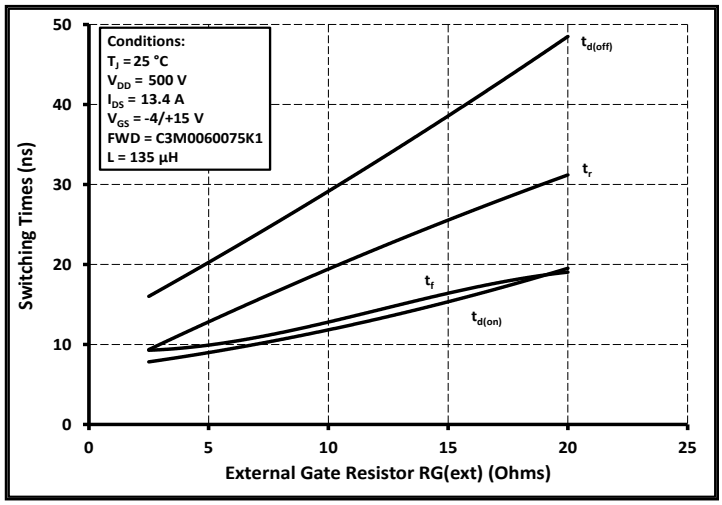


Figure 27. Switching Times vs. $R_{G(ext)}$

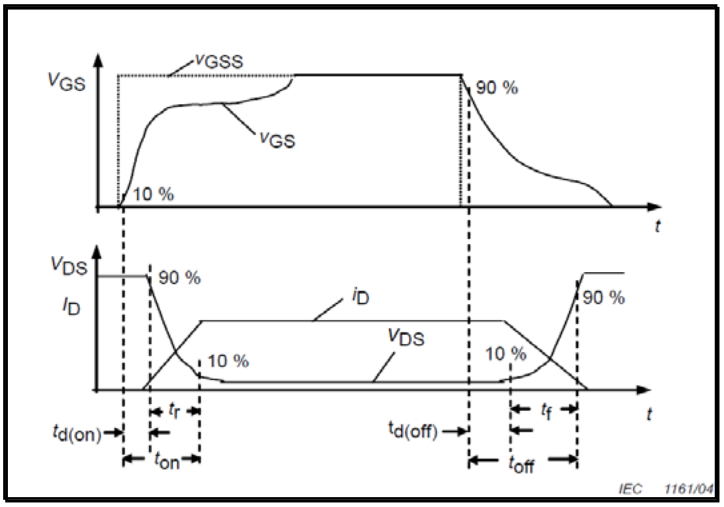


Figure 28. Switching Times Definition

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Test Circuit Schematic

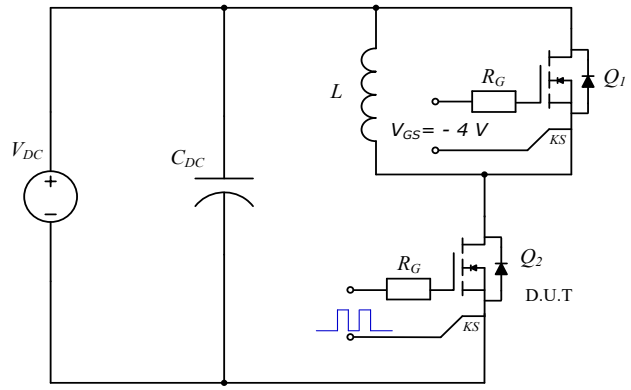
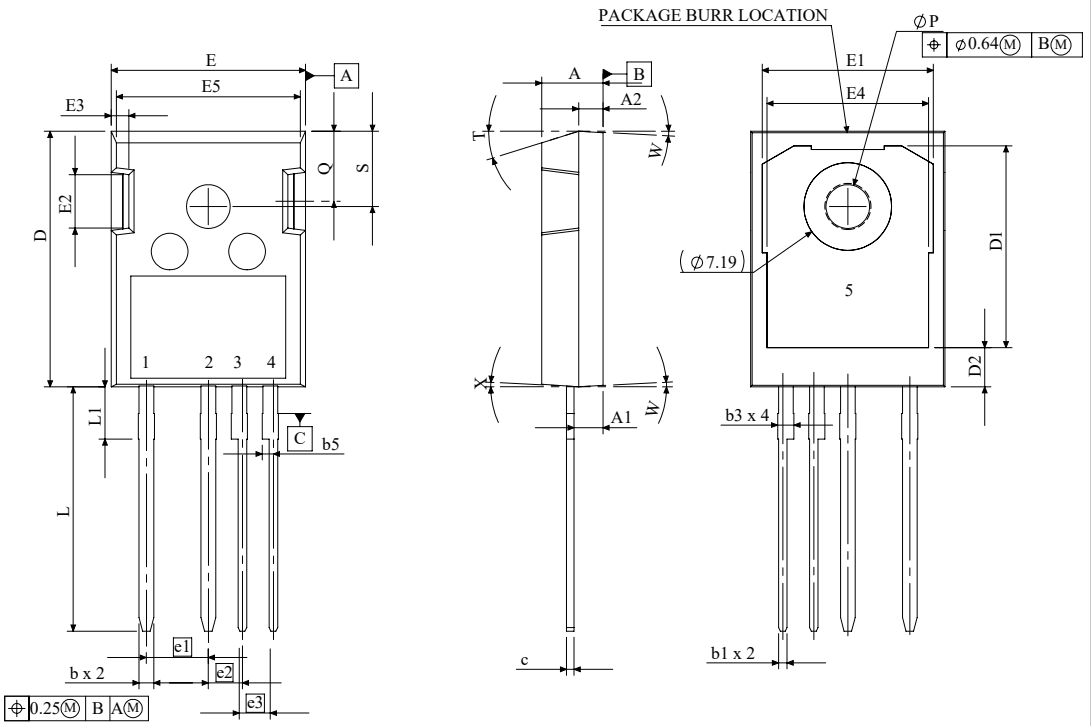


Figure 29. Clamped Inductive Switching Waveform Test Circuit

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Package Dimensions



SYMBOL	MIN (mm)	MAX (mm)
A	4.83	5.21
A1	2.22	2.6
A2	1.91	2.16
b	1.10	1.30
b1	0.65	0.79
b3	1.34	1.44
b5	0.74	1.14
c	0.55	0.68
D	20.76	21.14
D1	16.25	17.65
D2	2.95	3.35
E	15.75	16.13
E1	13.1	14.15
E2	3.68	5.10
E3	1.00	1.90
E4	12.38	13.43
E5	14.65	15.05
e1	5.08 BSC	
e2	2.79 BSC	
e3	2.54 BSC	
L	19.72	20.32
L1	3.87	4.47
ϕP	3.51	3.65
Q	5.49	6.00
S	6.04	6.30
T	17.5° REF.	
W	3.5° REF.	
X	4° REF.	

1	DRAIN
2	SOURCE
3	DRIVER SOURCE
4	GATE
5	DRAIN

NOTE:
1. ALL METAL SURFACES ARE TIN PLATED (MATTE), EXCEPT AREA OF CUT.
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
3. ALL DIMENSIONS ARE LISTED IN MILLIMETERS. ANGLES ARE IN DEGREES.
4. BURR OR MOLD FLASH SIZE (0.5 mm) IS NOT INCLUDED IN THE DIMENSIONS

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TITLE: PACKAGE OUTLINE DRAWING: TO-247-4L LP

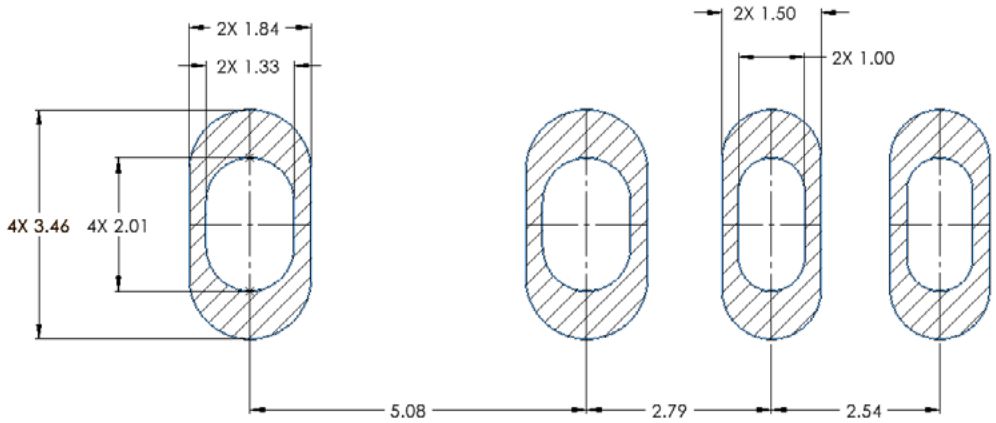
Date: 02/15/24 | REVISION NO. 02 | A4

PRD-05970 | SCALE:1:1 | SHEET 1 OF 1

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Recommended Solder Pad Layout

All dimensions in mm



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Revision history

Document Version	Date of release	Descriptiion of changes
1.0	March-2024	Initial datasheet
2.0	October - 2024	Legal Disclaimer

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Contact info:

4600 Silicon Drive
Durham, NC 27703 USA
Tel: +1.919.313.5300
www.wolfspeed.com/power

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