N-CHANNEL ENHANCEMENT MODE VERTICAL DMOS FET

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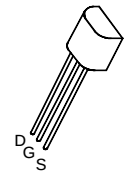
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FEATURES

* 240 Volt V_{DS}
* $R_{DS(on)}$=16Ω

APPLICATIONS

* Telephone handsets



E-Line
TO92 Compatible

ABSOLUTE MAXIMUM RATINGS.

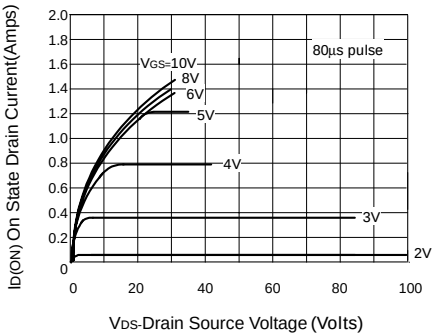
PARAMETER	SYMBOL	VALUE	UNIT
Drain-Source Voltage	V_{DS}	240	V
Continuous Drain Current at T_{amb}=25°C	I_D	160	mA
Pulsed Drain Current	I_{DM}	2	A
Gate Source Voltage	V_{GS}	± 20	V
Power Dissipation at T_{amb}=25°C	P_{tot}	700	mW
Operating and Storage Temperature Range	T_j:T_{stg}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS (at T_{amb} = 25°C unless otherwise stated).

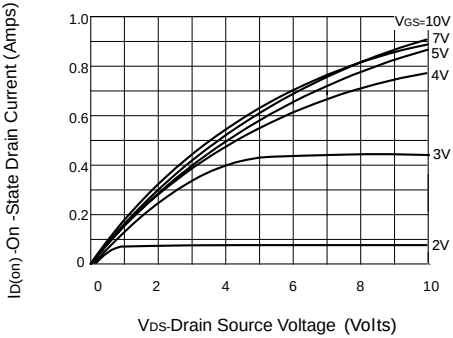
PARAMETER	SYMBOL	MIN.	MAX.	UNIT	CONDITIONS.
Drain-Source Breakdown Voltage	BV_{DSS}	240		V	I_D=1mA, V_{GS}=0V
Gate-Source Threshold Voltage	$V_{GS(th)}$	1	3	V	ID=1mA, V_{DS}= V_{GS}
Gate-Body Leakage	I_{GSS}		20	nA	V_{GS}=± 20V, V_{DS}=0V
Zero Gate Voltage Drain Current	I_{DSS}		10 100	µA µA	V_{DS}=240 V, V_{GS}=0 V_{DS}=192 V, V_{GS}=0V, T=125°C(2)
On-State Drain Current(1)	$I_{D(on)}$	500		mA	V_{DS}=25 V, V_{GS}=10V
Static Drain-Source On-State Resistance (1)	$R_{DS(on)}$		16	Ω	V_{GS}=10V,I_D=250mA
Forward Transconductance (1)(2)	g_{fs}	100		mS	V_{DS}=25V,I_D=250mA
Input Capacitance (2)	C_{iss}		85	pF	V_{DS}=25 V, V_{GS}=0V, f=1MHz
Common Source Output Capacitance (2)	C_{oss}		20	pF	
Reverse Transfer Capacitance (2)	C_{rss}		7	pF	
Turn-On Delay Time (2)(3)	$t_{d(on)}$		7	ns	V_{DD}≈25V, I_D=250mA
Rise Time (2)(3)	t_r		8	ns	
Turn-Off Delay Time (2)(3)	$t_{d(off)}$		16	ns	
Fall Time (2)(3)	t_f		8	ns	

(1) Measured under pulsed conditions. Width=300µs. Duty cycle ≤2%
(2) Sample test.

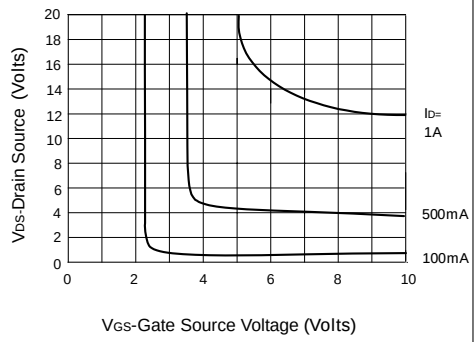
TYPICAL CHARACTERISTICS



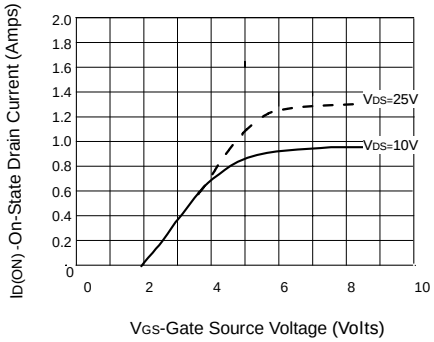
Output Characteristics



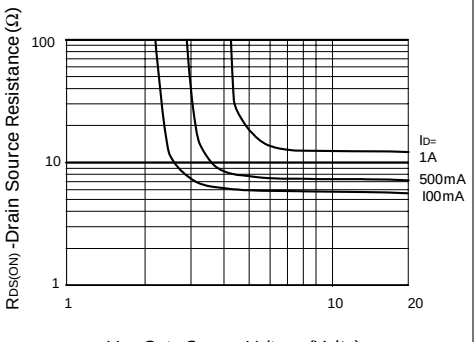
Saturation Characteristics



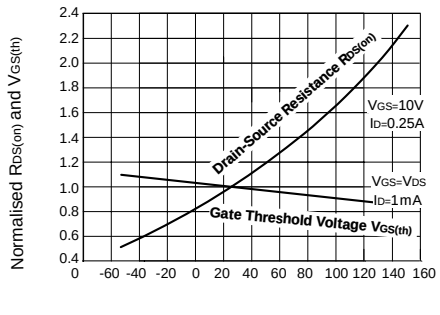
Voltage Saturation Characteristics



Transfer Characteristics



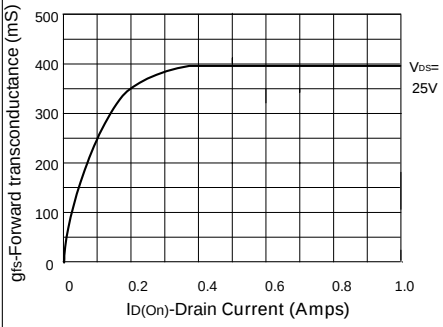
On-resistance vs gate-source voltage



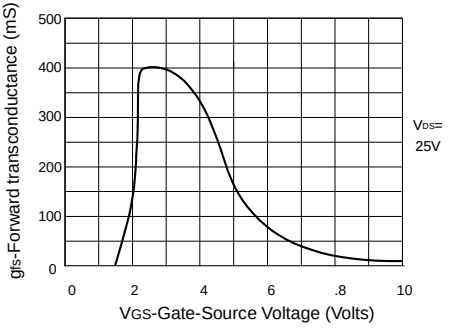
Normalised $R_{DS(on)}$ and $V_{GS(th)}$ V Temperature

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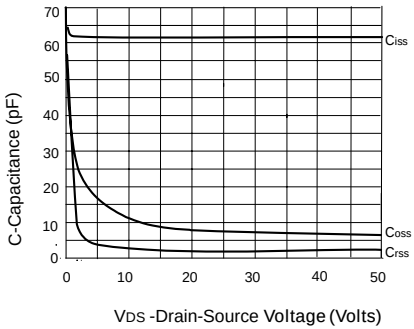
TYPICAL CHARACTERISTICS



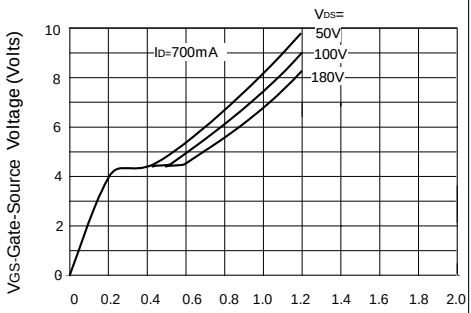
Transconductance v drain current



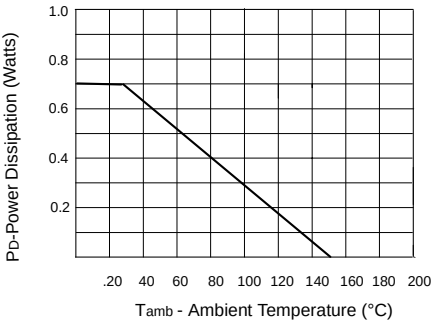
Transconductance v gate-source voltage



Capacitance v drain-source voltage



Gate charge v gate-source voltage



Power v temperature derating curve (ambient)

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