For Automotive 45 V Input 500 mA Fixed Output LDO Regulators

BD4xxS5-C Series

General Description

The BD4xxS5-C series are low quiescent regulators featuring 45 V absolute maximum voltage, and output voltage accuracy of ±2 % (3.3 V or 5 V: Typ), 500 mA output current and 38 µA (Typ) current consumption.
These regulators are therefore ideal for applications requiring a direct connection to the battery and a low current consumption.
A logical “HIGH” at the CTL enables the device and “LOW” at the CTL disables the device.
(Only W: Includes Enable Input).
Ceramic capacitors can be used for compensation of the output capacitor phase. Furthermore, these ICs also feature overcurrent protection to protect the device from damage caused by short-circuiting and an integrated thermal shutdown to protect the device from overheating at overload conditions.

Features

- Qualified for Automotive Applications
- Wide Temperature Range (Tj): -40 °C to +150 °C
- Wide Operating Input Range: 3.0 V to 42 V
- Low Quiescent Current: 38 µA (Typ)
- Output Current: 500 mA
- High Output Voltage Accuracy: ±2 %
- Output Voltage: 3.3 V or 5.0 V (Typ)
- Enable Input (Only W: Includes Enable Input)
- Overload Current Protection (OCP)
- Thermal Shutdown Protection (TSD)
- AEC-Q100 Qualified(Note 1)
- Functional Safety Supportive Automotive Products

(Note 1): Grade 1

Packages

W (Typ) x D (Typ) x H (Max)

- FP: TO252-3 6.5 mm × 9.5 mm × 2.5 mm
- FP: TO252-5 6.5 mm × 9.5 mm × 2.5 mm
- EFJ: HTSOP-J8 4.9 mm × 6.0 mm × 1.0 mm
- FP2: TO263-3 10.16 mm × 15.10 mm × 4.70 mm
- FP2: TO263-5 10.16 mm × 15.10 mm × 4.70 mm

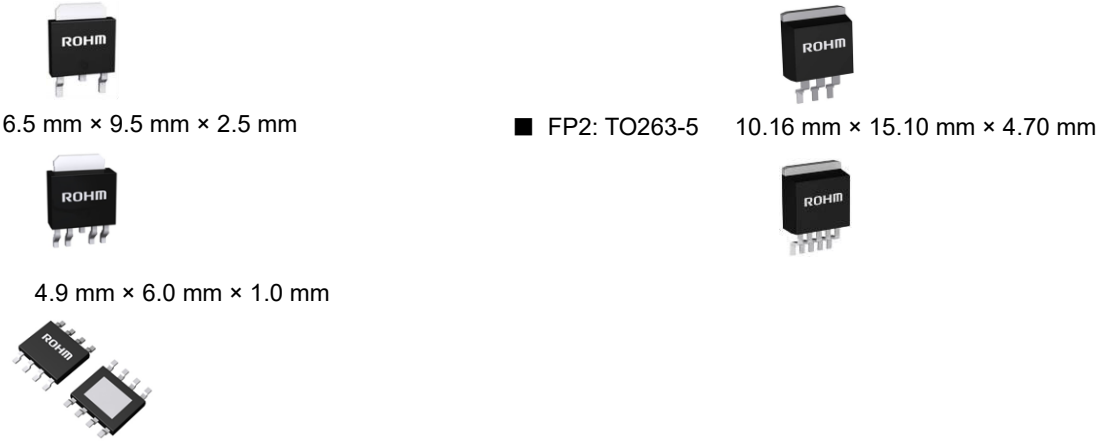


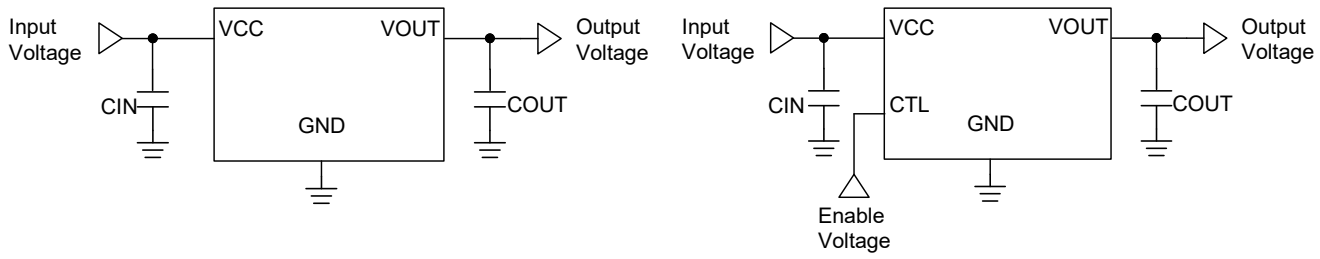
Figure 1. Package Outlook

Applications

- Body
- Audio System
- Navigation System, etc.

Typical Application Circuits

■Components Externally Connected: 0.1 µF ≤ CIN, 10 µF ≤ COUT (Typ)
* Electrolytic, tantalum and ceramic capacitors can be used.



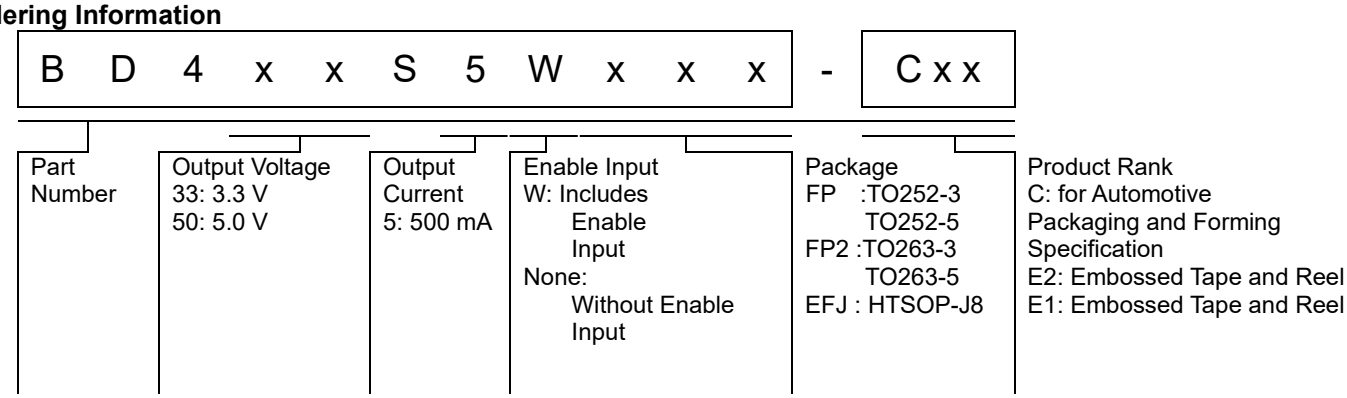
For product without Enable input For product with Enable input

Figure 2. Typical Application Circuits

○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

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Ordering Information



Lineup

Output Current Ability	Output Voltage (Typ)	Enable Input(Note 1)	Package Type	Orderable Part Number
500 mA	3.3 V	not available	TO252-3	BD433S5FP-CE2
			TO263-3	BD433S5FP2-CE2
			HTSOP-J8	BD433S5EFJ-CE2
		available	TO252-5	BD433S5WFP-CE2
			TO263-5	BD433S5WFP2-CE2
			HTSOP-J8	BD433S5WEFJ-CE2
	5.0 V	not available	TO252-3	BD450S5FP-CE2
			TO263-3	BD450S5FP2-CE2
			HTSOP-J8	BD450S5EFJ-CE2
		available	TO252-5	BD450S5WFP-CE2 BD450S5WFP-CE1
			TO263-5	BD450S5WFP2-CE2
			HTSOP-J8	BD450S5WEFJ-CE2

(Note 1) available: Includes Enable Input

not available: Not includes Enable Input

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Pin Configurations

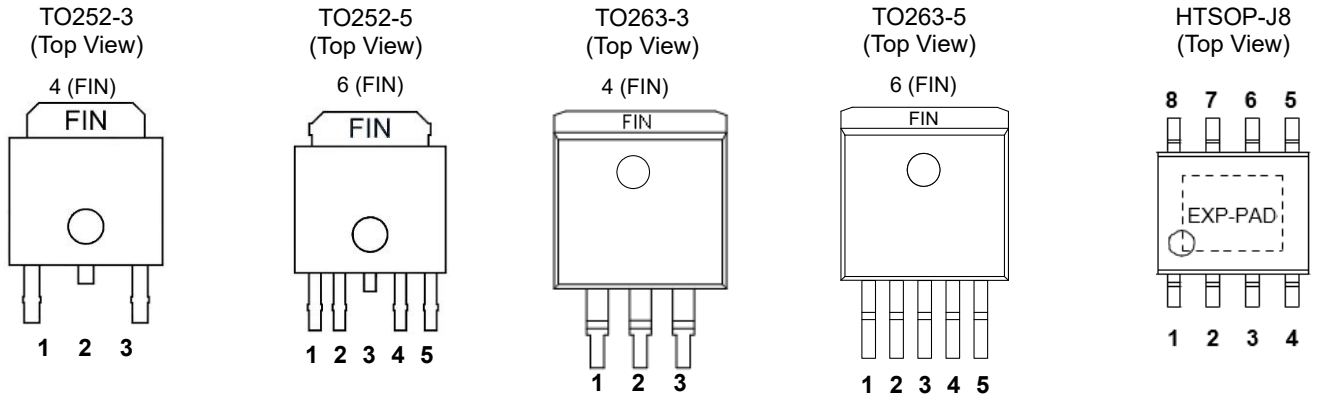


Figure 3. Pin Configurations

Pin Descriptions

■BD433S5FP-C / BD450S5FP-C

Pin No.	Pin Name	Pin Function
1	VCC	Supply voltage input pin
2	N.C.	Not connected
3	VOUT	Output pin
4 (FIN)	GND	Ground pin

■BD433S5WFP-C / BD450S5WFP-C

Pin No.	Pin Name	Pin Function
1	VCC	Supply voltage input pin
2	CTL	Output control pin
3	N.C.	Not connected
4	N.C.	Not connected
5	VOUT	Output pin
6 (FIN)	GND	Ground pin

■BD433S5FP2-C / BD450S5FP2-C

Pin No.	Pin Name	Pin Function
1	VCC	Supply voltage input pin
2	GND	Ground pin
3	VOUT	Output pin
4 (FIN)	GND	Ground pin

■BD433S5WFP2-C / BD450S5WFP2-C

Pin No.	Pin Name	Pin Function
1	VCC	Supply voltage input pin
2	CTL	Output control pin
3	GND	Ground pin
4	N.C.	Not connected
5	VOUT	Output pin
6 (FIN)	GND	Ground pin

■BD433S5EFJ-C / BD450S5EFJ-C

Pin No.	Pin Name	Pin Function
1	VOUT	Output pin
2	N.C.	Not connected
3	N.C.	Not connected
4	N.C.	Not connected
5	GND	Ground pin
6	N.C.	Not connected
7	N.C.	Not connected
8	VCC	Supply voltage input pin
-	EXP-PAD	Heat dissipation

■BD433S5WEFJ-C / BD450S5WEFJ-C

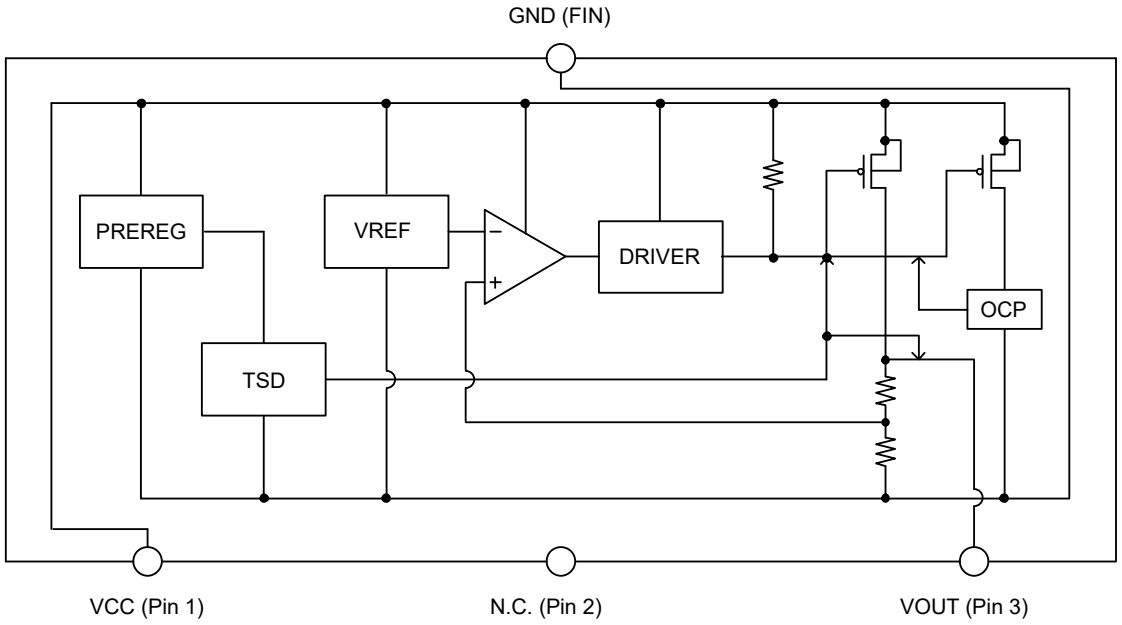
Pin No.	Pin Name	Pin Function
1	VOUT	Output pin
2	N.C.	Not connected
3	N.C.	Not connected
4	N.C.	Not connected
5	GND	Ground pin
6	N.C.	Not connected
7	CTL	Output control pin
8	VCC	Supply voltage input pin
-	EXP-PAD	Heat dissipation

* N.C. Pin is recommended to short with GND.
* N.C. Pin can be open because it isn't connected it inside of IC.
* EXP-PAD on the back side is connected to the IC substrate, so it should connect to external ground node.

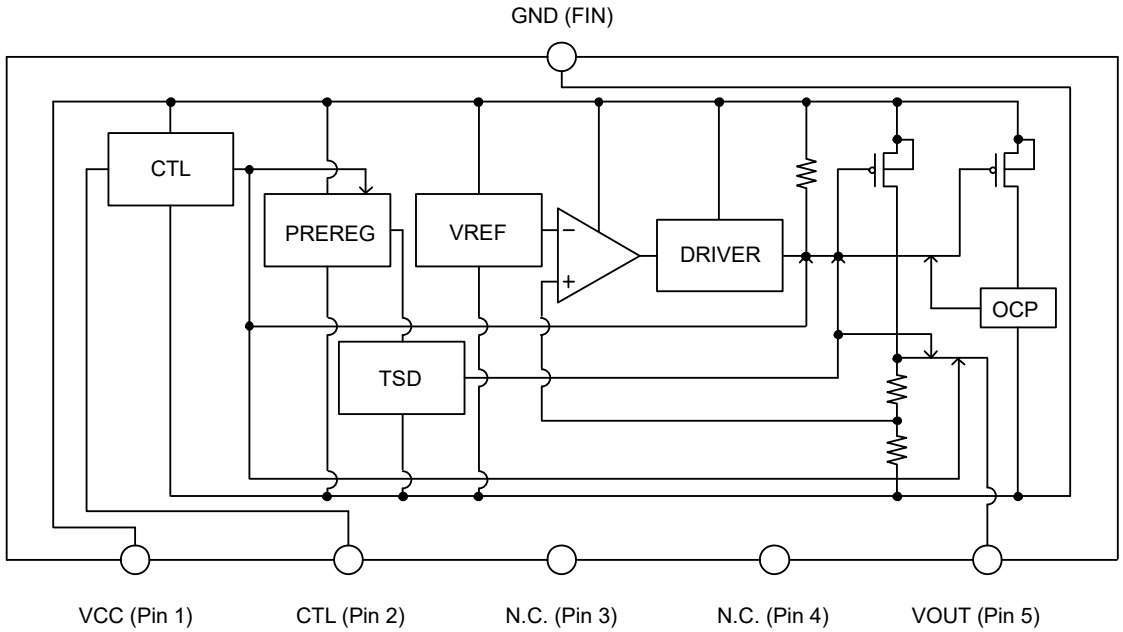
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Block Diagrams

■ BD4xxS5FP-C



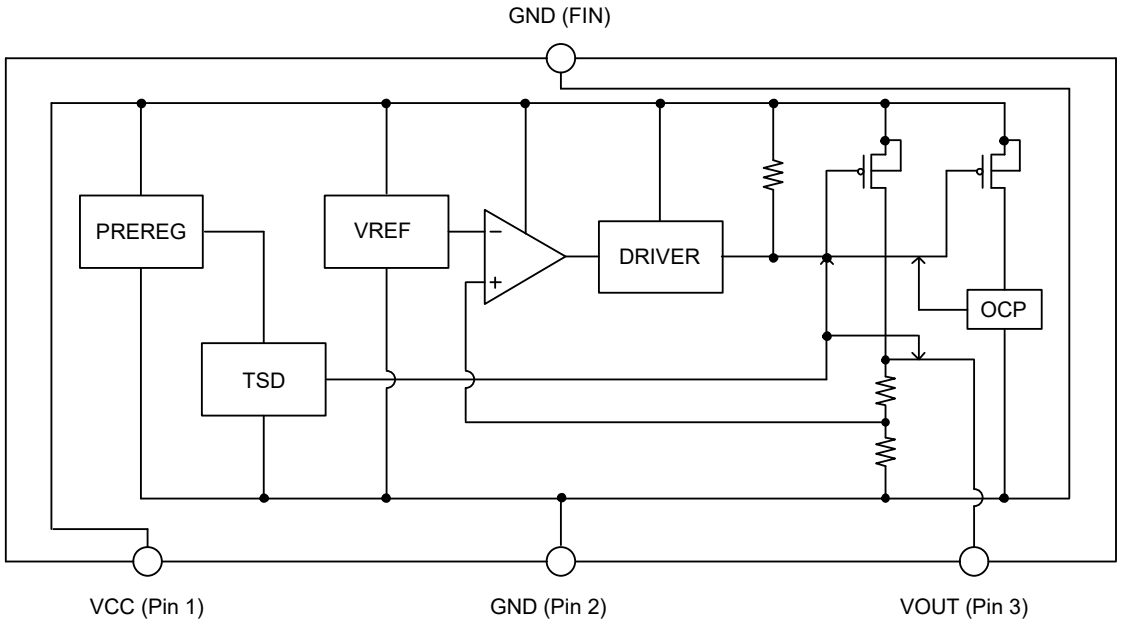
■ BD4xxS5WFP-C



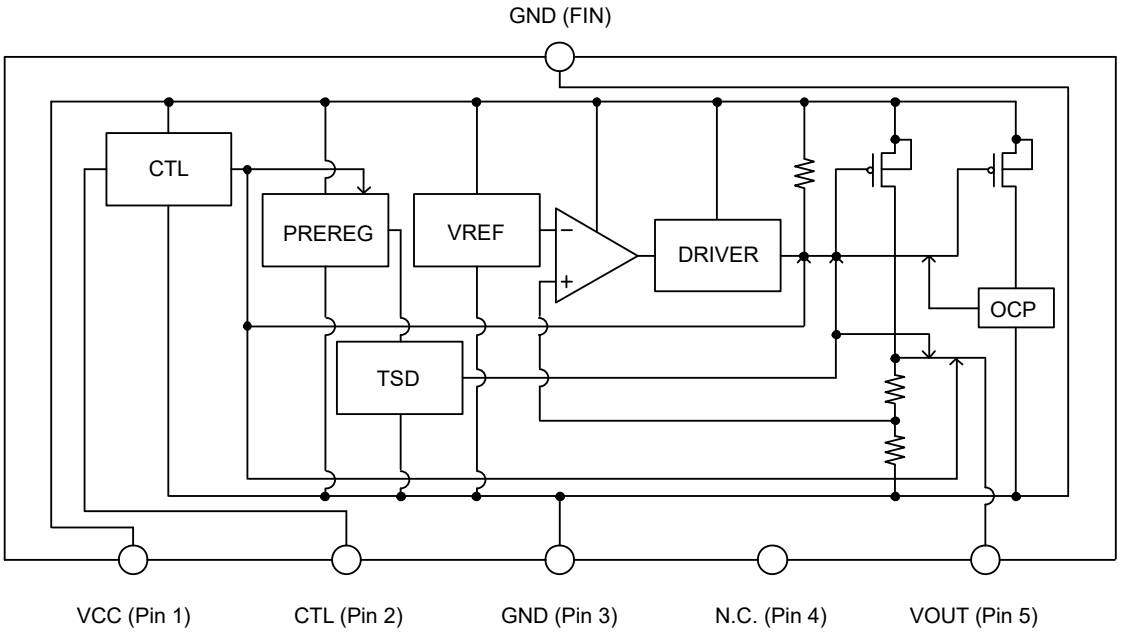
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Block Diagrams – continued

■ BD4xxS5FP2-C



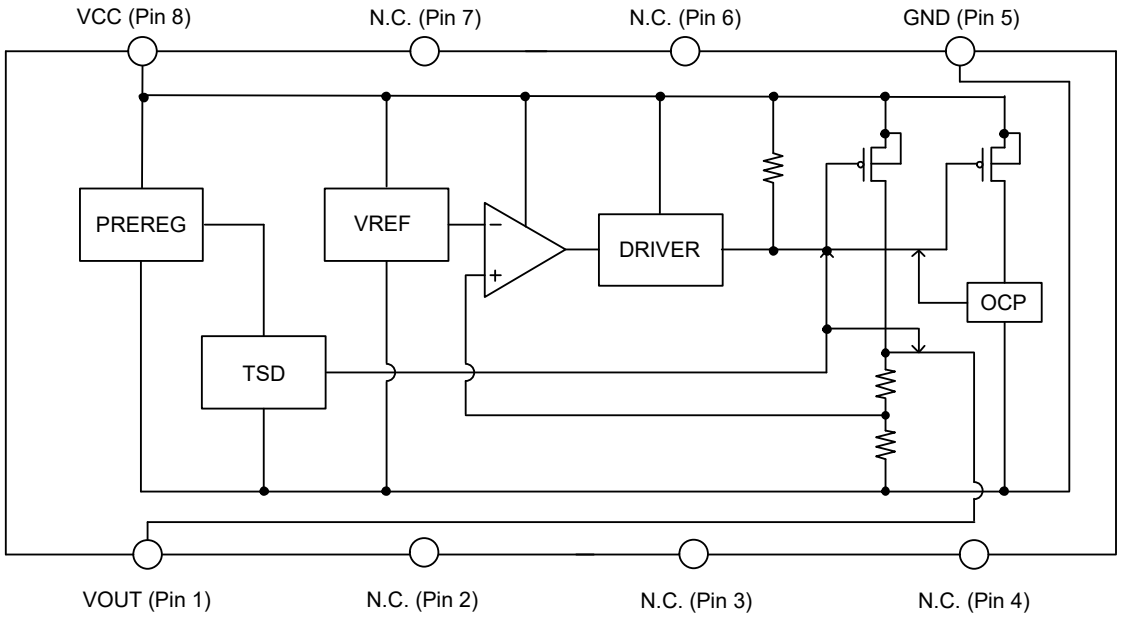
■ BD4xxS5WFP2-C



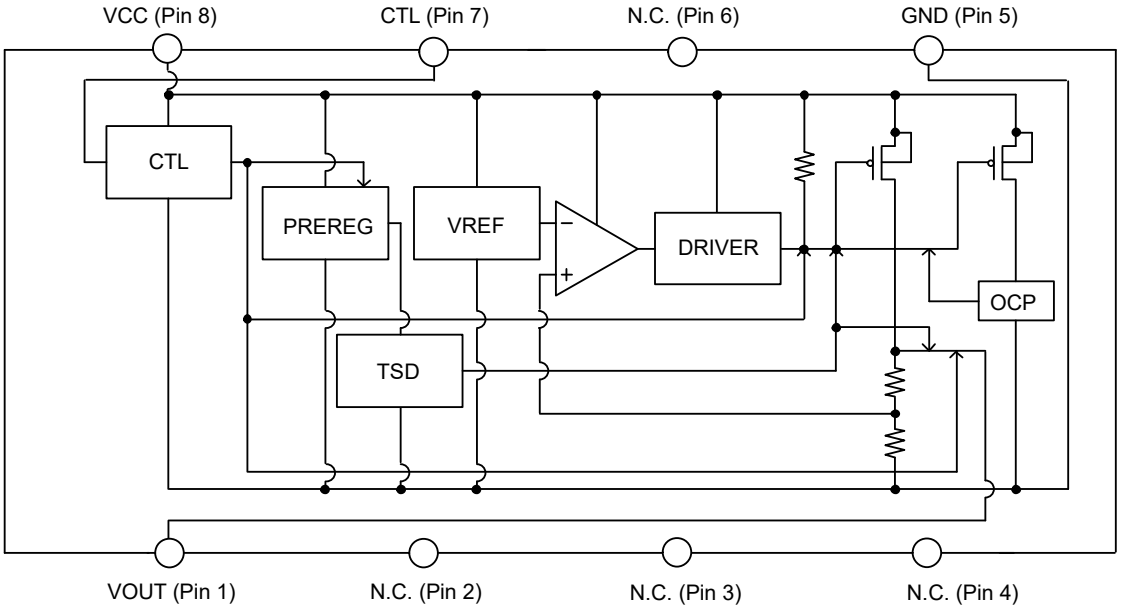
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Block Diagrams – continued

■ BD4xxS5EFJ-C



■ BD4xxS5WEFJ-C



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Description of Blocks

Block Name	Function	Description of Blocks
CTL *(Note 1)*	Control Output Voltage ON/OFF	A logical “HIGH” (≥ 2.8 V) at the CTL enables the device and “LOW” (≤ 0.8 V) at the CTL disable the device.
PREREG	Internal Power Supply	Power Supply for Internal Circuit
TSD	Thermal Shutdown Protection	To protect the device from overheating. If the chip temperature (Tj) reaches ca. 175 °C (Typ), the output is turned off.
VREF	Reference Voltage	Generate the Reference Voltage
DRIVER	Output MOS FET Driver	Drive the Output MOS FET
OCP	Over Current Protection	To protect the device from damage caused by over current. If the output current reaches ca. 900 mA (Typ), the output is turned off.

(Note 1) Applicable for product with Enable Input.

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Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply Voltage *(Note 1)*	VCC	-0.3 to +45.0	V
Output Control Voltage *(Note 2)*	CTL	-0.3 to +45.0	V
Output Voltage	VOUT	-0.3 to +8.0	V
Junction Temperature Range	Tj	-40 to +150	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	+150	°C
ESD withstand Voltage (HBM) *(Note 3)*	$V_{ESD, HBM}$	±2000	V

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance and power dissipation taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

(Note 1) Do not exceed Pd.

(Note 2) Applicable for product with Enable Input.
The start-up orders of power supply (VCC) and the CTL pin do not influence if the voltage is within the operation power supply voltage range.

(Note 3) ESD susceptibility Human Body Model “HBM”.

Operating Conditions (-40 °C ≤ Tj ≤ +150 °C)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (IOUT ≤ 500 mA) *(Note 1)*	VCC	5.9	42.0	V
Supply Voltage (IOUT ≤ 250 mA) *(Note 1)*	VCC	5.5	42.0	V
Supply Voltage (IOUT ≤ 500 mA) *(Note 2)*	VCC	4.6	42.0	V
Supply Voltage (IOUT ≤ 250 mA) *(Note 2)*	VCC	4.0	42.0	V
Output Control Voltage *(Note 3)*	CTL	0	42.0	V
Start-Up Voltage *(Note 4)*	VCC	3.0	–	V
Output Current	IOUT	0	500	mA
Junction Temperature Range	Tj	-40	+150	°C

(Note 1) For 5.0 V Output products (BD450S5FP-C, BD450S5WFP-C, BD450S5FP2-C, BD450S5WFP2-C, BD450S5EFJ-C, BD450S5WEFJ-C)

(Note 2) For 3.3 V Output products (BD433S5FP-C, BD433S5WFP-C, BD433S5FP2-C, BD433S5WFP2-C, BD433S5EFJ-C, BD433S5WEFJ-C)

(Note 3) Applicable for product with Enable Input.

(Note 4) When IOUT = 0 mA

Notice: Please consider that the output voltage would be dropped (Dropout voltage) according to the output current.

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Thermal Impedance *(Note 1)*

Parameter	Symbol	Typ	Unit	Conditions
TO252-3 / TO252-5				
Junction to Ambient	θ_{JA}	136	°C/W	1s *(Note 2)*
		23	°C/W	2s2p *(Note 3)*
Junction to Top Center of Case*(Note 4)*	Ψ_{JT}	17	°C/W	1s *(Note 2)*
		3	°C/W	2s2p *(Note 3)*
TO263-3 / TO263-5				
Junction to Ambient	θ_{JA}	81	°C/W	1s *(Note 2)*
		21	°C/W	2s2p *(Note 3)*
Junction to Top Center of Case*(Note 4)*	Ψ_{JT}	8	°C/W	1s *(Note 2)*
		2	°C/W	2s2p *(Note 3)*
HTSOP-J8				
Junction to Ambient	θ_{JA}	126	°C/W	1s *(Note 2)*
		27	°C/W	2s2p *(Note 3)*
Junction to Top Center of Case*(Note 4)*	Ψ_{JT}	9	°C/W	1s *(Note 2)*
		2	°C/W	2s2p *(Note 3)*

(Note 1) The thermal impedance is based on JESD51 - 2A (Still-Air) standard.

(Note 2) JESD51 - 3 standard FR4 114.3 mm × 76.2 mm × 1.57 mm 1-layer (1s)

(Top copper foil: ROHM recommended footprint + wiring to measure, 2 oz. copper.)

(Note 3) JESD51 -5 / -7 standard FR4 114.3 mm × 76.2 mm × 1.60 mm 4-layer（2s2p）
(Top copper foil: ROHM recommended footprint + wiring to measure / 2 inner layers copper foil area of PCB: 74.2 mm × 74.2 mm, copper (top & reverse side / inner layers) 2oz. / 1oz.)

(Note 4) T_T : Top center of case's (mold) temperature

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Electrical Characteristics

Unless otherwise specified, -40 °C ≤ Tj ≤ +150 °C, VCC = 13.5 V, CTL = 5 V *(Note 1)*, IOUT = 0 mA
The typical value is defined at Tj = 25 °C.

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Shutdown Current	Ishut(Note 1)	–	2.0	5.0	μA	CTL = 0 V Tj ≤ 125 °C
Circuit Current	Icc	–	38	95	μA	IOUT = 0 mA Tj ≤ 125 °C
		–	38	175	μA	IOUT ≤ 500 mA Tj ≤ 150 °C
Output Voltage	VOUT(Note 2)	4.90	5.00	5.10	V	6 V ≤ VCC ≤ 42 V, 0 mA ≤ IOUT ≤ 400 mA
		4.80	5.00	5.10	V	6 V ≤ VCC ≤ 42V 0 mA ≤ IOUT ≤ 500 mA
	VOUT(Note 3)	3.23	3.30	3.37	V	6 V ≤ VCC ≤ 42 V 0 mA ≤ IOUT ≤ 400 mA
		3.20	3.30	3.37	V	6 V ≤ VCC ≤ 42 V 0 mA ≤ IOUT ≤ 500 mA
Dropout Voltage	ΔVd(Note 2)	–	0.20	0.50	V	VCC = VOUT × 0.95 (Typ 4.75 V) IOUT = 300 mA
	ΔVd(Note 3)	–	0.25	0.75	V	VCC = VOUT × 0.95 (Typ 3.135 V) IOUT = 300 mA
Ripple Rejection	R.R.	55	60	–	dB	f = 120 Hz, ein = 1 Vrms IOUT = 100 mA
Line Regulation	Reg.I	–	10	30	mV	8 V ≤ VCC ≤ 16 V
Load Regulation	Reg.L	–	10	30	mV	10 mA ≤ IOUT ≤ 400 mA
Thermal Shutdown	TSD	–	175	–	°C	Tj at TSD ON

(Note 1) Applicable for product with Enable Input.

(Note 2) For 5.0 V Output products (BD450S5FP-C, BD450S5WFP-C, BD450S5FP2-C, BD450S5WFP2-C, BD450S5EFJ-C, BD450S5WEFJ-C)

(Note 3) For 3.3 V Output products (BD433S5FP-C, BD433S5WFP-C, BD433S5FP2-C, BD433S5WFP2-C, BD433S5EFJ-C, BD433S5WEFJ-C)

Electrical Characteristics (Enable function * Applicable for product with Enable Input.)

Unless otherwise specified, -40 °C ≤ Tj ≤ +150 °C, VCC = 13.5 V, IOUT = 0 mA. The typical value is defined at Tj = 25 °C.

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
CTL ON Mode Voltage	VthH	2.8	–	–	V	Active Mode
CTL OFF Mode Voltage	VthL	–	–	0.8	V	Off Mode
CTL Bias Current	ICTL	–	15	30	μA	CTL = 5 V

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Typical Performance Curves (Reference Data)

■For 3.3 V Output products

■Applicable Models:BD433S5FP-C, BD433S5WFP-C, BD433S5FP2-C, BD433S5WFP2-C, BD433S5EFJ-C, BD433S5WEFJ-C

Unless otherwise specified: -40 °C ≤ Tj ≤ +150 °C, VCC = 13.5 V, CTL = 5 V(Note 1), IOUT = 0 mA.

(Note 1) Applicable for product with Enable Input.

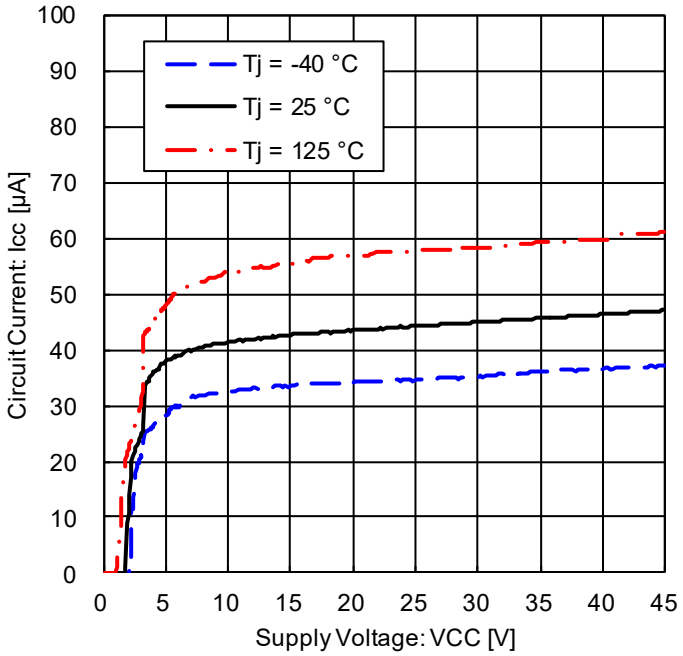


Figure 4. Circuit Current vs Power Supply Voltage

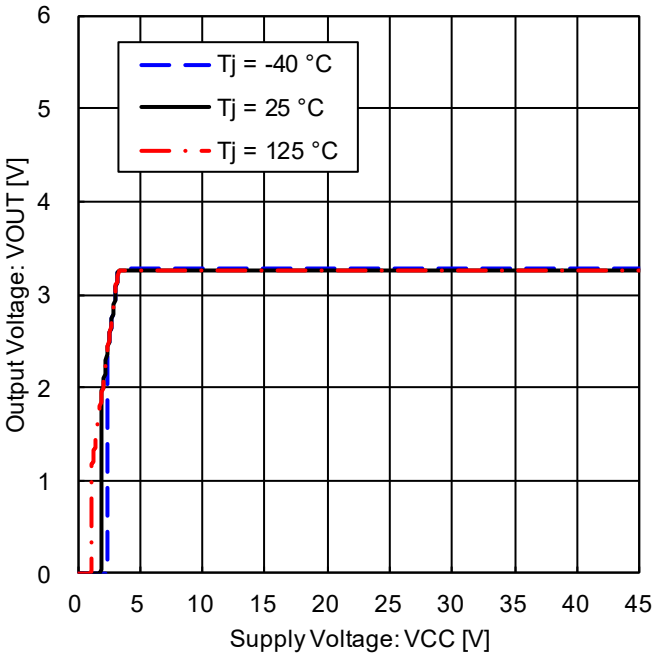


Figure 5. Output Voltage vs Power Supply Voltage (IOUT = 0 mA)

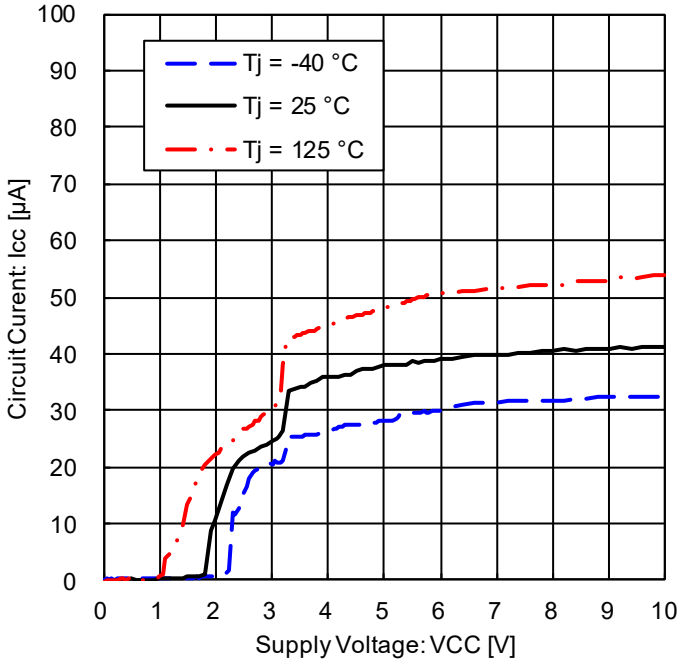


Figure 6. Circuit Current vs Power Supply Voltage - Magnified Figure 4.

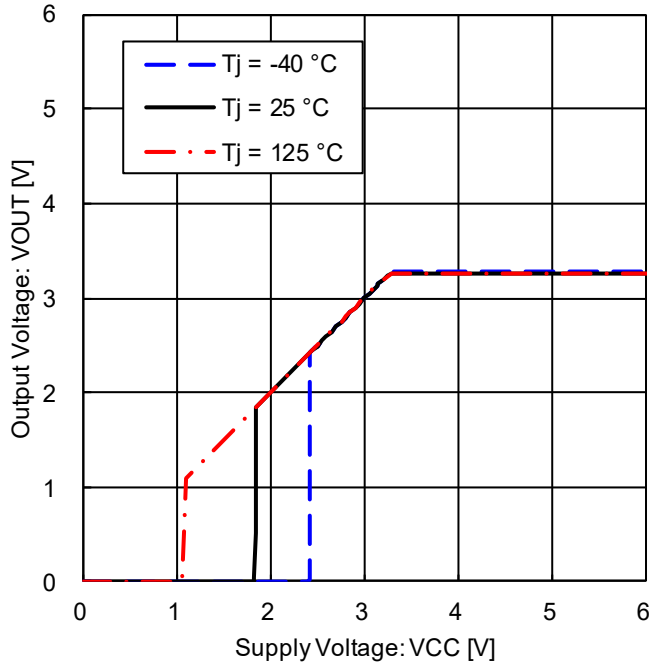


Figure 7. Output Voltage vs Power Supply Voltage (IOUT = 0 mA) - Magnified Figure 5.

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Typical Performance Curves (Reference Data) – continued

■For 3.3 V Output products

■Applicable Models:BD433S5FP-C, BD433S5WFP-C, BD433S5FP2-C, BD433S5WFP2-C, BD433S5EFJ-C, BD433S5WEFJ-C

Unless otherwise specified: -40 °C ≤ Tj ≤ +150 °C, VCC = 13.5 V, CTL = 5 V(Note 1), IOUT = 0 mA.

(Note 1) Applicable for product with Enable Input.

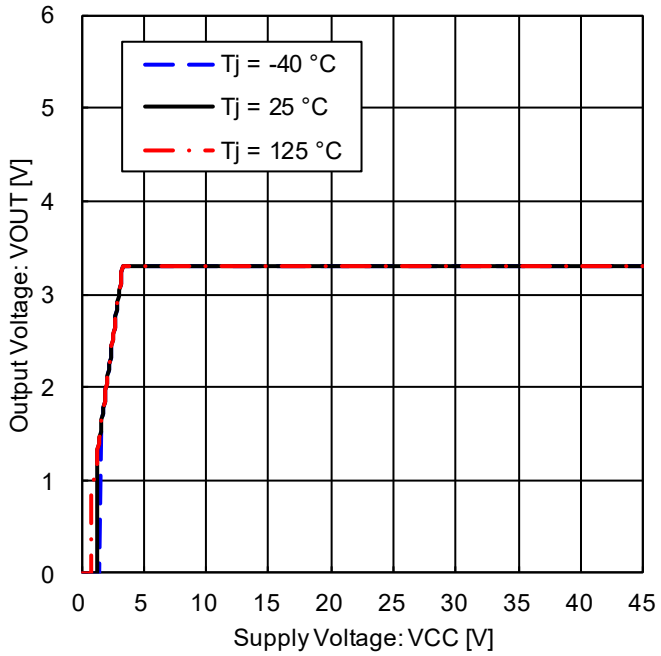


Figure 8. Output Voltage vs Power Supply Voltage (IOUT = 10 mA)

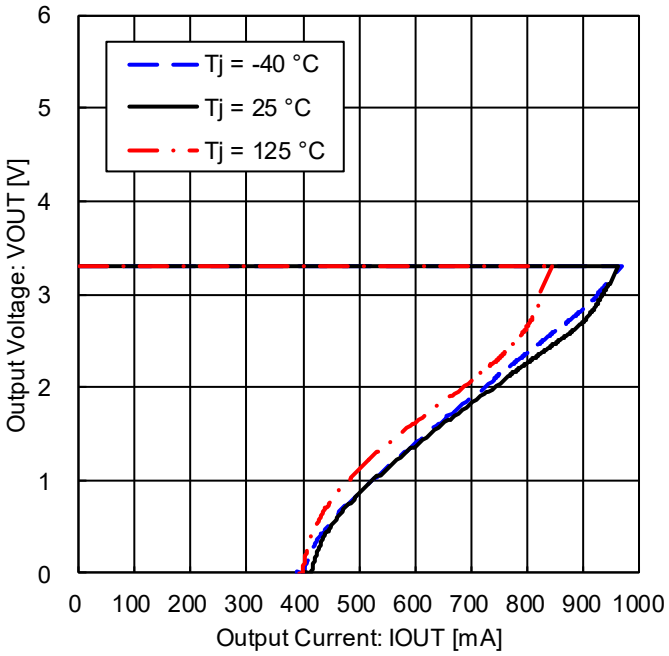


Figure 9. Output Voltage vs Output Current (Over Current Protection)

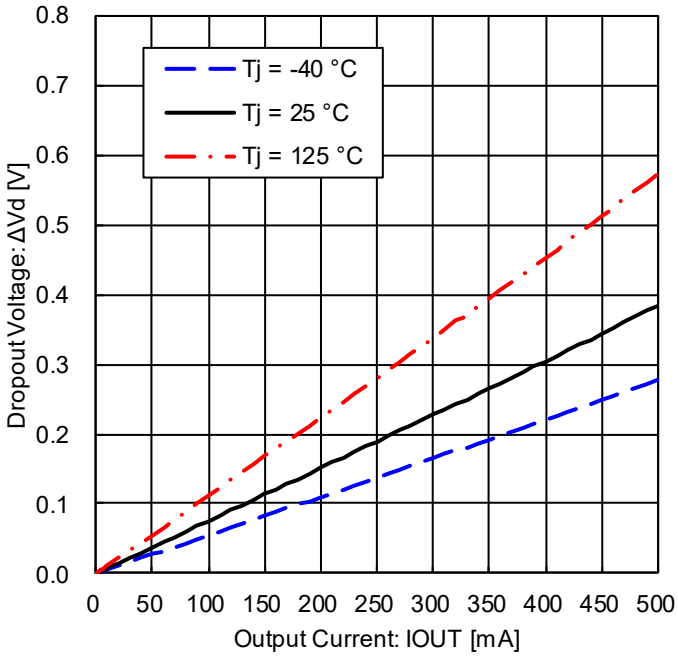


Figure 10. Dropout Voltage (VCC = 3.135 V)

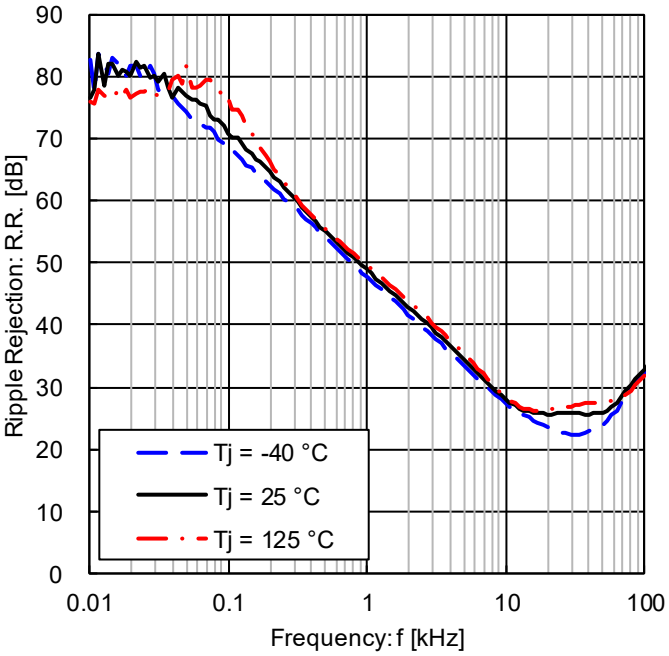


Figure 11. Ripple Rejection (ein = 1 Vrms, IOUT = 100 mA)

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Typical Performance Curves (Reference Data) – continued

■For 3.3 V Output products

■Applicable Models:BD433S5FP-C, BD433S5WFP-C, BD433S5FP2-C, BD433S5WFP2-C, BD433S5EFJ-C, BD433S5WEFJ-C

Unless otherwise specified: -40 °C ≤ Tj ≤ +150 °C, VCC = 13.5 V, CTL = 5 V(Note 1), IOUT = 0 mA.

(Note 1) Applicable for product with Enable Input.

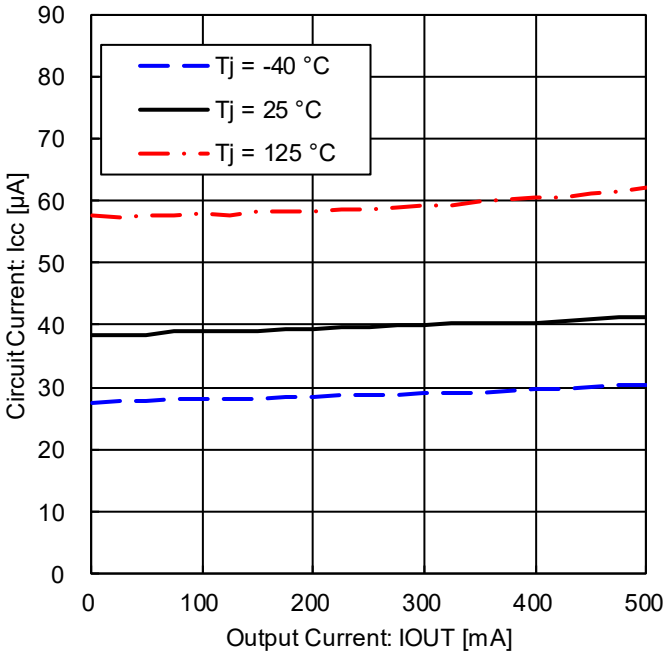


Figure 12. Circuit Current vs Output Current

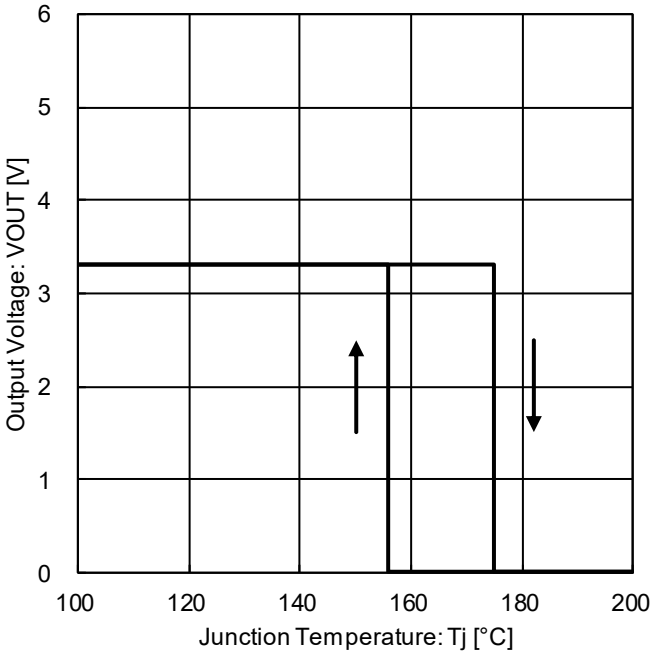


Figure 13. Output Voltage vs Temperature (Thermal Shutdown)

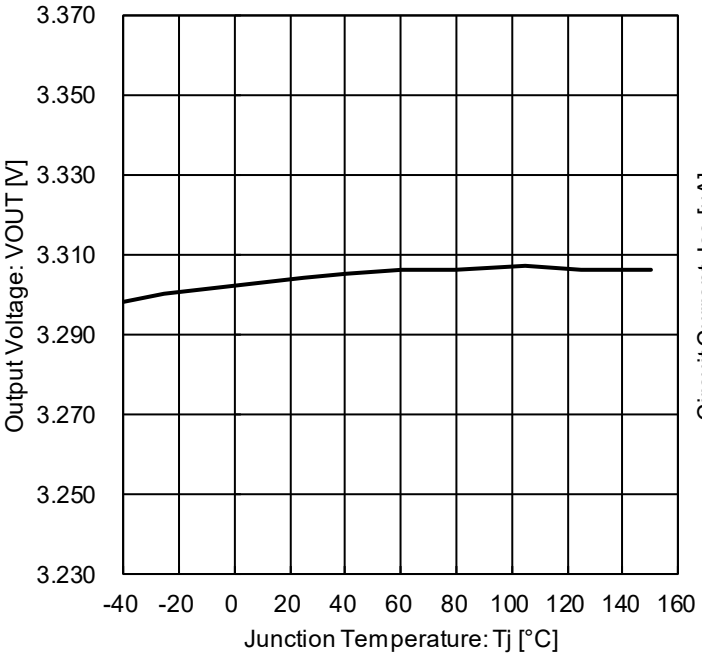


Figure 14. Output Voltage vs Temperature

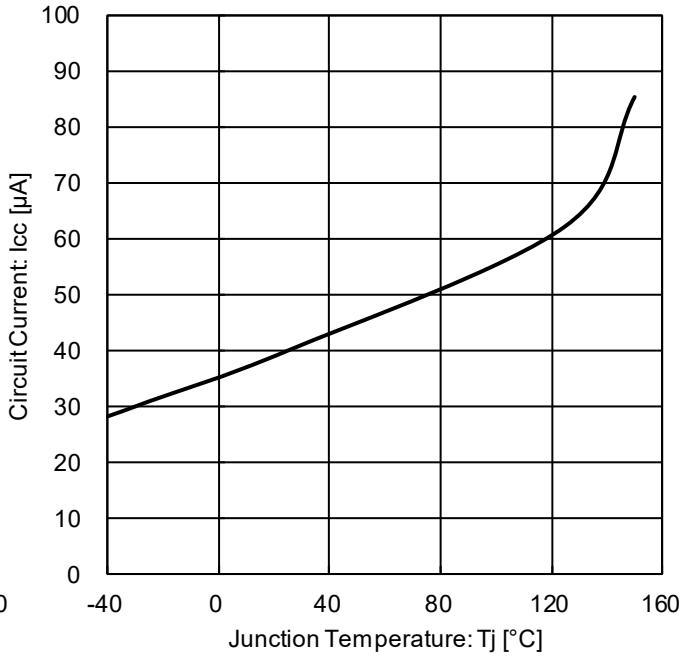


Figure 15. Circuit Current vs Temperature

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Typical Performance Curves (Reference Data) – continued

■For 3.3 V Output with Enable input products

■Applicable Model:BD433S5WFP-C, BD433S5WFP2-C, BD433S5WEFJ-C

Unless otherwise specified: -40 °C ≤ Tj ≤ +150 °C, VCC = 13.5 V, IOUT = 0 mA

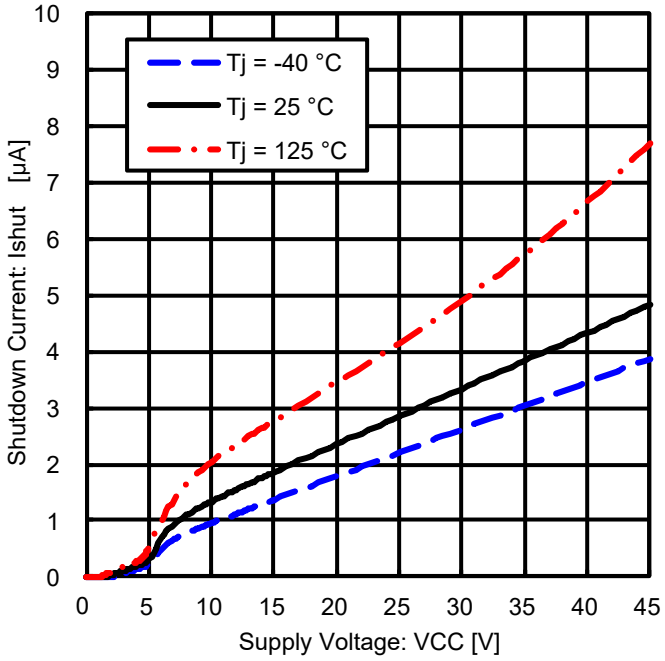


Figure 16. Shutdown Current vs Power Supply Voltage (CTL = 0 V)

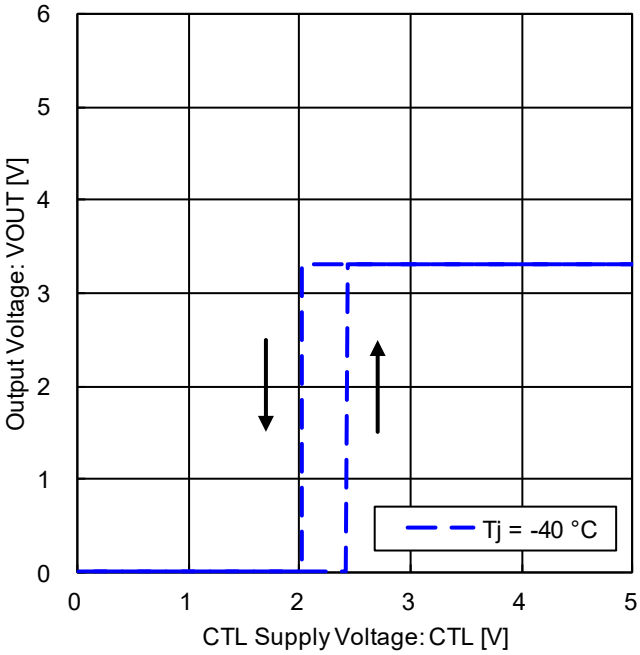


Figure 17. CTL ON / OFF Mode Voltage (Tj = -40 °C)

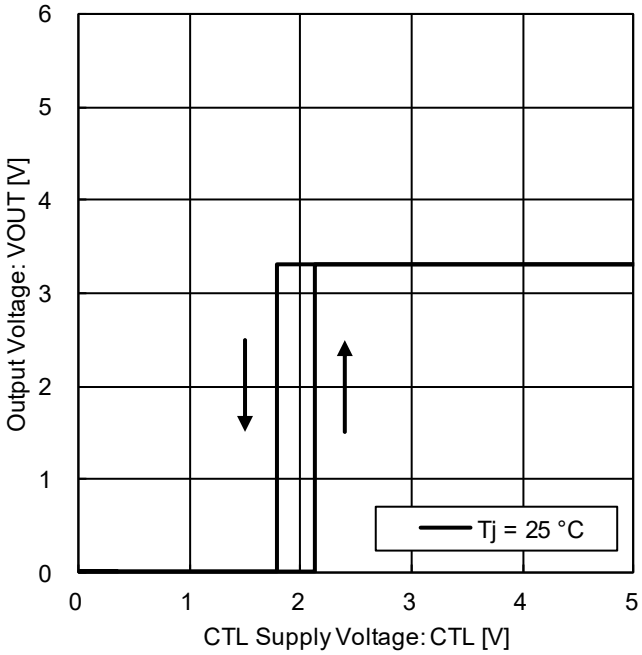


Figure 18. CTL ON / OFF Mode Voltage (Tj = 25 °C)

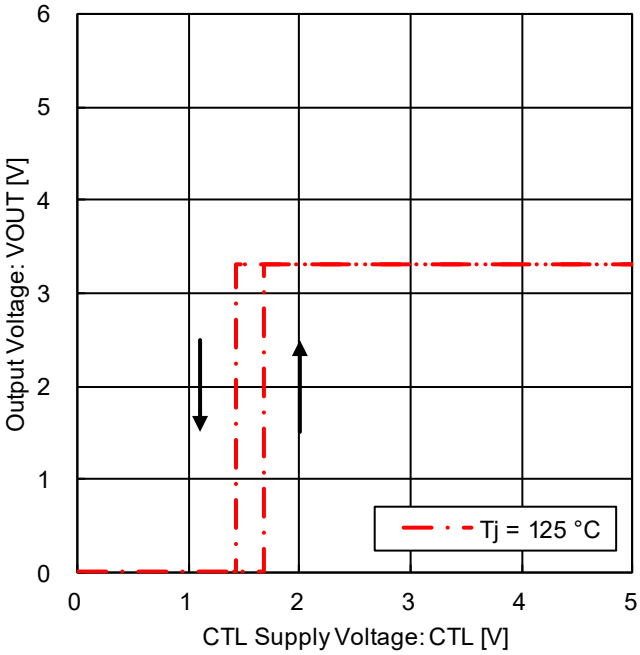


Figure 19. CTL ON / OFF Mode Voltage (Tj = 125 °C)

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Typical Performance Curves (Reference Data) – continued

■For 3.3 V Output with Enable input products

■Applicable Model:BD433S5WFP-C, BD433S5WFP2-C, BD433S5WEFJ-C

Unless otherwise specified: -40 °C ≤ Tj ≤ +150 °C, VCC = 13.5 V, IOUT = 0 mA

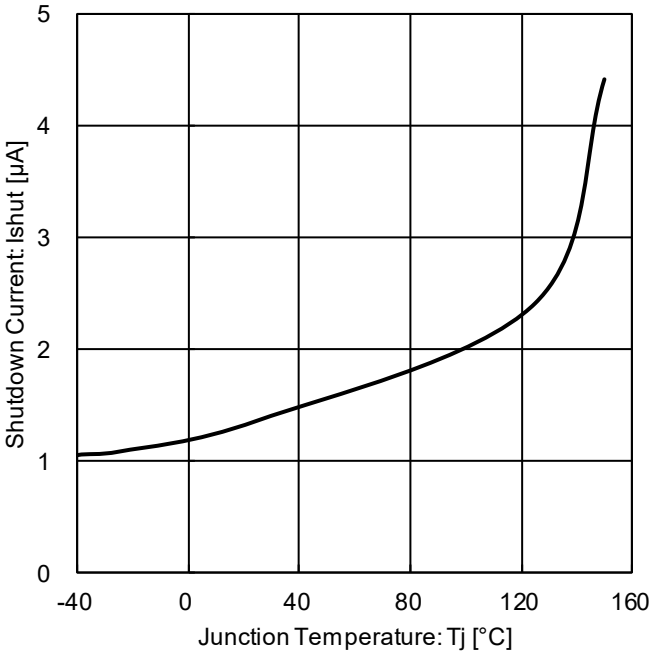


Figure 20. Shutdown Current
(CTL = 0 V)

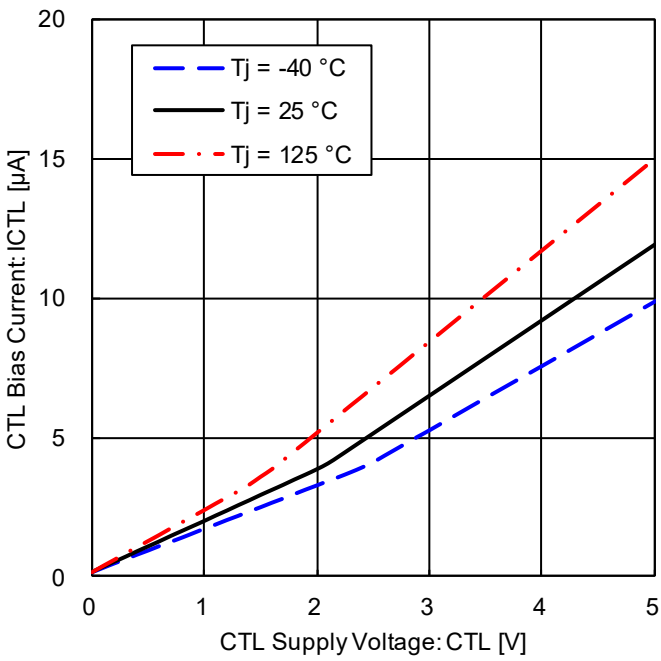


Figure 21. CTL Bias Current vs CTL Supply Voltage

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Typical Performance Curves (Reference Data) – continued

■For 5.0 V Output products

■Applicable Models:BD450S5FP-C, BD450S5WFP-C, BD450S5FP2-C, BD450S5WFP2-C, BD450S5EFJ-C, BD450S5WEFJ-C

Unless otherwise specified: -40 °C ≤ Tj ≤ +150 °C, VCC = 13.5 V, CTL = 5 V(Note 1), IOUT = 0 mA.

(Note 1) Applicable for product with Enable Input

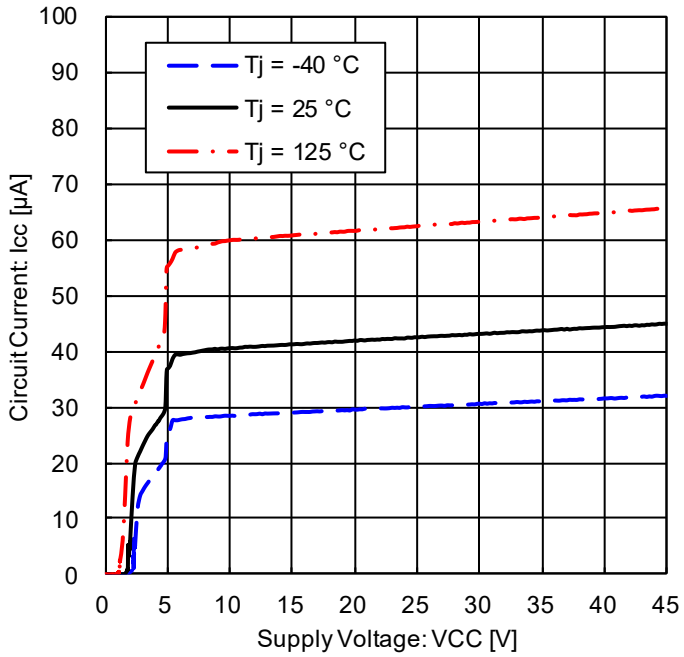


Figure 22. Circuit Current vs Power Supply Voltage

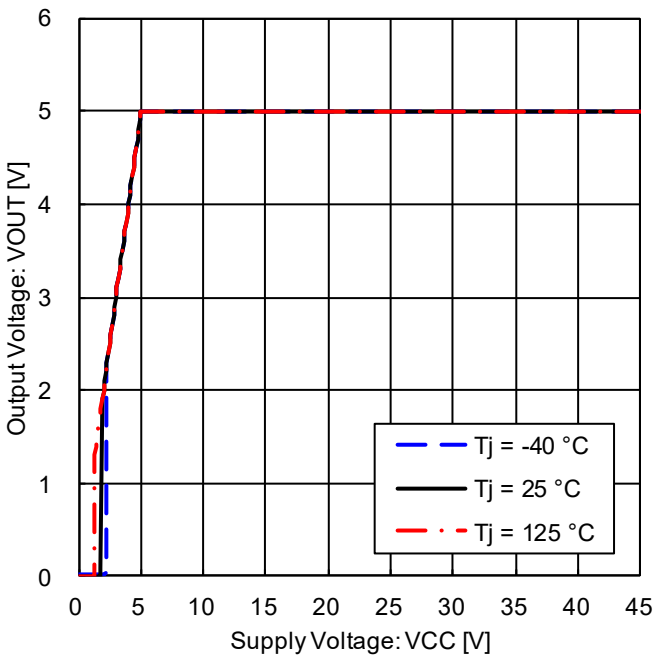


Figure 23. Output Voltage vs Power Supply Voltage (IOUT = 0 mA)

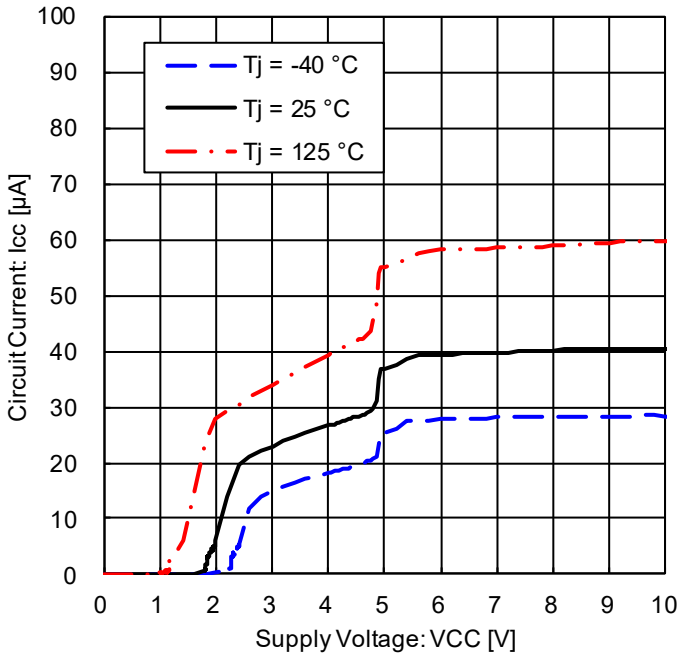


Figure 24. Circuit Current vs Power Supply Voltage - Magnified Figure 22.

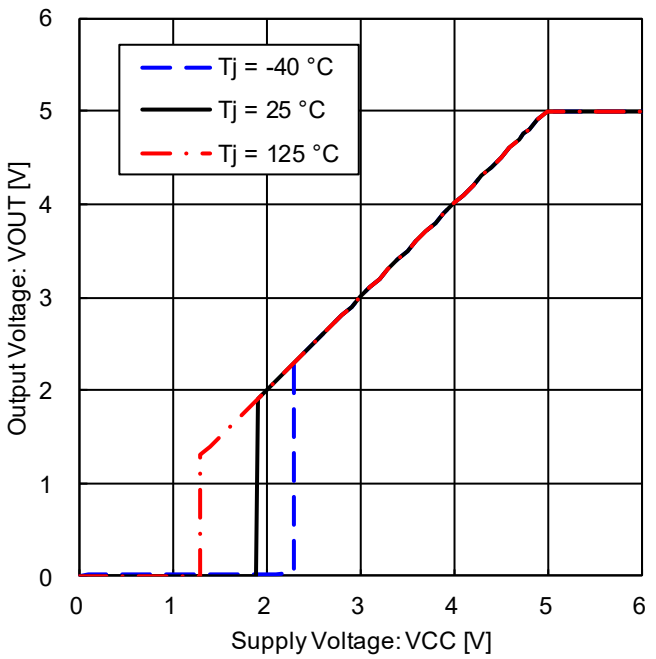


Figure 25. Output Voltage vs Power Supply Voltage (IOUT = 0 mA) - Magnified Figure 23.

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Typical Performance Curves (Reference Data) – continued

■For 5.0 V Output products

■Applicable Models:BD450S5FP-C, BD450S5WFP-C, BD450S5FP2-C, BD450S5WFP2-C, BD450S5EFJ-C, BD450S5WEFJ-C

Unless otherwise specified: -40 °C ≤ Tj ≤ +150 °C, VCC = 13.5 V, CTL = 5 V(Note 1), IOUT = 0 mA.

(Note 1) Applicable for product with Enable Input

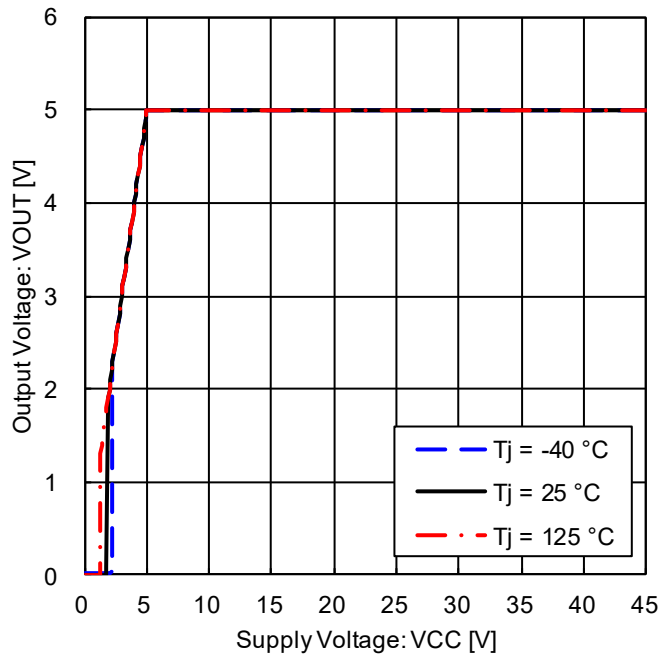


Figure 26. Output Voltage vs Power Supply Voltage (IOUT = 10 mA)

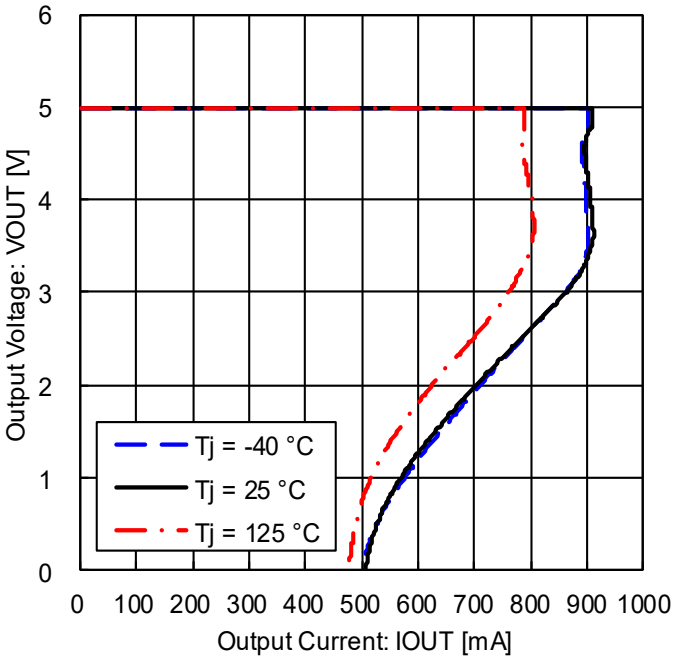


Figure 27. Output Voltage vs Output Current (Over Current Protection)

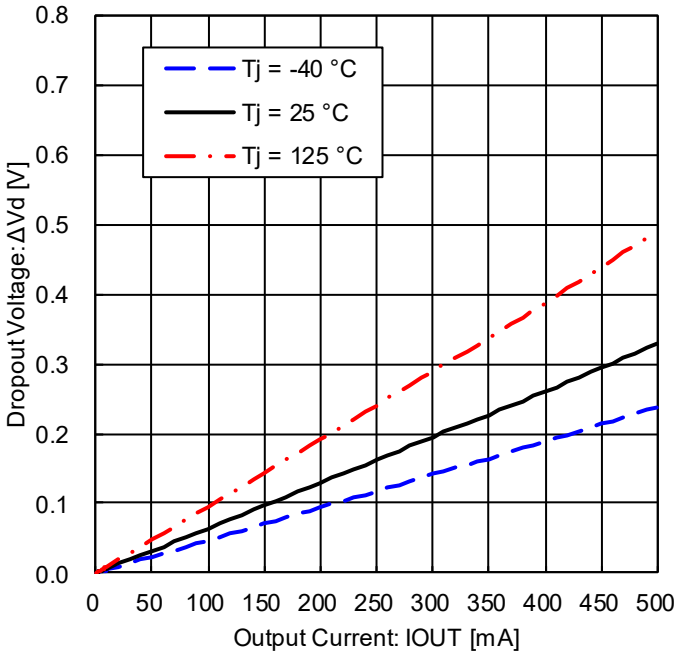


Figure 28. Dropout Voltage (VCC = 4.75 V)

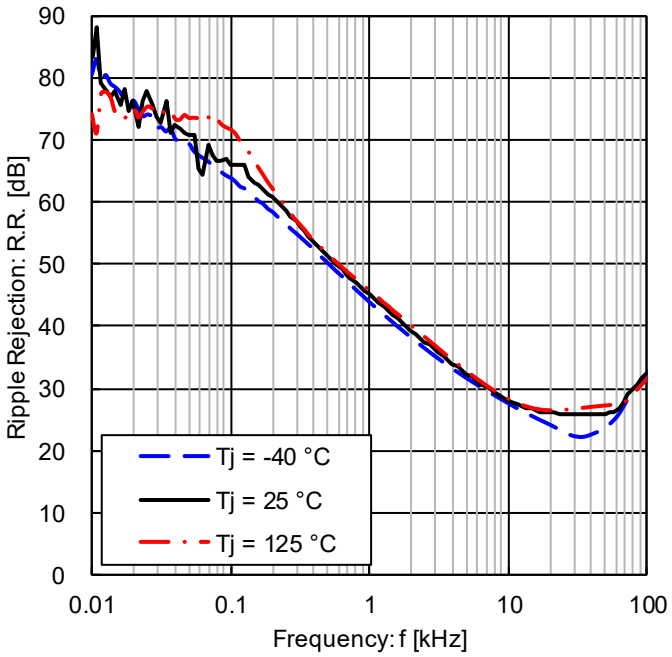


Figure 29. Ripple Rejection (ein = 1 Vrms, IOUT = 100 mA)

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Typical Performance Curves (Reference Data) – continued

■For 5.0 V Output products

■Applicable Models:BD450S5FP-C, BD450S5WFP-C, BD450S5FP2-C, BD450S5WFP2-C, BD450S5EFJ-C, BD450S5WEFJ-C

Unless otherwise specified: -40 °C ≤ Tj ≤ +150 °C, VCC = 13.5 V, CTL = 5 V(Note 1), IOUT = 0 mA.

(Note 1) Applicable for product with Enable Input

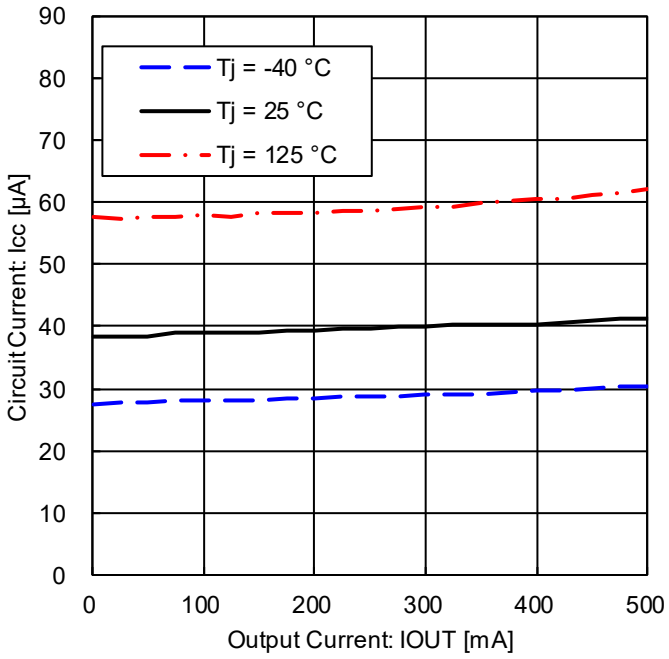


Figure 30. Circuit Current vs Output Current

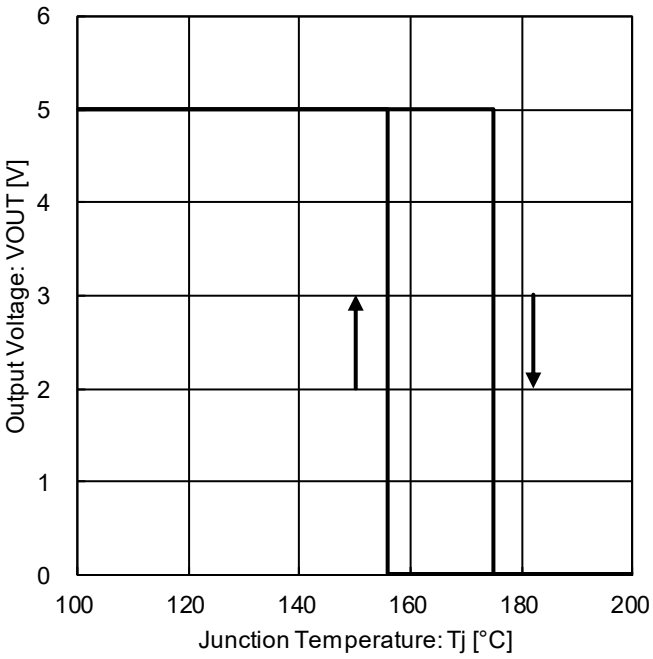


Figure 31. Output Voltage vs Temperature (Thermal Shutdown)

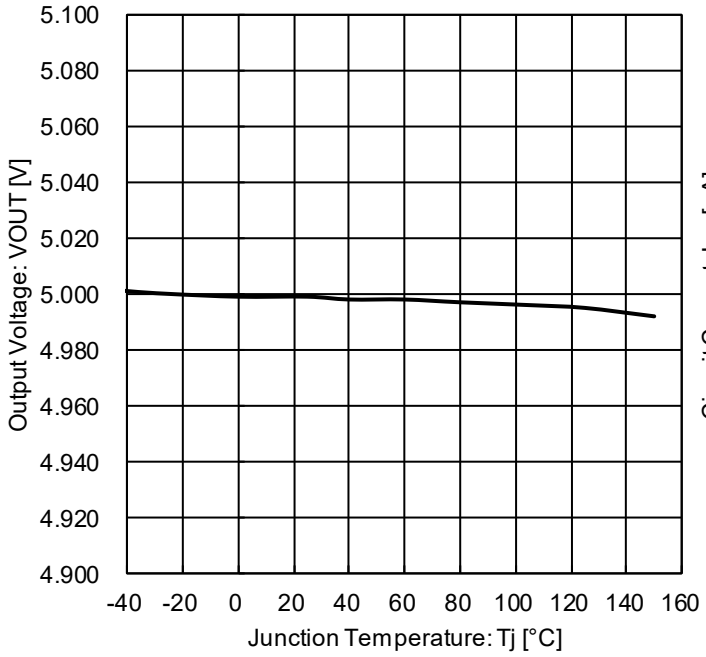


Figure 32. Output Voltage vs Temperature

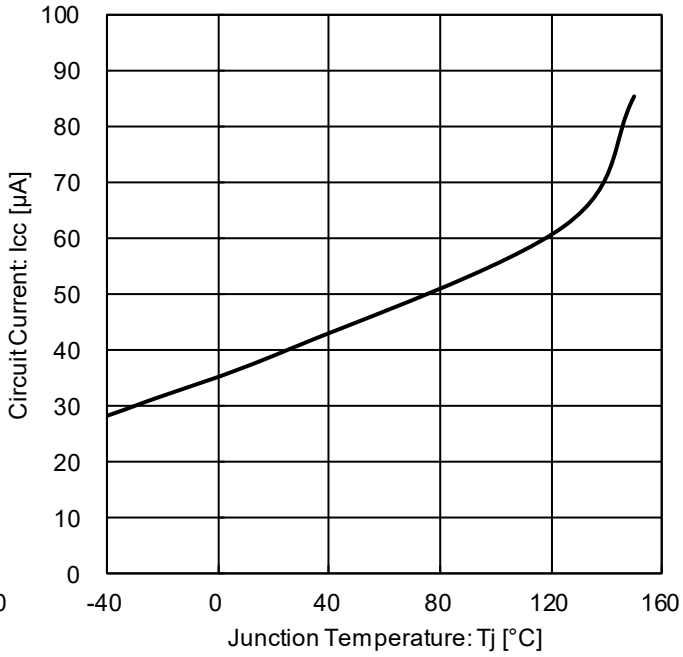


Figure 33. Circuit Current vs Temperature

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Typical Performance Curves (Reference Data) – continued

■For 5.0 V Output with Enable input products

■Applicable Model:BD450S5WFP-C, BD450S5WFP2-C, BD450S5WEFJ-C

Unless otherwise specified: -40 °C ≤ Tj ≤ +150 °C, VCC = 13.5 V, IOUT = 0 mA

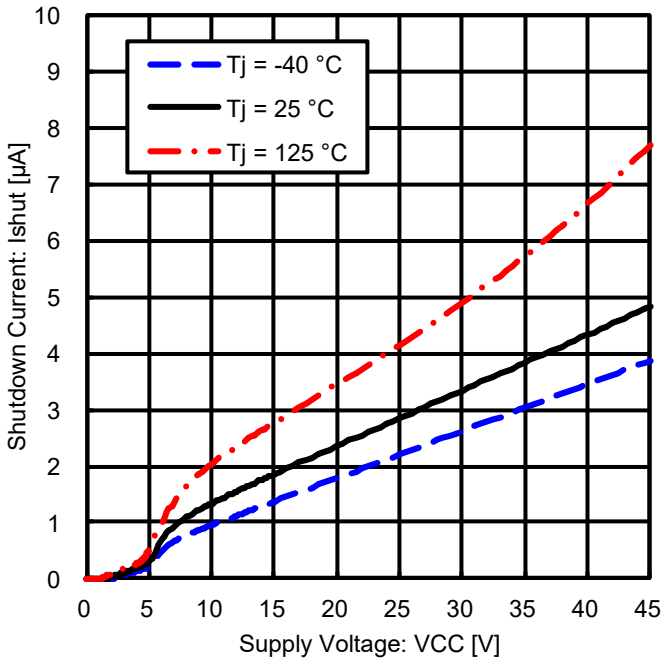


Figure 34. Shutdown Current vs Power Supply Voltage
(CTL = 0 V)

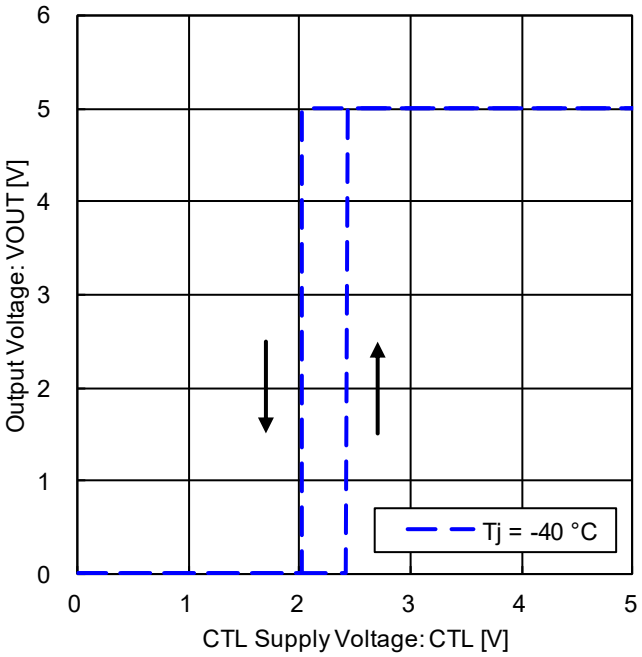


Figure 35. CTL ON / OFF Mode Voltage
(Tj = -40 °C)

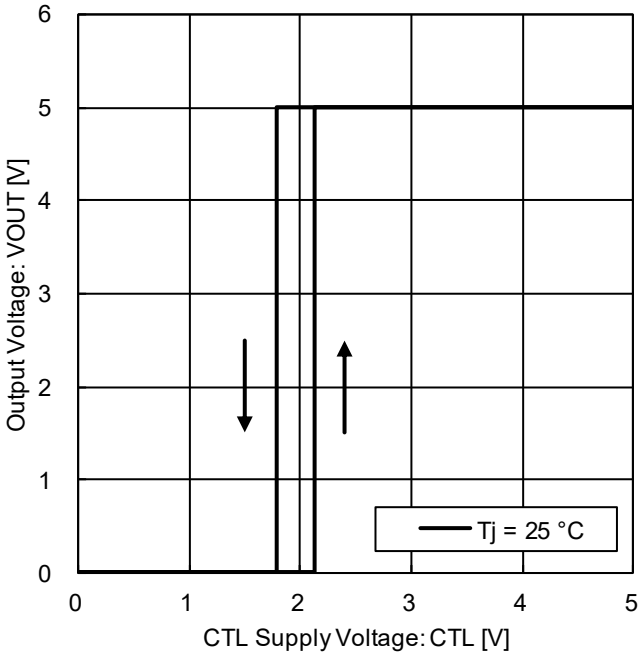


Figure 36. CTL ON / OFF Mode Voltage
(Tj = 25 °C)

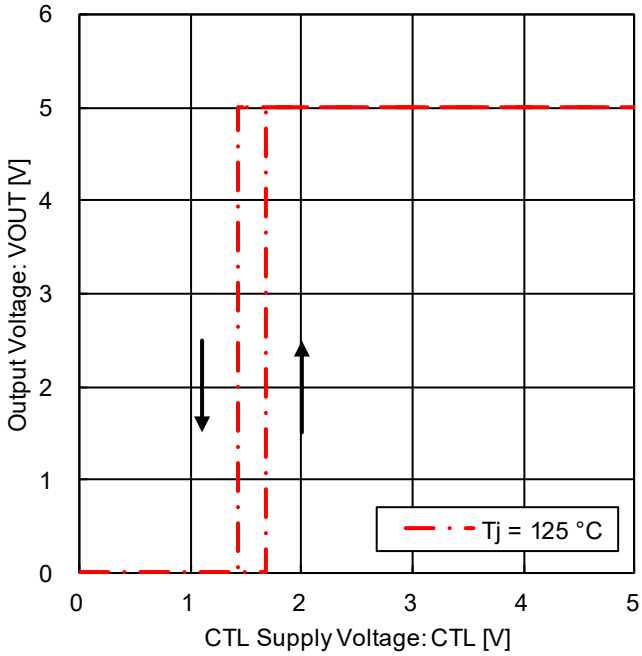


Figure 37. CTL ON / OFF Mode Voltage
(Tj = 125 °C)

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Typical Performance Curves (Reference Data) – continued

■For 5.0 V Output with Enable input products

■Applicable Model:BD450S5WFP-C, BD450S5WFP2-C, BD450S5WEFJ-C

Unless otherwise specified: -40 °C ≤ Tj ≤ +150 °C, VCC = 13.5 V, IOUT = 0 mA

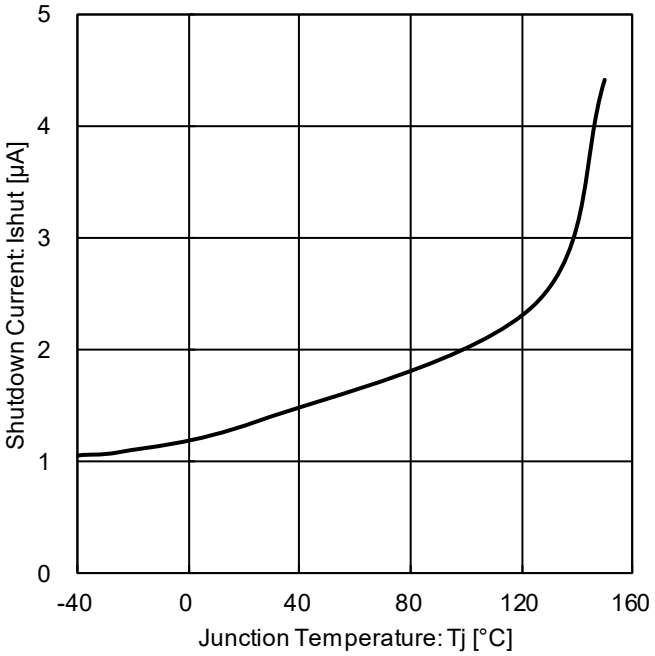


Figure 38. Shutdown Current vs Temperature (CTL = 0 V)

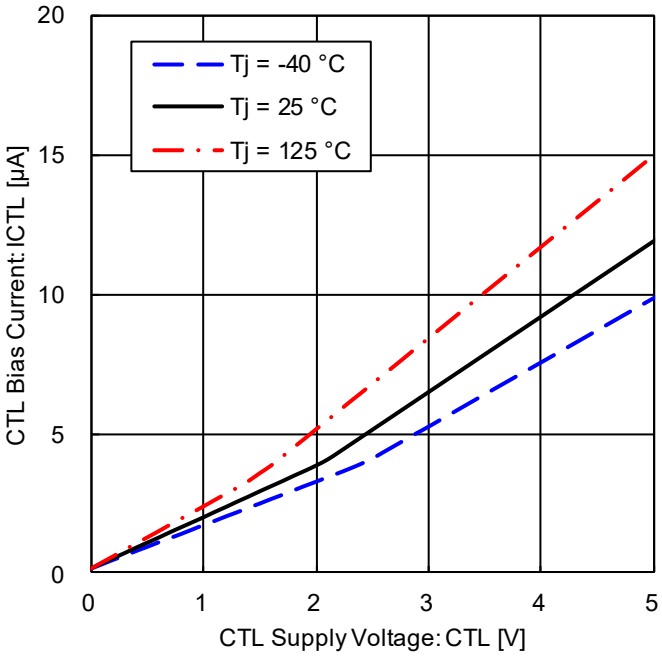
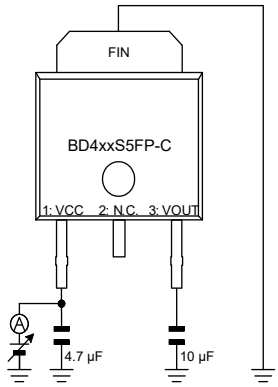


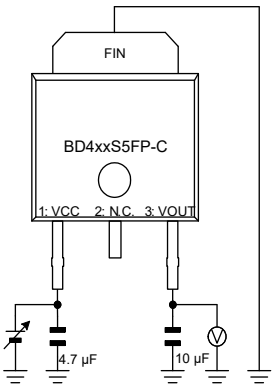
Figure 39. CTL Bias Current vs CTL Supply Voltage

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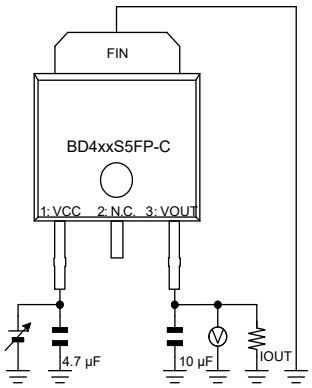
Measurement Circuit for Typical Performance Curves (BD4xxS5FP-C)



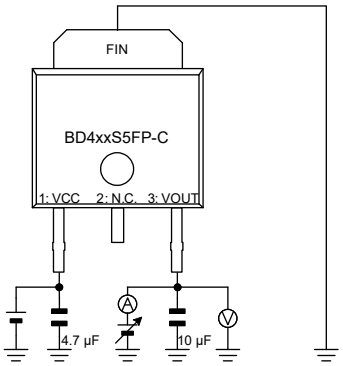
Measurement Setup for
Figure 4, 6, 15,
Figure 22, 24, 33



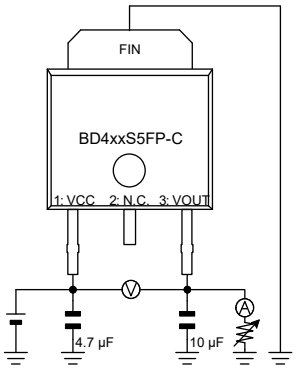
Measurement Setup for
Figure 5, 7, 13, 14,
Figure 23, 25, 31, 32



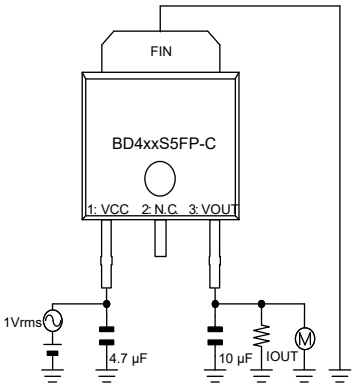
Measurement Setup for
Figure 8, 26



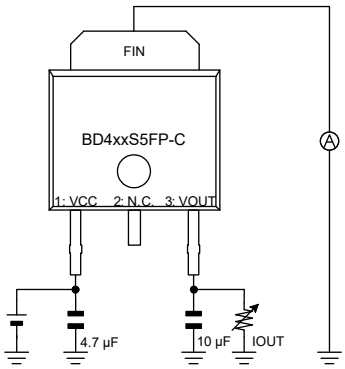
Measurement Setup for
Figure 9, 27



Measurement Setup for
Figure 10, 28



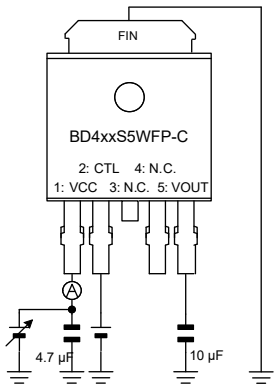
Measurement Setup for
Figure 11, 29



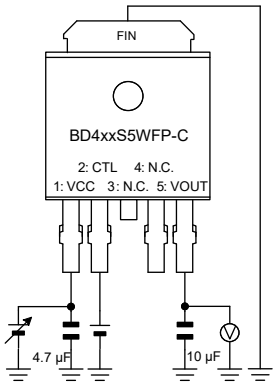
Measurement Setup for
Figure 12, 30

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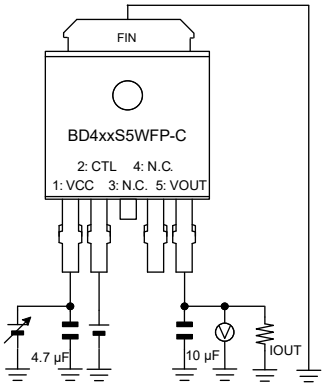
Measurement Circuit for Typical Performance Curves (BD4xxS5WFP-C) – continued



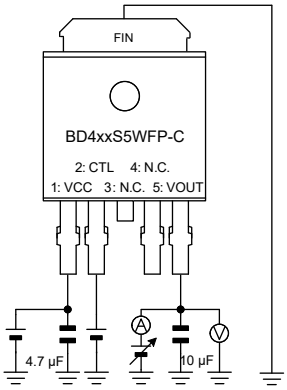
Measurement Setup for
Figure 4, 6, 15, 16, 20,
Figure 22, 24, 33, 34, 38



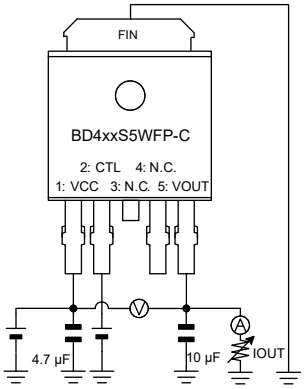
Measurement Setup for
Figure 5, 7, 13, 14,
Figure 23, 25, 31, 32



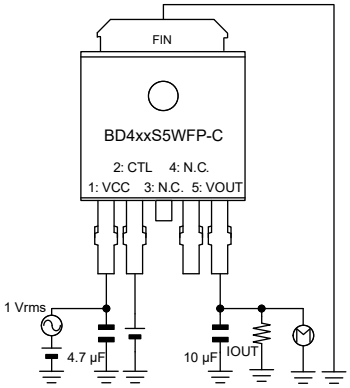
Measurement Setup for
Figure 8, 26



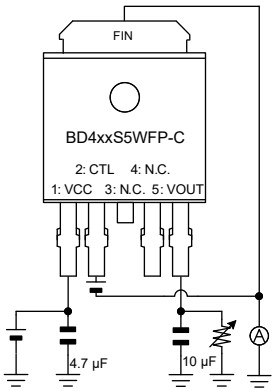
Measurement Setup for
Figure 9, 27



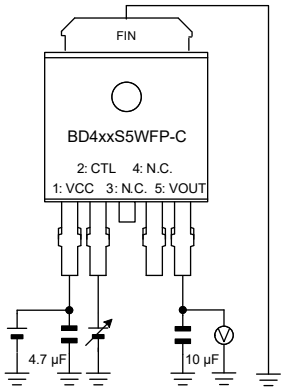
Measurement Setup for
Figure 10, 28



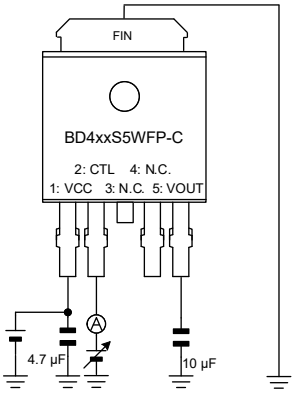
Measurement Setup for
Figure 11, 29



Measurement Setup for
Figure 12, 30



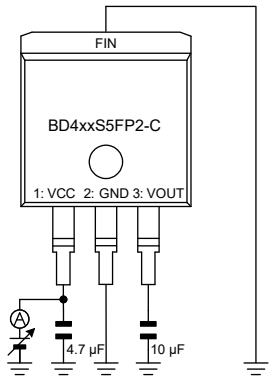
Measurement Setup for
Figure 17, 18, 19,
Figure 35, 36, 37



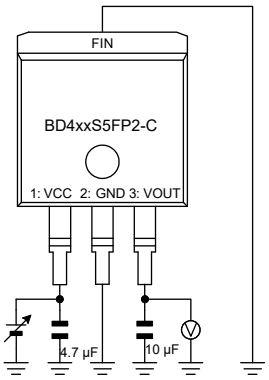
Measurement Setup for
Figure 21, 39

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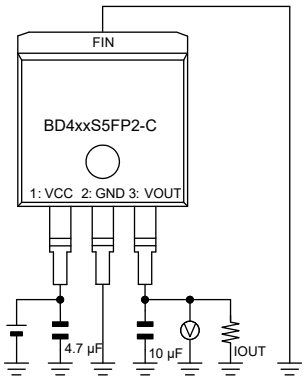
Measurement Circuit for Typical Performance Curves (BD4xxS5FP2-C) – continued



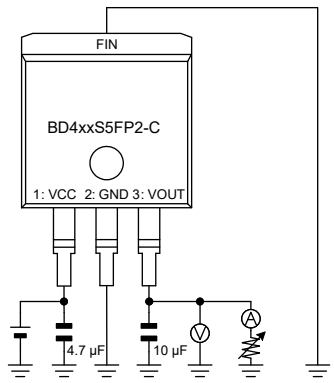
Measurement Setup for
Figure 4, 6, 15,
Figure 22, 24, 33



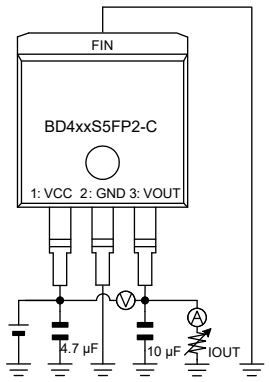
Measurement Setup for
Figure 5, 7, 13, 14,
Figure 23, 25, 31, 32



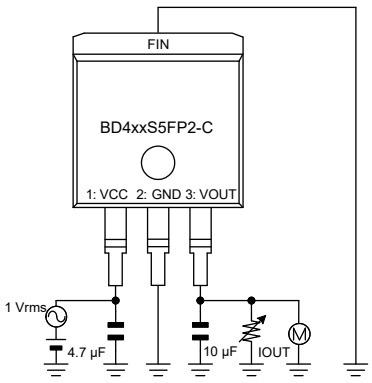
Measurement Setup for
Figure 8, 26



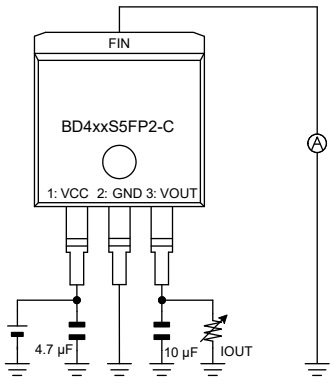
Measurement Setup for
Figure 9, 27



Measurement Setup for
Figure 10, 28



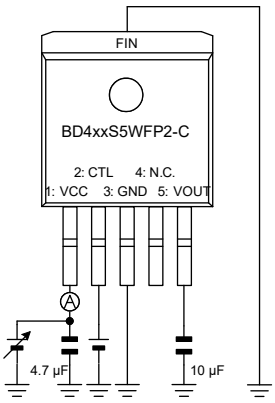
Measurement Setup for
Figure 11, 29



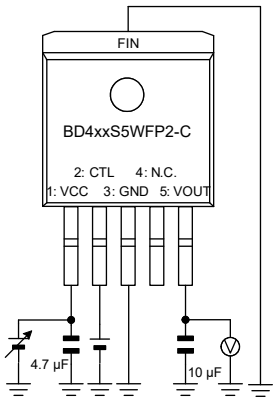
Measurement Setup for
Figure 12, 30

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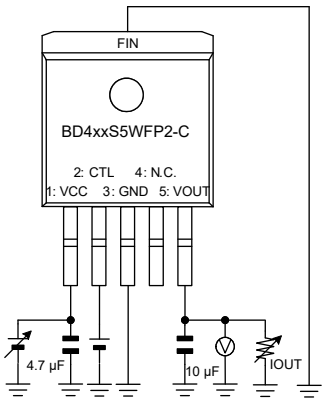
Measurement Circuit for Typical Performance Curves (BD4xxS5WFP2-C) – continued



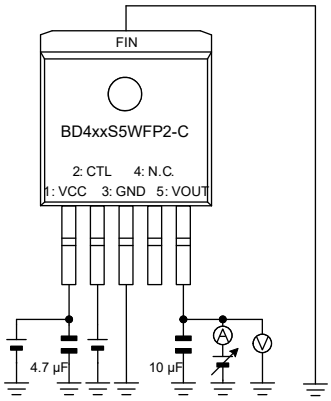
Measurement Setup for
Figure 4, 6, 15, 16, 20,
Figure 22, 24, 33, 34, 38



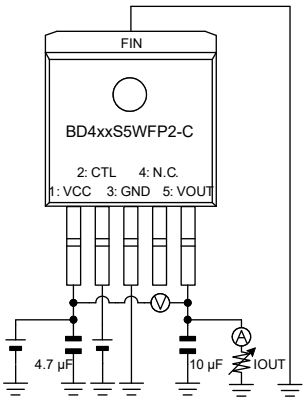
Measurement Setup for
Figure 5, 7, 13, 14,
Figure 23, 25, 31, 32



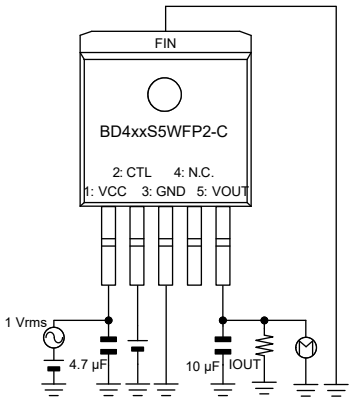
Measurement Setup for
Figure 8, 26



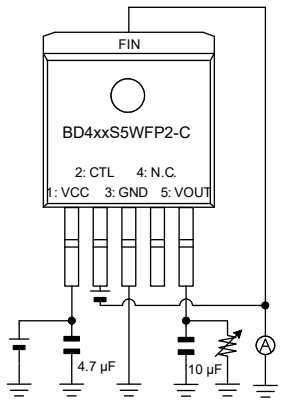
Measurement Setup for
Figure 9, 27



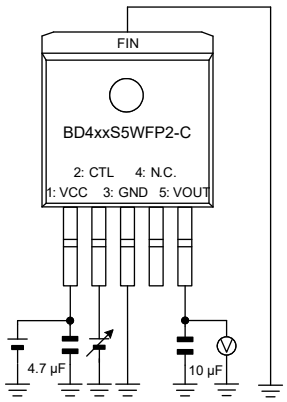
Measurement Setup for
Figure 10, 28



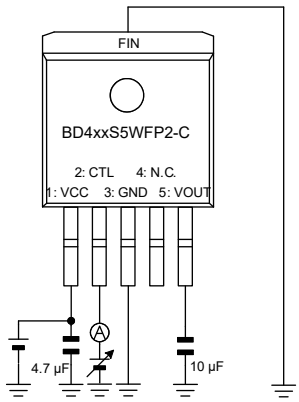
Measurement Setup for
Figure 11, 29



Measurement Setup for
Figure 12, 30



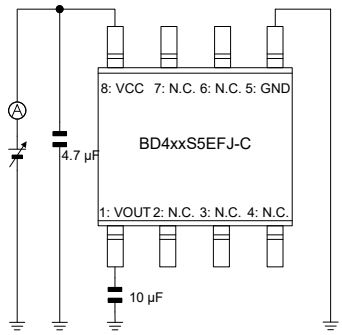
Measurement Setup for
Figure 17, 18, 19,
Figure 35, 36, 37



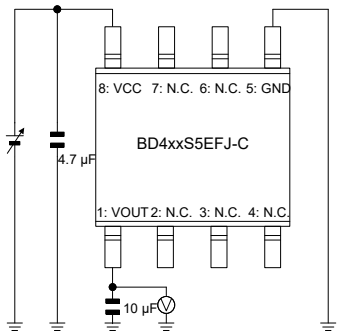
Measurement Setup for
Figure 21, 39

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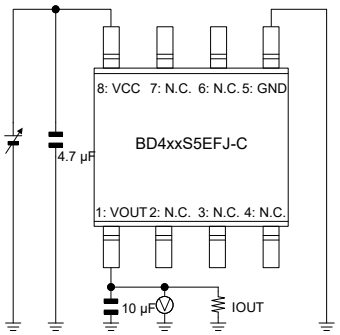
Measurement Circuit for Typical Performance Curves (BD4xxS5EFJ-C) – continued



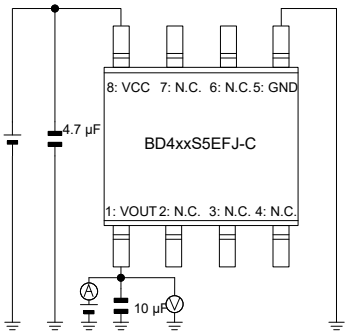
Measurement Setup for
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Figure 22, 24, 33



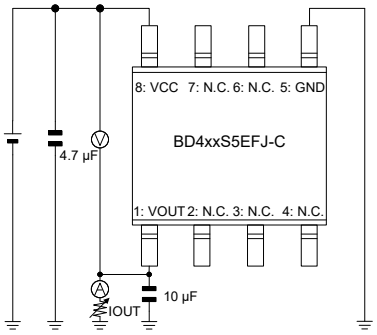
Measurement Setup for
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Figure 23, 25, 31, 32



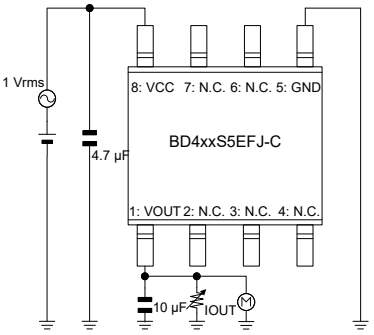
Measurement Setup for
Figure 8, 26



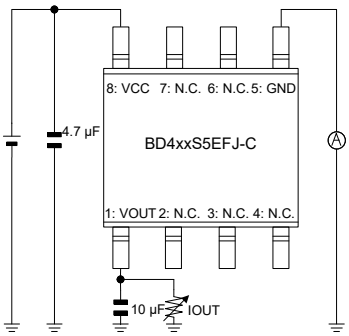
Measurement Setup for
Figure 9, 27



Measurement Setup for
Figure 10, 28



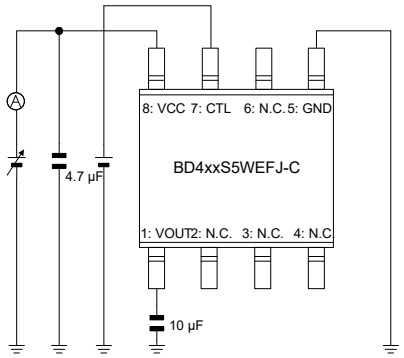
Measurement Setup for
Figure 11, 29



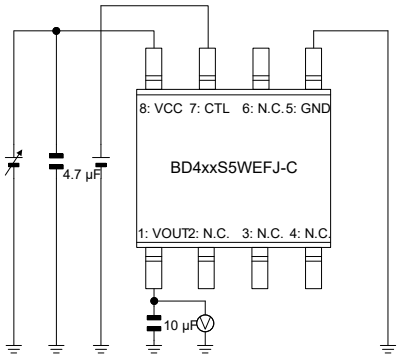
Measurement Setup for
Figure 12, 30

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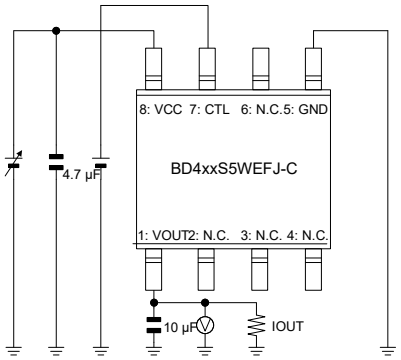
Measurement Circuit for Typical Performance Curves (BD4xxS5WEFJ-C) – continued



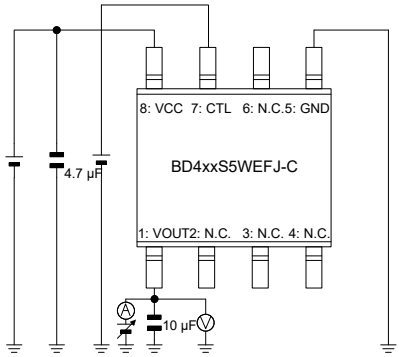
Measurement Setup for
Figure 4, 6, 15, 16, 20,
Figure 22, 24, 33, 34, 38



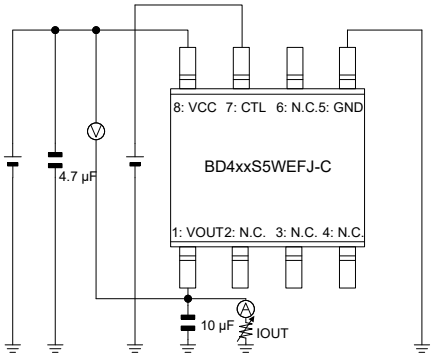
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Figure 23, 25, 31, 32



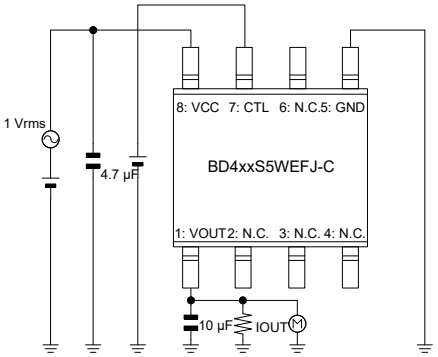
Measurement Setup for
Figure 8, 26



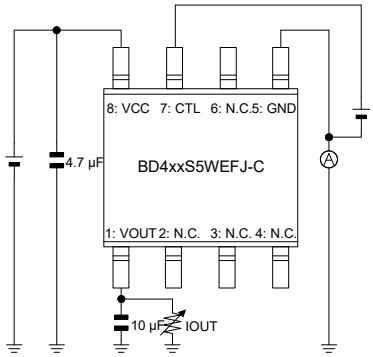
Measurement Setup for
Figure 9, 27



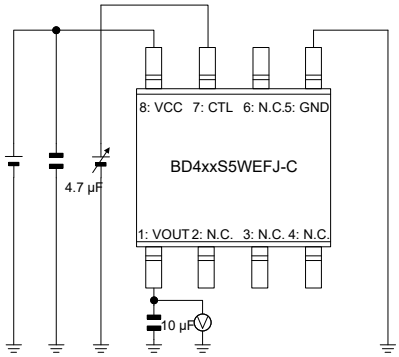
Measurement Setup for
Figure 10, 28



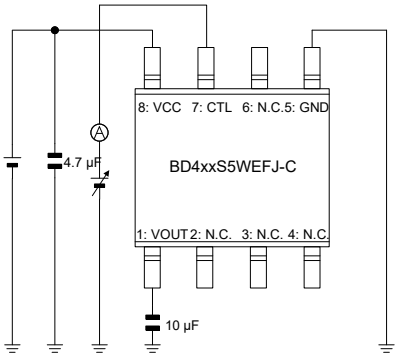
Measurement Setup for
Figure 11, 29



Measurement Setup for
Figure 12, 30



Measurement Setup for
Figure 17, 18, 19,
Figure 35, 36, 37



Measurement Setup for
Figure 21, 39

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Selection of Components Externally Connected

VCC

Insert capacitors with a capacitance of 0.1 µF or higher between the VCC and the GND. Choose the capacitance according to the line between the power smoothing circuit and the VCC. Selection of the capacitance also depends on the application. Verify the application and allow sufficient margins in the design. We recommend using a capacitor with excellent voltage and temperature characteristics.

Output Pin Capacitor

In order to prevent oscillation, a capacitor needs to be placed between the output pin and GND. We recommend using a capacitor with a capacitance of 10 µF (Typ) or higher. Electrolytic, tantalum and ceramic capacitors can be used. When selecting the capacitor ensure that the capacitance of 6 µF or higher is maintained at the intended applied voltage and temperature range. Due to changes in temperature the capacitor's capacitance can fluctuate possibly resulting in oscillation. For selection of the capacitor refer to the data of Figure 40.

The stable operation range given in the data of Figure 40 and Figure 41 is based on the standalone IC and resistive load. For actual applications the stable operating range is influenced by the PCB impedance, input supply impedance and load impedance. Therefore verification of the final operating environment is needed.

When selecting a ceramic type capacitor, we recommend using X5R, X7R or better with excellent temperature and DC-biasing characteristics and high voltage tolerance.

Also, in case of rapidly fluctuation of input voltage and load current, select the capacitance in accordance with verifying that the actual application meets with the required specification. Mount the capacitor as much as possible near connected pin.

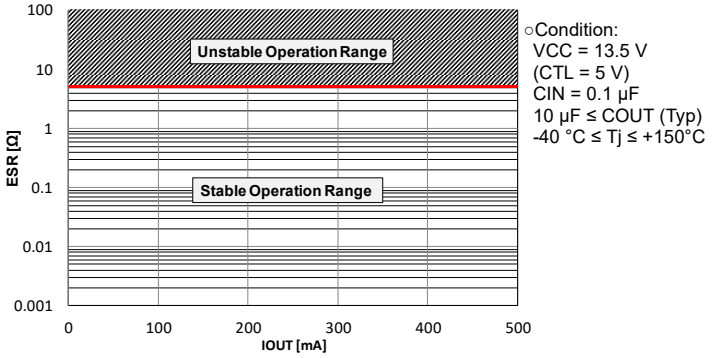


Figure 40. ESR vs IOUT

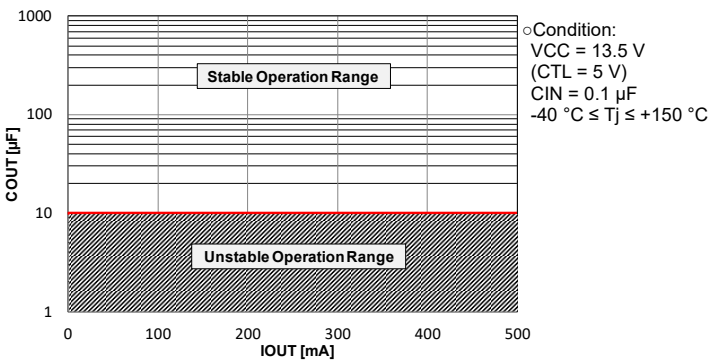


Figure 41. COUT (Typ) vs IOUT

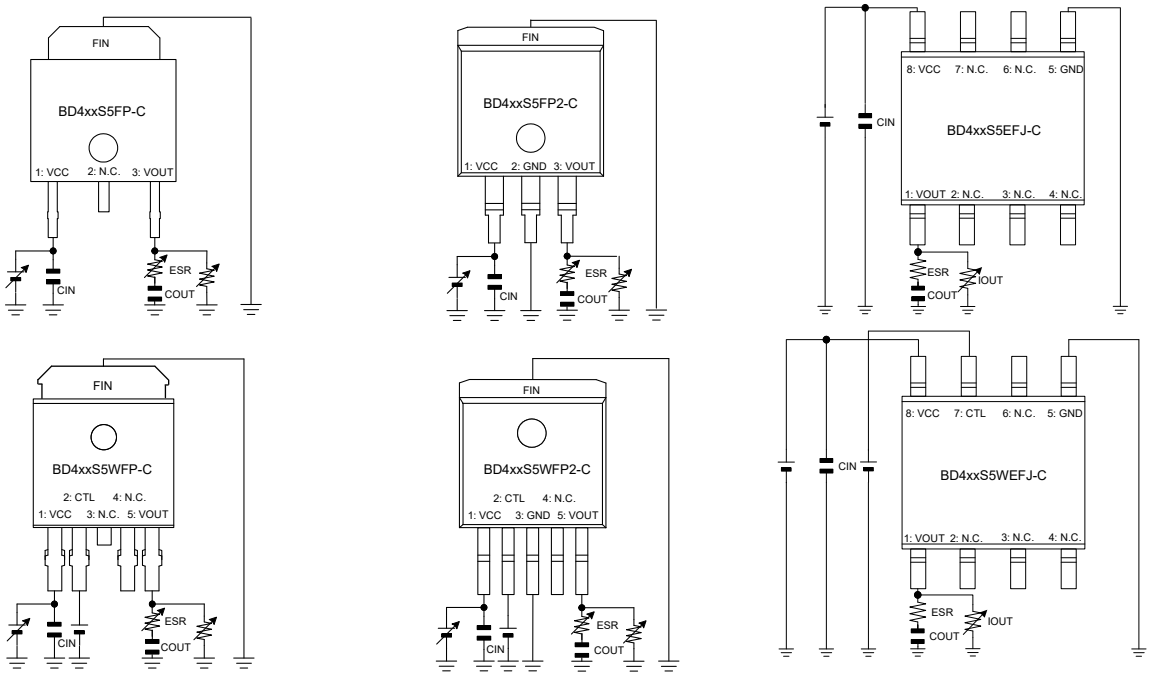


Figure 42. Measurement Setups for ESR Reference Data

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Selection of Components Externally Connected – continued

Surge Voltage Protection for Linear Regulators

The following shows some helpful tips to protect ICs from possible inputting surge voltage which exceeds absolute maximum ratings.

Positive Surge to the Input

If there is any potential risk that positive surges higher than absolute maximum ratings, it is applied to the input, a Zener Diode should be inserted between the VCC pin and the GND to protect the device as shown in Figure 43.

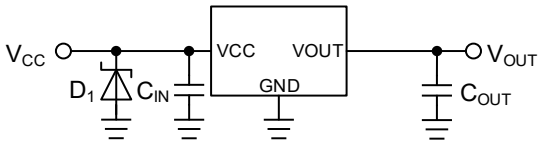


Figure 43. Surges Higher than absolute maximum ratings are Applied to the Input

Negative Surge to the Input

If there is any potential risk that negative surges below the absolute maximum ratings, (e.g.) -0.3 V, is applied to the input, a Schottky Diode should be inserted between the VCC and the GND to protect the device as shown in Figure 44.

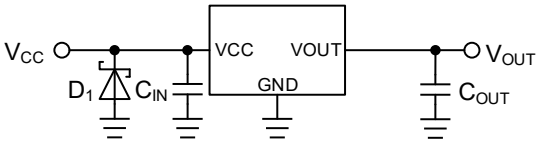


Figure 44. Surges Lower than -0.3 V is Applied to the Input

Reverse Voltage Protection for Linear Regulators

A linear regulator which is one of the integrated circuit (IC) operates normally in the condition that the input voltage is higher than the output voltage. However, it is possible to happen the abnormal situation in specific conditions which is the output voltage becomes higher than the input voltage. A reverse polarity connection between the input and the output might be occurred or a certain inductor component can also cause a polarity reverse conditions. If the countermeasure is not implemented, it may cause damage to the IC. In this case, use a capacitor with a capacitance with less than 1000 µF, to reduce damage to internal circuits or elements. The following shows some helpful tips to protect ICs from the reverse voltage occasion.

Protection against Reverse Input/Output Voltage

In the case that MOSFET is used for the pass transistor, a parasitic body diode between the drain-source generally exists. If the output voltage becomes higher than the input voltage and if its voltage difference exceeds V_F of the body diode, a reverse current flows from the output to the input through the body diode as shown in Figure 45. The current flows in the parasitic body diode is not limited in the protection circuit because it is the parasitic element, therefore too much reverse current may cause damage to degrade or destroy the semiconductor elements of the regulator.

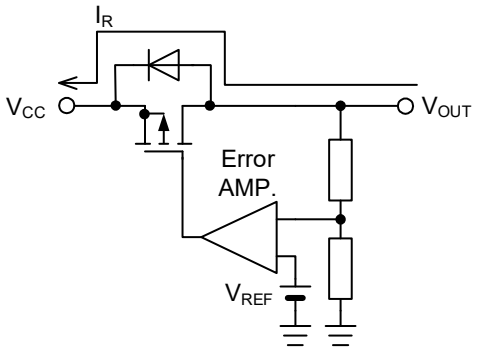


Figure 45. Reverse Current Path in a MOS Linear Regulator

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Protection against Reverse Input/Output Voltage – continued

An effective solution for this problem is to implement an external bypass diode in order to prevent the reverse current flow inside the IC as shown in Figure 46. Especially in applications where the output voltage setting is high and a large output capacitor is connected, be sure to consider countermeasures for large reverse current values. Note that the bypass diode must be turned on prior to the internal body diode of the IC. This external bypass diode should be chosen as being lower forward voltage V_F than the internal body diode. It should to be selected a diode which has a rated reverse voltage greater than the IC's input maximum rating voltage and also which has a rated forward current greater than the anticipated reverse current in the actual application.

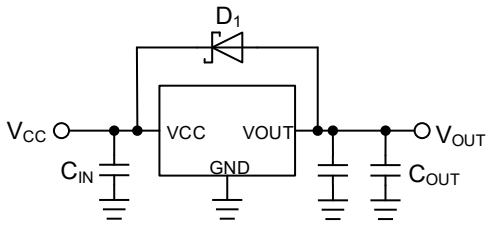


Figure 46. Bypass Diode for Reverse Current Diversion

A Schottky barrier diode which has a characteristic of low forward voltage (V_F) can meet to the requirement for the external diode to protect the IC from the reverse current. However, it also has a characteristic that the leakage (I_R) caused by the reverse voltage is bigger than other diodes. Therefore, it should be taken into the consideration to choose it because if I_R is large, it may cause increase of the current consumption, or raise of the output voltage in the light-load current condition. I_R characteristic of Schottky diode has positive temperature characteristic, which the details shall be checked with the datasheet of the products, and the careful confirmation of behavior in the actual application is mandatory.

Even in the condition when the input/output voltage is inverted, if the VCC pin is open as shown in Figure 47, or if the VIN pin becomes high-impedance condition as designed in the system, it cannot damage or degrade the parasitic element. It's because a reverse current via the pass transistor becomes extremely low. In this case, therefore, the protection external diode is not necessary.

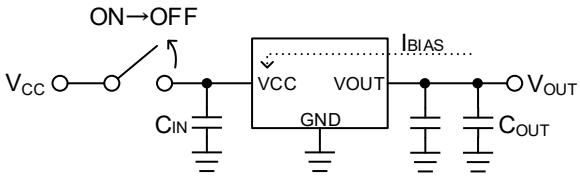


Figure 47. Open VIN

Protection against Input Reverse Voltage

When the input of the IC is connected to the power supply, accidentally if plus and minus are routed in reverse, or if there is a possibility that the input may become lower than the GND pin, it may cause to destroy the IC because a large current passes via the internal electrostatic breakdown prevention diode between the input pin and the GND pin inside the IC as shown in Figure 48.

The simplest solution to avoid this problem is to connect a Schottky barrier diode or a rectifier diode in series to the power supply line as shown in Figure 49. However, it causes the voltage drop by a forward voltage V_F at the supply voltage while normal operation.
Generally, since the Schottky barrier diode has lower V_F, so it contributes to rather smaller power loss than rectifier diodes. If IC has load currents, the required input current to the IC is also bigger. In this case, this external diode generates heat more, therefore select a diode with enough margin in power dissipation. On the other hand, a reverse current passes this diode in the reverse connection condition, however, it is negligible because its small amount.

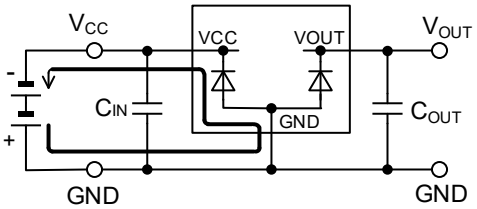


Figure 48. Current Path in Reverse Input Connection

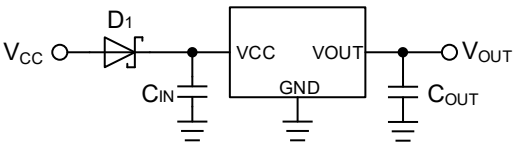


Figure 49. Protection against Reverse Polarity 1

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Protection against Input Reverse Voltage – continued

Figure 50 shows a circuit in which a P-channel MOSFET is connected in series to the power. The body diode (parasitic element) is located in the drain-source junction area of the MOSFET. The drop voltage in a forward connection is calculated from the on state resistance of the MOSFET and the output current I_O. It is smaller than the drop voltage by the diode as shown in Figure 49 and results in less of a power loss. No current flows in a reverse connection where the MOSFET remains off in Figure 50.

If the gate-source voltage exceeds maximum rating of MOSFET gate-source junction with derating curve in consideration, reduce the gate-source junction voltage by connecting resistor voltage divider as shown in Figure 51.

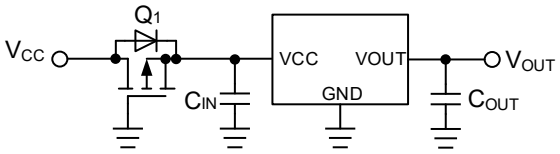


Figure 50. Protection against Reverse Polarity 2

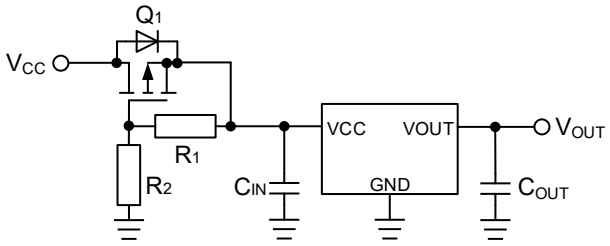


Figure 51. Protection against Reverse Polarity 3

Protection against Reverse Output Voltage when Output Connect to an Inductor

If the output load is inductive, electrical energy accumulated in the inductive load is released to the ground at the moment that the output voltage is turned off. IC integrates ESD protection diodes between the IC output and ground pins. A large current may flow in such condition finally resulting on destruction of the IC. To prevent this situation, connect a Schottky barrier diode in parallel to the integrated diodes as shown in Figure 52.

Further, if a long wire is in use for the connection between the output pin of the IC and the load, confirm that the negative voltage is not generated at the VOUT pin when the output voltage is turned off by observation of the waveform on an oscilloscope, since it is possible that the load becomes inductive. An additional diode is required for a motor load that is affected by its counter electromotive force, as it produces an electrical current in a similar way.

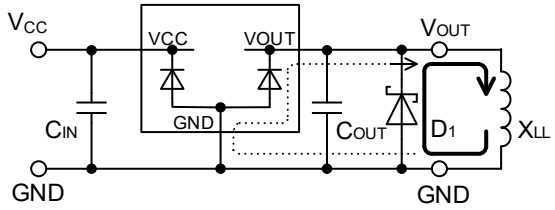


Figure 52. Current Path in Inductive Load (Output: Off)

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Power Dissipations

■TO252-3 / TO252-5

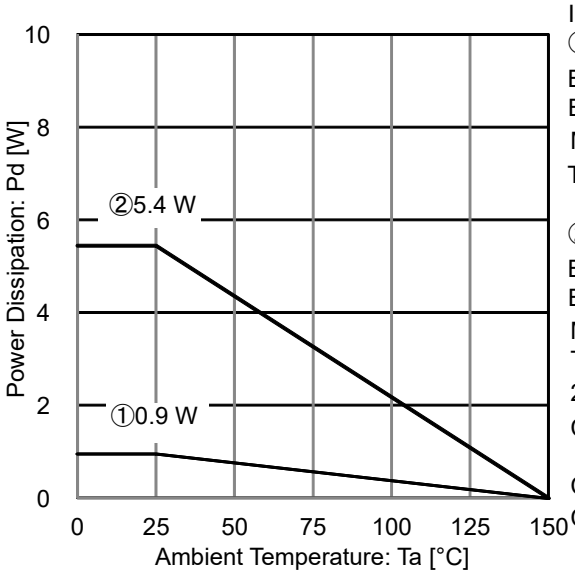


Figure 53. Package Data
(TO252-3 / TO252-5)

IC mounted on ROHM standard board based on JEDEC.
①: 1-layer PCB (Copper foil area on the reverse side of PCB: 0 mm × 0 mm)
Board material: FR4
Board size: 114.3 mm × 76.2 mm × 1.57 mmt
Mount condition: PCB and exposed pad are soldered.
Top copper foil: ROHM recommended footprint + wiring to measure, 2 oz. copper.

②: 4-layer PCB (Copper foil area on the reverse side of PCB: 74.2 mm × 74.2 mm)
Board material: FR4
Board size: 114.3 mm × 76.2 mm × 1.60 mmt
Mount condition: PCB and exposed pad are soldered.
Top copper foil: ROHM recommended footprint + wiring to measure, 2 oz. copper.
2 inner layers copper foil area of PCB: 74.2 mm × 74.2 mm, 1 oz. copper.
Copper foil area on the reverse side of PCB: 74.2 mm × 74.2 mm, 2 oz. copper.

Condition①: θ_{JA} = 136 °C/W, Ψ_{JT} (top center) = 17 °C/W
Condition②: θ_{JA} = 23 °C/W, Ψ_{JT} (top center) = 3 °C/W

■TO263-3 / TO263-5

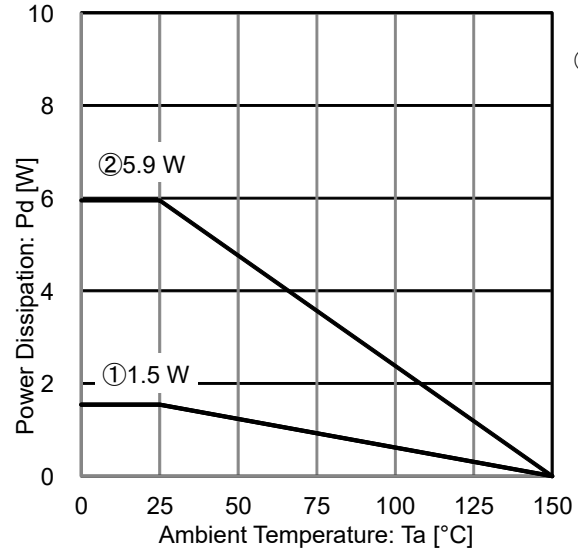


Figure 54. Package Data
(TO263-3 / TO263-5)

IC mounted on ROHM standard board based on JEDEC.
①1-layer PCB (Copper foil area on the reverse side of PCB: 0 mm × 0 mm)
Board material: FR4
Board size: 114.3 mm × 76.2 mm × 1.57 mmt
Mount condition: PCB and exposed pad are soldered.
Top copper foil: ROHM recommended footprint + wiring to measure, 2 oz. copper.

②4-layer PCB (Copper foil area on the reverse side of PCB: 74.2 mm × 74.2 mm)
Board material: FR4
Board size: 114.3 mm × 76.2 mm × 1.60 mmt
Mount condition: PCB and exposed pad are soldered.
Top copper foil: ROHM recommended footprint + wiring to measure, 2 oz. copper.
2 inner layers copper foil area of PCB: 74.2 mm × 74.2 mm, 1 oz. copper.
Copper foil area on the reverse side of PCB: 74.2 mm × 74.2 mm, 2 oz. copper.

Condition①: θ_{JA} = 81 °C/W, Ψ_{JT} (top center) = 8 °C/W
Condition②: θ_{JA} = 21 °C/W, Ψ_{JT} (top center) = 2 °C/W

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Power Dissipations – continued

■HTSOP-J8

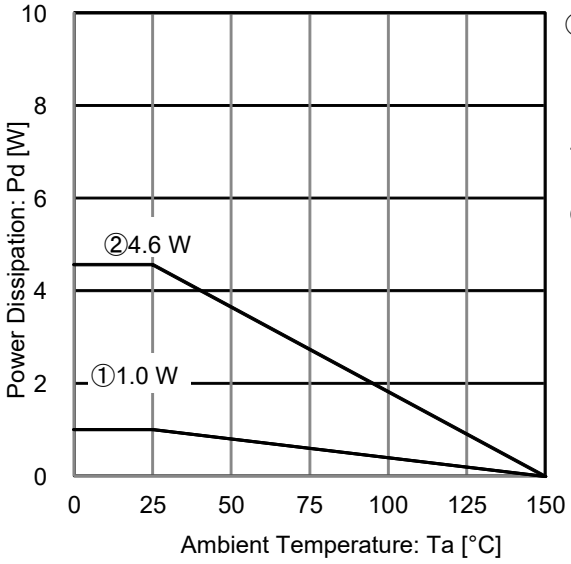


Figure 55. Package Data
(HTSOP-J8)

IC mounted on ROHM standard board based on JEDEC.
①1-layer PCB (Copper foil area on the reverse side of PCB: 0 mm × 0 mm)
Board material: FR4
Board size: 114.3 mm × 76.2 mm × 1.57 mmt
Mount condition: PCB and exposed pad are soldered.
Top copper foil: ROHM recommended footprint + wiring to measure, 2 oz. copper.

②4-layer PCB (Copper foil area on the reverse side of PCB: 74.2 mm × 74.2 mm)
Board material: FR4
Board size: 114.3 mm × 76.2 mm × 1.60 mmt
Mount condition: PCB and exposed pad are soldered.
Top copper foil: ROHM recommended footprint + wiring to measure, 2 oz. copper.
2 inner layers copper foil area of PCB: 74.2 mm × 74.2 mm, 1 oz. copper.
Copper foil area on the reverse side of PCB: 74.2 mm × 74.2 mm, 2 oz. copper.

Condition①: θ_{JA} = 126 °C/W, Ψ_{JT} (top center) = 9 °C/W
Condition②: θ_{JA} = 27 °C/W, Ψ_{JT} (top center) = 2 °C/W

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Thermal Design

This product exposes a frame on the back side of the package for thermal efficiency improvement.
Within this IC, the power consumption is decided by the dropout voltage condition, the load current and the circuit current. Refer to power dissipation curves illustrated in Figure 53, 54, 55 when using the IC in an environment of Ta ≥ 25 °C. Even if the ambient temperature Ta is at 25 °C, depending on the input voltage and the load current, chip junction temperature can be very high. Consider the design to be Tj ≤ Tjmax = 150 °C in all possible operating temperature range.
Should by any condition the maximum junction temperature Tjmax = 150 °C rating be exceeded by the temperature increase of the chip, it may result in deterioration of the properties of the chip. The thermal impedance in this specification is based on recommended PCB and measurement condition by JEDEC standard. Verify the application and allow sufficient margins in the thermal design by the following method is used to calculate the junction temperature Tj.
Tj can be calculated by either of the two following methods.

1. The following method is used to calculate the junction temperature Tj.

$$Tj = Ta + P_C \times \theta_{JA} \text{ [°C]}$$

Tj : Junction Temperature
Ta : Ambient Temperature
P_C : Power Consumption
θ_{JA} : Thermal Impedance (Junction to Ambient)

2. The following method is also used to calculate the junction temperature Tj.

$$Tj = T_T + P_C \times \Psi_{JT} \text{ [°C]}$$

Tj : Junction Temperature
T_T : Top Center of Case's (mold) Temperature
P_C : Power consumption
Ψ_{JT} : Thermal Impedance (Junction to Top Center of Case)

The following method is used to calculate the power consumption Pc (W).

$$Pc = (VCC - VOUT) \times IOUT + VCC \times I_{CC} \text{ [W]}$$

P_C : Power Consumption
VCC : Input Voltage
VOUT : Output Voltage
IOUT : Load Current
Icc : Circuit Current

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Calculation Example (TO252-3 / TO252-5)

If VCC = 13.5 V, VOUT = 5.0 V, IOUT = 200 mA, Icc = 38 μA, the power consumption Pc can be calculated as follows:

$$\begin{aligned} Pc &= (VCC - VOUT) \times IOUT + VCC \times I_{CC} \\ &= (13.5\,V - 5.0\,V) \times 200\,mA + 13.5\,V \times 38\,\mu A \\ &= 1.7\,W \end{aligned}$$

At the ambient temperature Ta = 85 °C, the thermal impedance (Junction to Ambient) θ_{JA} = 23 °C/W(4-layer PCB),

$$\begin{aligned} Tj &= Ta + P_C \times \theta_{JA} \\ &= 85\,°C + 1.7\,W \times 23\,°C/W \\ &= 124.1\,°C \end{aligned}$$

When operating the IC, the top center of case's (mold) temperature T_T = 100 °C, Ψ_{JT} = 17 °C/W(1-layer PCB),

$$\begin{aligned} Tj &= T_T + P_C \times \Psi_{JT} \\ &= 100\,°C + 1.7\,W \times 17\,°C/W \\ &= 128.9\,°C \end{aligned}$$

For optimum thermal performance, it is recommended to expand the copper foil area of the board, increasing the layer and thermal via between thermal land pad.

Calculation Example (TO263-3 / TO263-5)

If VCC = 13.5 V, VOUT = 5.0 V, IOUT = 200 mA, Icc = 38 μA, the power consumption Pc can be calculated as follows:

$$\begin{aligned} Pc &= (VCC - VOUT) \times IOUT + VCC \times I_{CC} \\ &= (13.5\,V - 5.0\,V) \times 200\,mA + 13.5\,V \times 38\,\mu A \\ &= 1.7\,W \end{aligned}$$

At the ambient temperature Ta = 85 °C, the thermal impedance (Junction to Ambient) θ_{JA} = 21 °C/W(4-layer PCB),

$$\begin{aligned} Tj &= Ta + P_C \times \theta_{JA} \\ &= 85\,°C + 1.7\,W \times 21\,°C/W \\ &= 120.7\,°C \end{aligned}$$

When operating the IC, the top center of case's (mold) temperature T_T = 100 °C, Ψ_{JT} = 8 °C/W(1-layer PCB),

$$\begin{aligned} Tj &= T_T + P_C \times \Psi_{JT} \\ &= 100\,°C + 1.7\,W \times 8\,°C/W \\ &= 113.6\,°C \end{aligned}$$

For optimum thermal performance, it is recommended to expand the copper foil area of the board, increasing the layer and thermal via between thermal land pad.

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Calculation Example (HTSOP-J8)

If VCC = 13.5 V, VOUT = 5.0 V, IOUT = 200 mA, Icc = 38 μA, the power consumption Pc can be calculated as follows:

$$\begin{aligned} Pc &= (VCC - VOUT) \times IOUT + VCC \times I_{CC} \\ &= (13.5\,V - 5.0\,V) \times 200\,mA + 13.5\,V \times 38\,\mu A \\ &= 1.7\,W \end{aligned}$$

At the ambient temperature Ta = 85 °C, the thermal impedance (Junction to Ambient) θ_{JA} = 27 °C/W(4-layer PCB),

$$\begin{aligned} Tj &= Ta + P_C \times \theta_{JA} \\ &= 85\,°C + 1.7\,W \times 27\,°C/W \\ &= 130.9\,°C \end{aligned}$$

When operating the IC, the top center of case's (mold) temperature T_T = 100 °C, Ψ_{JT} = 9 °C/W(1-layer PCB),

$$\begin{aligned} Tj &= T_T + P_C \times \Psi_{JT} \\ &= 100\,°C + 1.7\,W \times 9\,°C/W \\ &= 115.3\,°C \end{aligned}$$

For optimum thermal performance, it is recommended to expand the copper foil area of the board, increasing the layer and thermal via between thermal land pad.

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I/O Equivalence Circuit

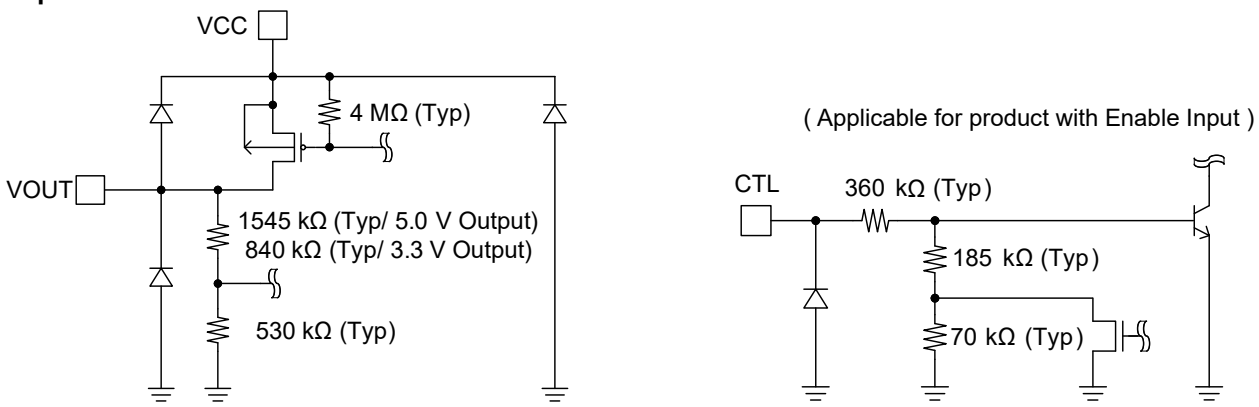


Figure 56. Input / Output Equivalence Circuit

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Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

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Operational Notes – continued

9. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

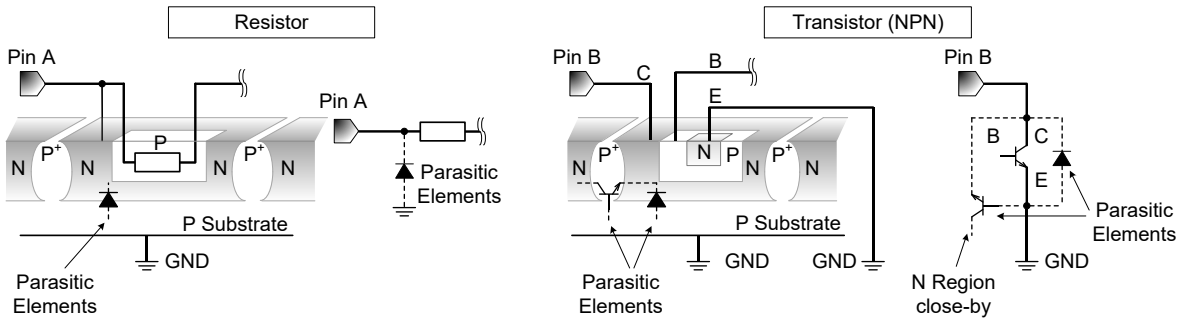


Figure 57. Example of Monolithic IC Structure

10. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

11. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

12. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

13. Thermal Consideration

The power dissipation under actual operating conditions should be taken into consideration and a sufficient margin should be allowed in the thermal design. On the reverse side of the package this product has an exposed heat pad for improving the heat dissipation. The amount of heat generation depends on the voltage difference between the input and output, load current, and bias current. Therefore, when actually using the chip, ensure that the generated heat does not exceed the Pd rating. If Junction temperature is over Tjmax (= 150 °C), IC characteristics may be worse due to rising chip temperature. Heat resistance in specification is measurement under PCB condition and environment recommended in JEDEC. Ensure that heat resistance in specification is different from actual environment.

14. CTL Pin

The CTL pin is for controlling ON/OFF the output voltage. Do not make voltage level of chip enable keep floating level, or between VthH and VthL. Otherwise, the output voltage would be unstable or indefinite.

15. Functional Safety

"ISO 26262 process compliant to support ASIL-*"
A product that has been developed based on an ISO 26262 design process compliant to the ASIL level described in the datasheet.

"Safety mechanism is implemented to support functional safety (ASIL-*)"
A product that has implemented safety mechanism to meet ASIL level requirements described in the datasheet.

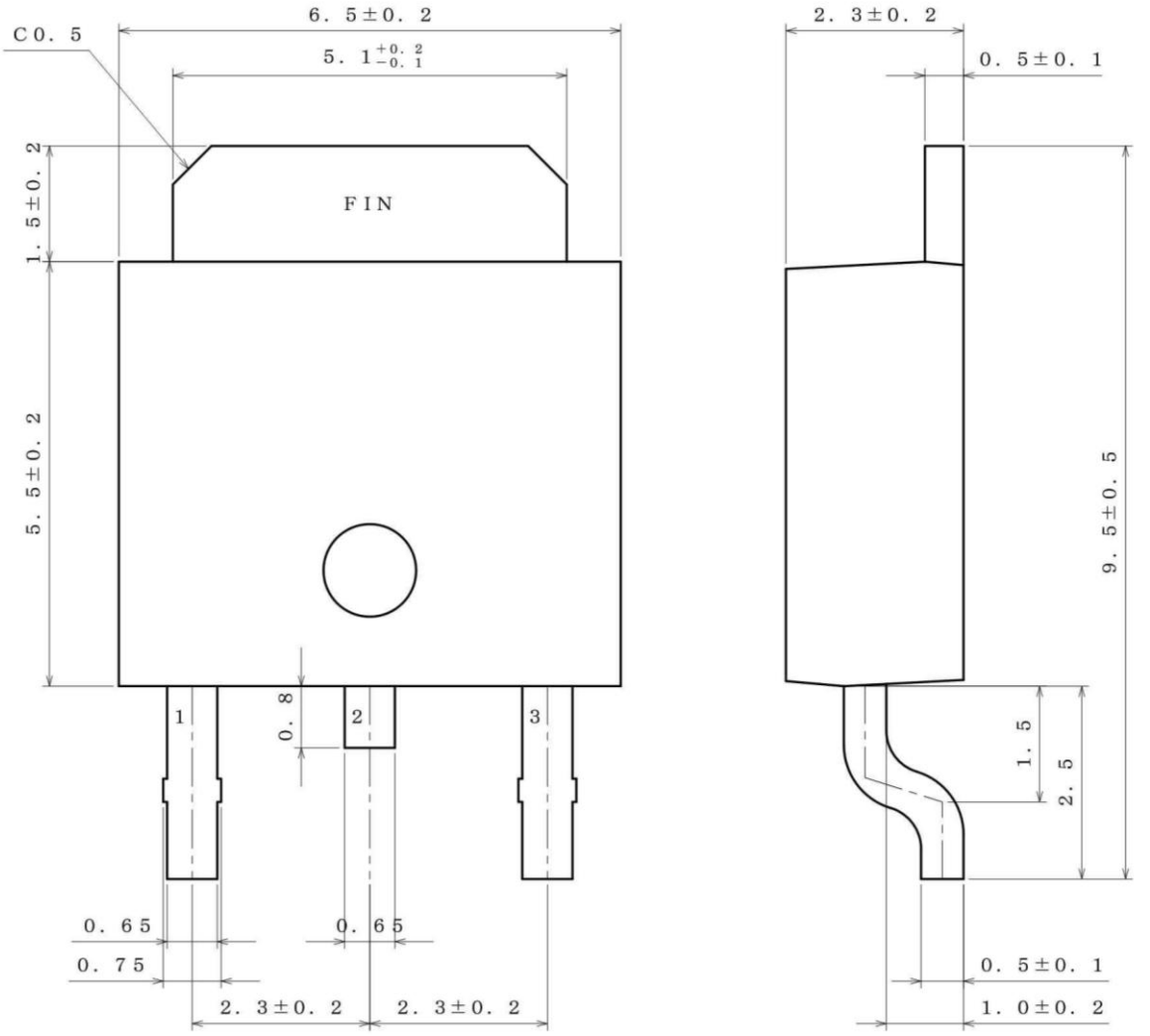
"Functional safety supportive automotive products"
A product that has been developed for automotive use and is capable of supporting safety analysis with regard to the functional safety.

Note: "ASIL-*" is stands for the ratings of "ASIL-A", "-B", "-C" or "-D" specified by each product's datasheet.

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Physical Dimension and Packing Information

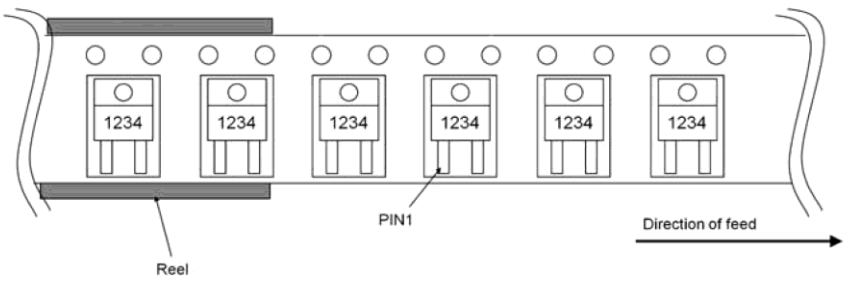
Package Name	TO252-3



(UNITS ; mm)
PKG : TO252−3
Drawing No. EX535−5001−1

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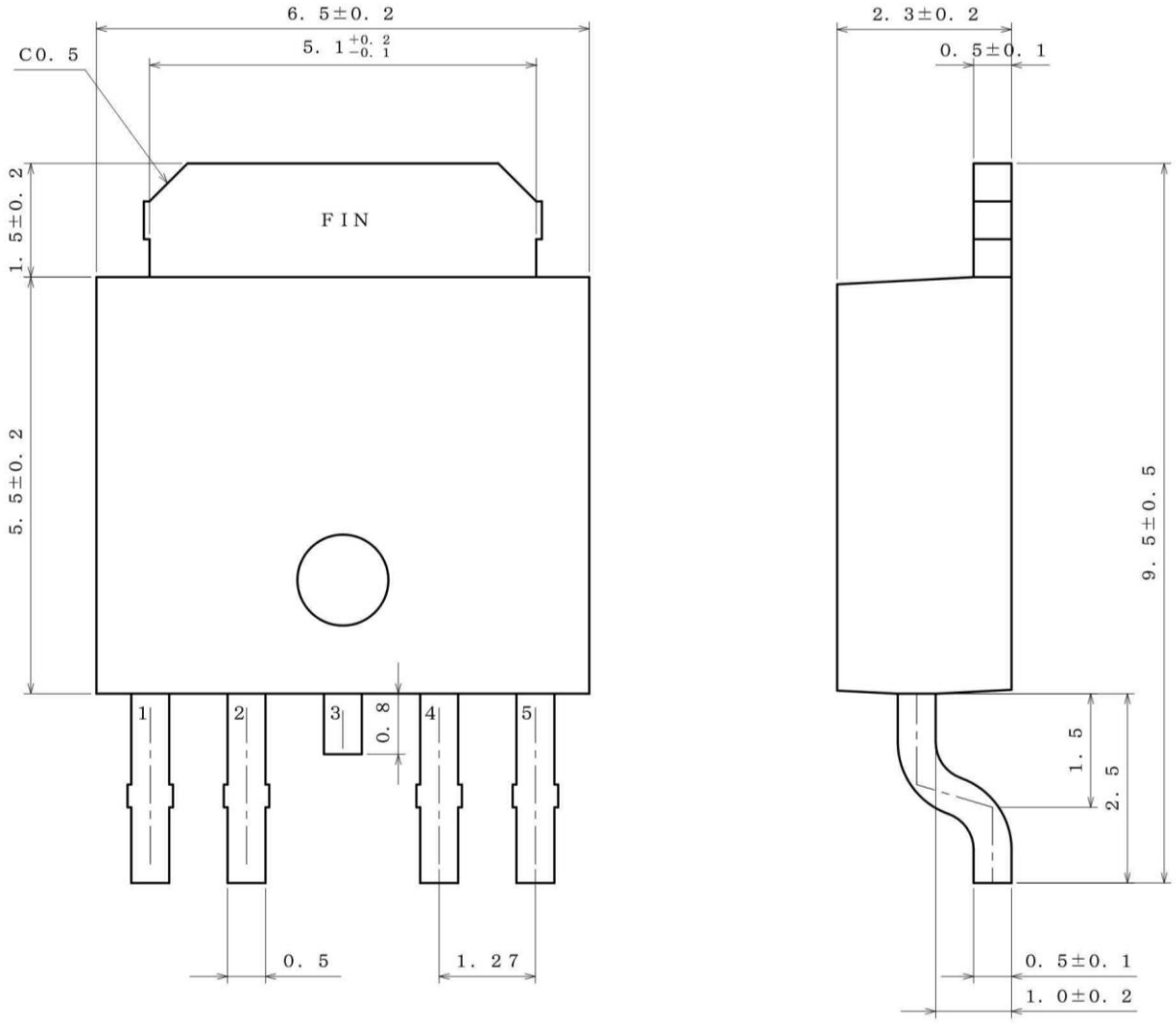
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Quantity	2000pcs
Direction of feed	E2



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Physical Dimension and Packing Information – continued

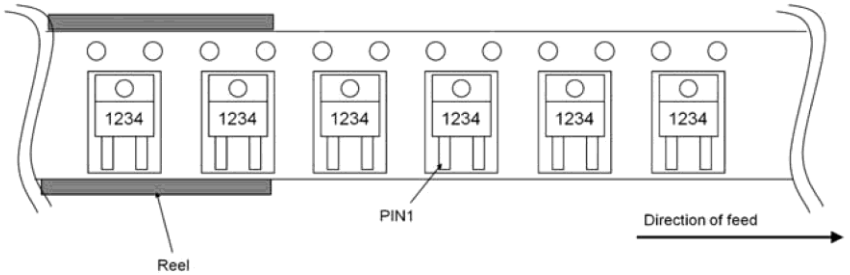
Package Name	TO252-5



(UNIT : mm)
PKG : TO252−5
Drawing No. EX536−5001−1

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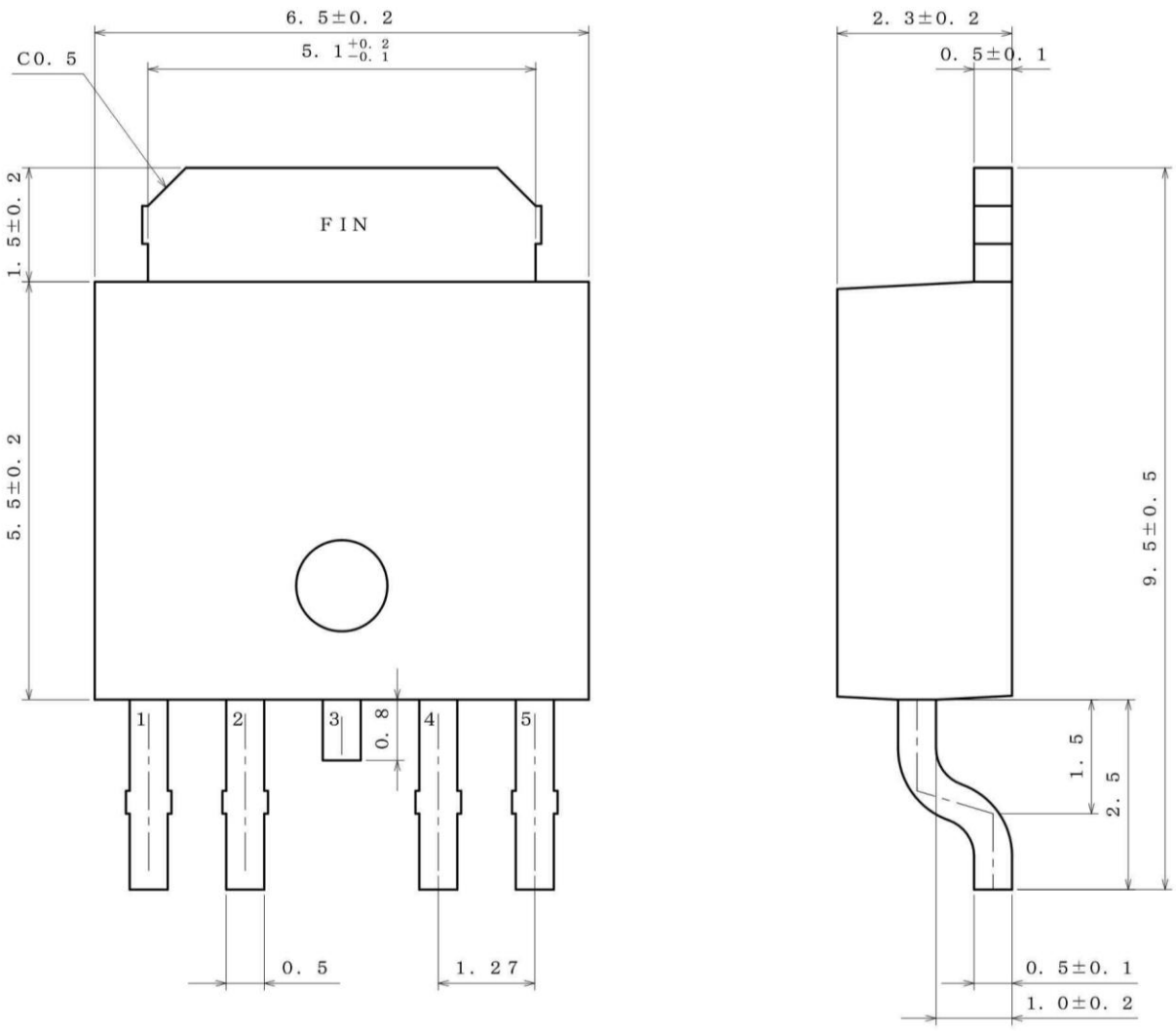
Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2



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Physical Dimension and Packing Information – continued

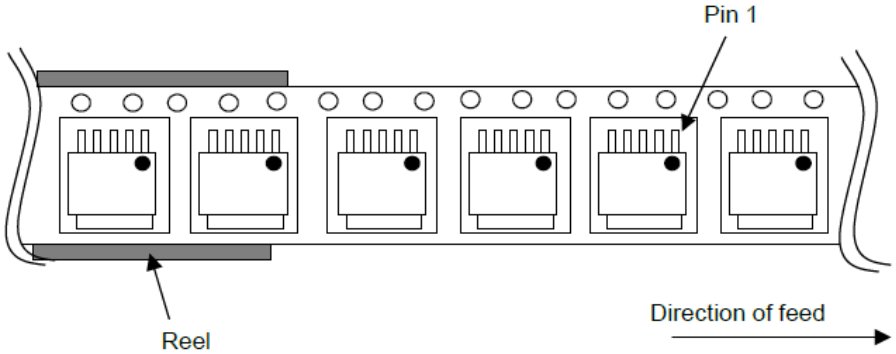
Package Name	TO252-5



(UNIT : mm)
PKG : TO252−5
Drawing No. EX536−5001−1

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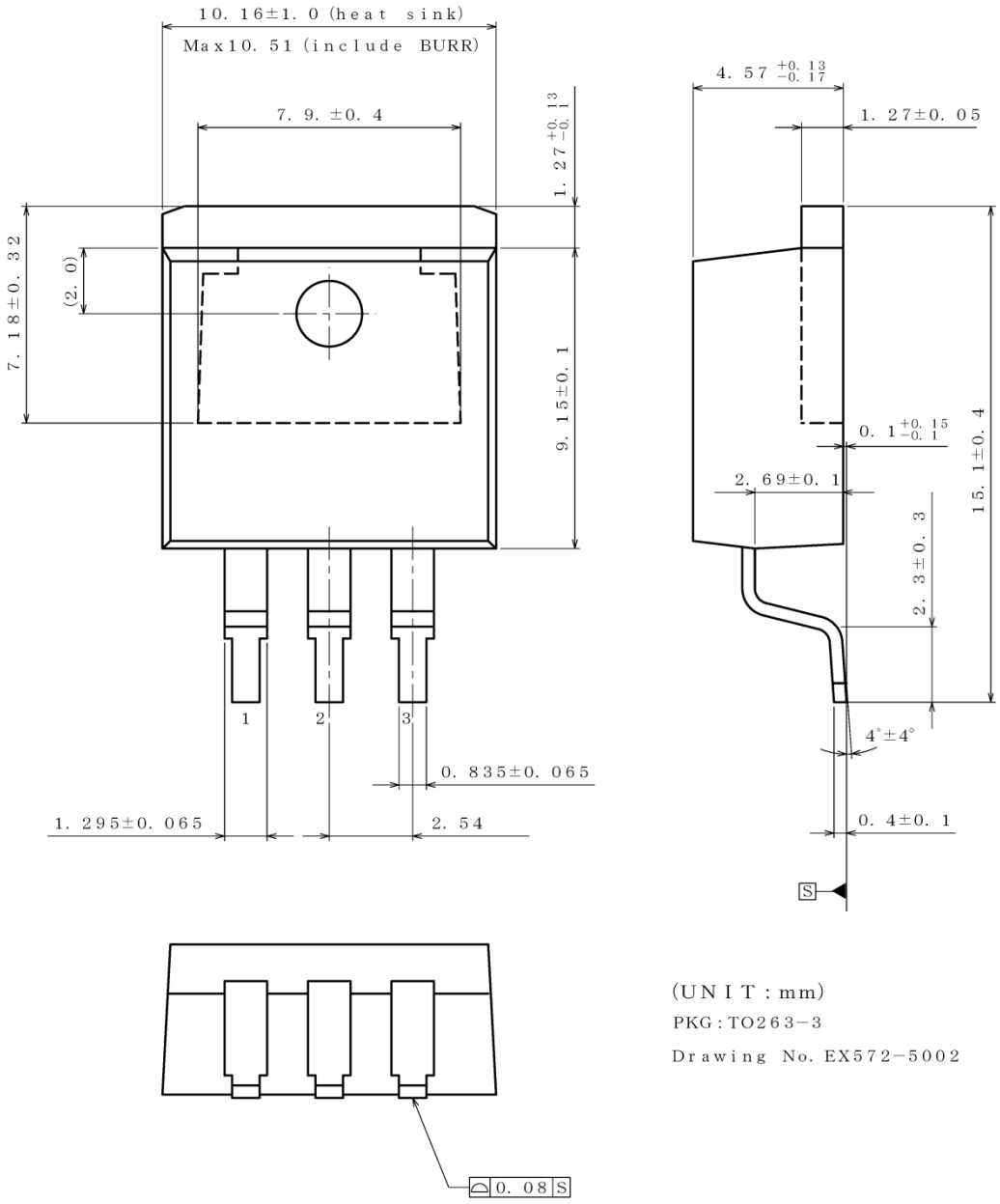
Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E1



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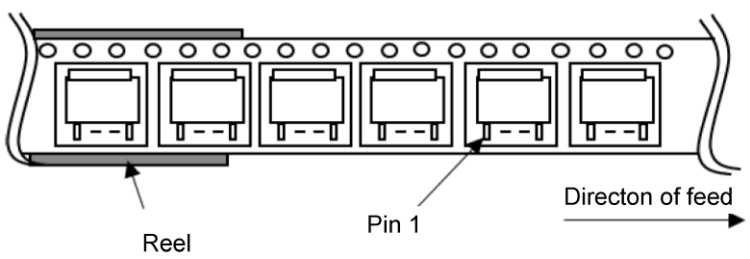
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Package Name	TO263-3



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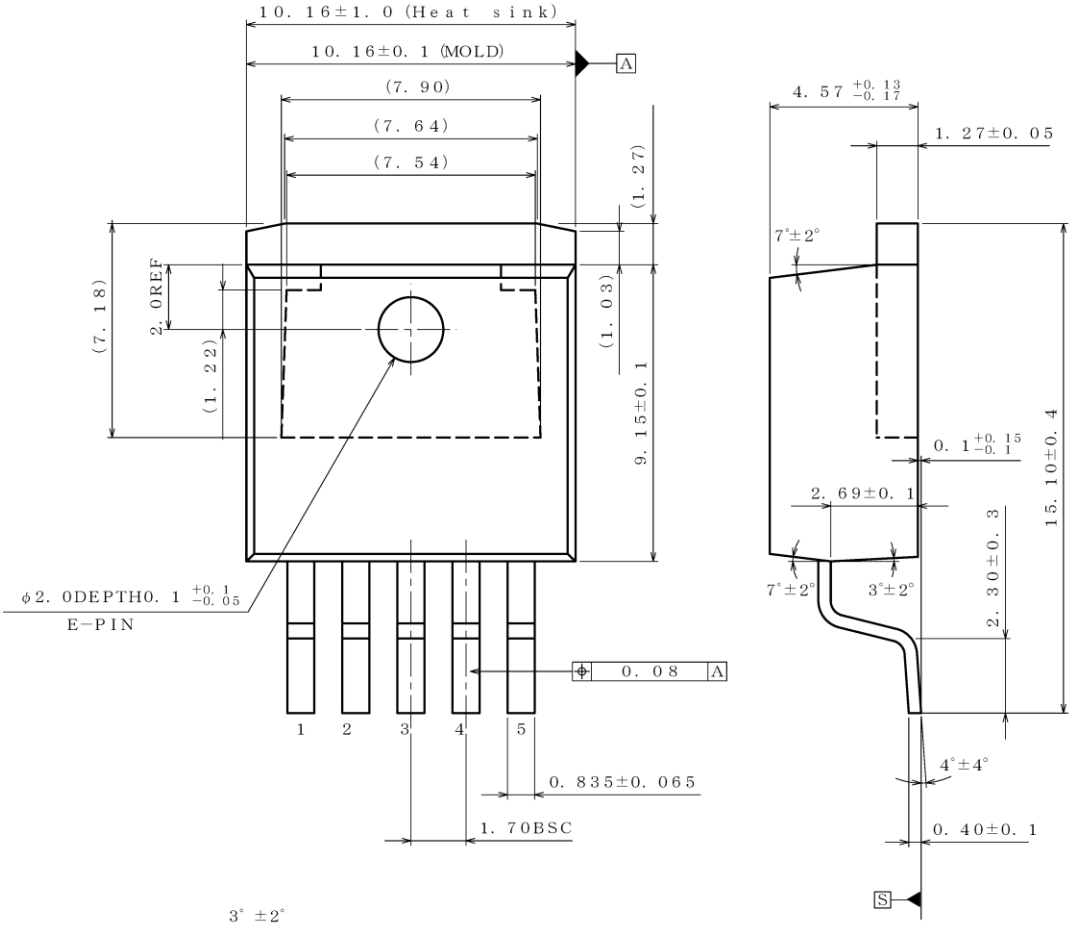
Tape	Embossed carrier tape
Quantity	500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the lower left when you hold reel on the left hand and you pull out the tape on the right hand



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Physical Dimension and Packing Information – continued

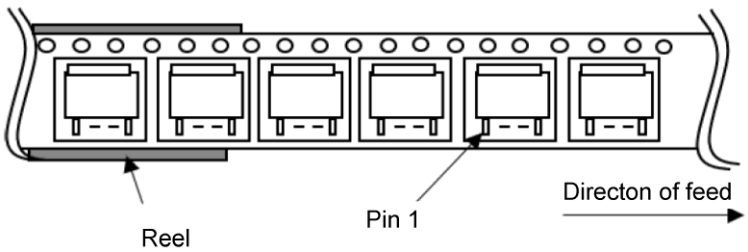
Package Name	TO263-5



(UNIT : mm)
PKG : TO263-5
Drawing No. EX573-5002

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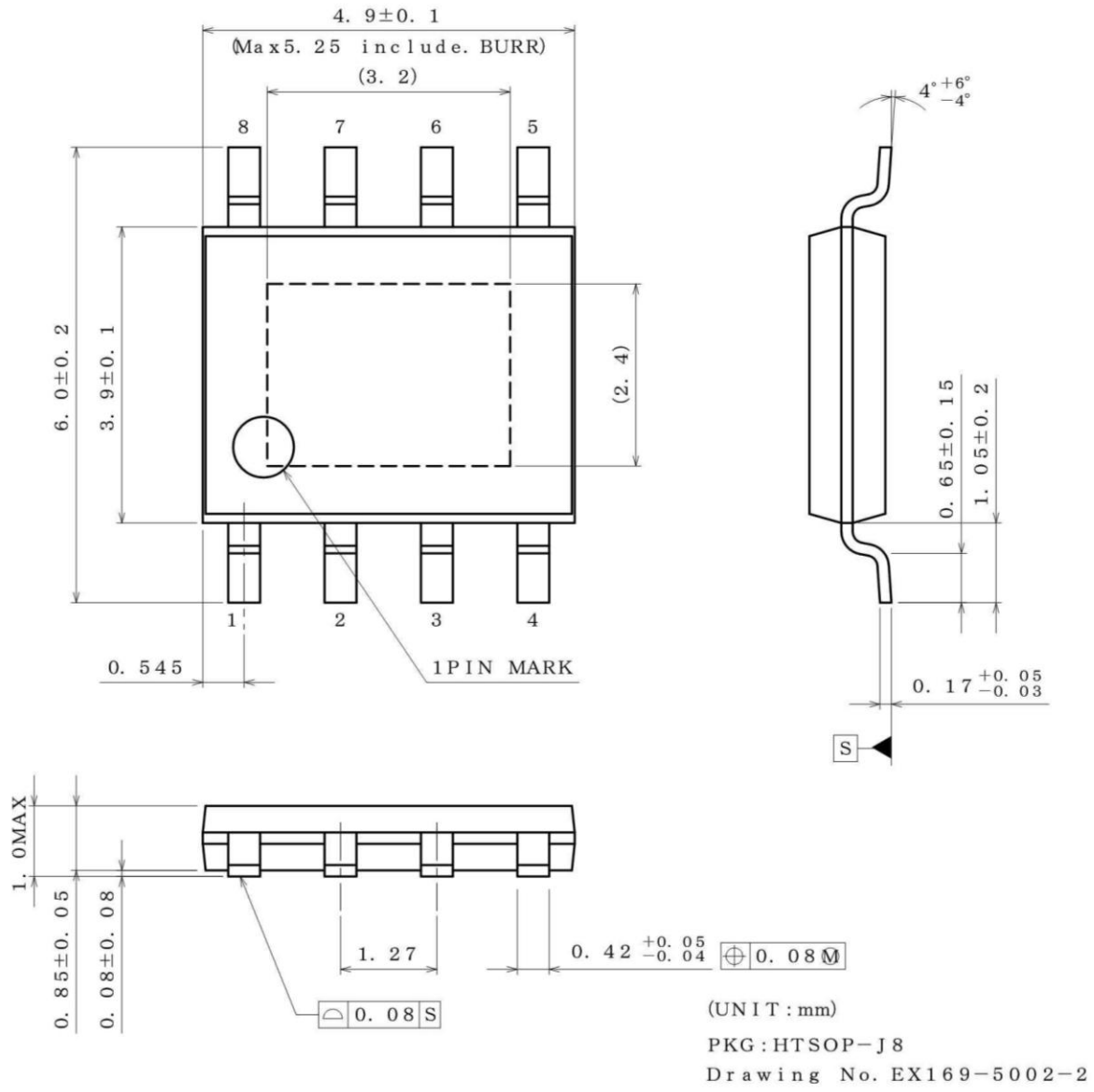
Tape	Embossed carrier tape
Quantity	500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the lower left when you hold reel on the left hand and you pull out the tape on the right hand



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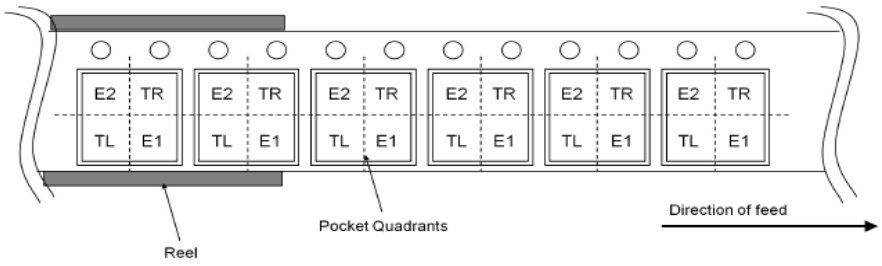
Physical Dimension and Packing Information – continued

Package Name	HTSOP-J8



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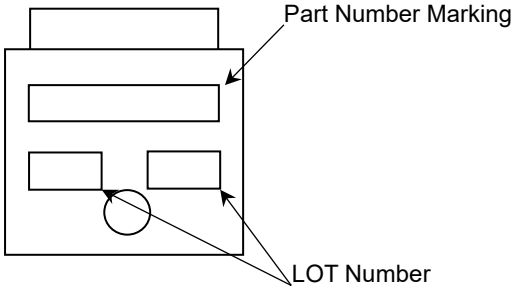
Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



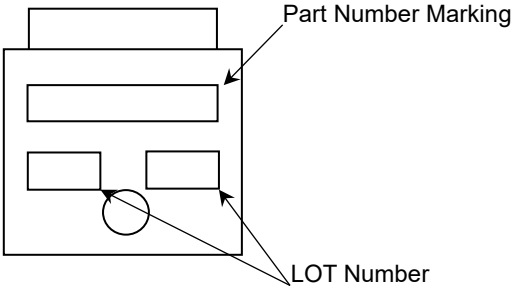
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Marking Diagrams (Top View)

TO252-3 (Top View)



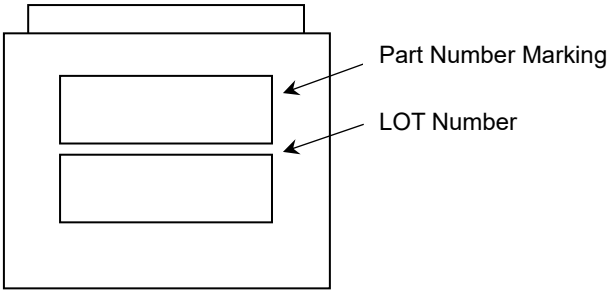
TO252-5 (Top View)



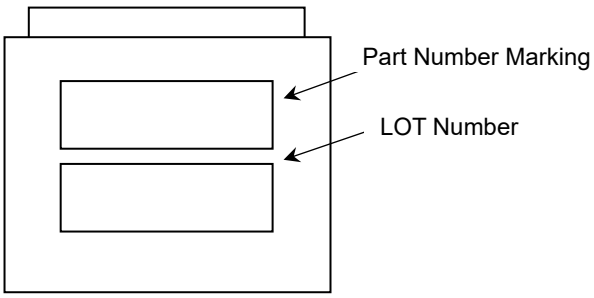
Part Number Marking	Output Voltage [V]	Enable Input(Note 1)	Orderable Part Number
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450S5	5.0	not available	BD450S5FP-CE2
433S5W	3.3	available	BD433S5WFP-CE2
450S5W	5.0	available	BD450S5WFP-CE2 BD450S5WFP-CE1

(Note 1) available: Includes Enable Input
not available: Not includes Enable Input

TO263-3 (Top View)



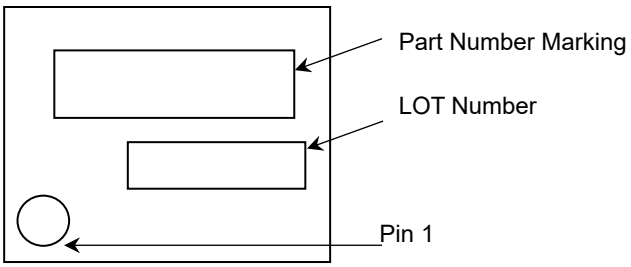
TO263-5 (Top View)



Part Number Marking	Output Voltage [V]	Enable Input(Note 1)	Orderable Part Number
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450S5	5.0	not available	BD450S5FP2-CE2
433S5W	3.3	available	BD433S5WFP2-CE2
450S5W	5.0	available	BD450S5WFP2-CE2

(Note 1) available: Includes Enable Input
not available: Not includes Enable Input

HTSOP-J8 (Top View)



Part Number Marking	Output Voltage [V]	Enable Input(Note 1)	Orderable Part Number
433S5	3.3	not available	BD433S5EFJ-CE2
450S5	5.0	not available	BD450S5EFJ-CE2
433S5W	3.3	available	BD433S5WEFJ-CE2
450S5W	5.0	available	BD450S5WEFJ-CE2

(Note 1) available: Includes Enable Input
not available: Not includes Enable Input

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Revision History

Date	Revision	Changes
24.Jun.2022	001	New Release
26.Oct.2022	002	Add lineup
30.May.2023	003	Add lineup
22.May.2025	004	P.27 Improved the title of Figure 41.
07.Jan.2026	005	Add packing information (BD450S5WFP-CE1)

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Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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