Single-Output LDO Regulators

# Ultra Low Quiescent Current LDO Regulator

**BD7xxL2EFJ-C BD7xxU2EFJ-C BD7xxL2FP-C BD7xxL2FP3-C**

## ●General Description

The BD7xxL2EFJ-C, BD7xxU2EFJ-C, BD7xxL2FP-C, BD7xxL2FP3-C are low quiescent regulators featuring 50V absolute maximum voltage, and output voltage accuracy of ±2%, 200mA output current and 6μA (Typ) current consumption. These regulators are therefore ideal for applications requiring a direct connection to the battery and a low current consumption. Ceramic capacitors can be used for compensation of the output capacitor phase. Furthermore, these ICs also feature overcurrent protection to protect the device from damage caused by short-circuiting and an integrated thermal shutdown to protect the device from overheating at overload conditions.

## ●Features

- Ultra low quiescent current: 6μA (Typ)
- Output current capability: 200mA
- Output voltage: 3.3 V or 5.0 V (Typ)
- High output voltage accuracy: ±2%
- Low saturation voltage by using PMOS output transistor.
- Integrated overcurrent protection to protect the IC from damage caused by output short-circuiting.
- Integrated thermal shutdown to protect the IC from overheating at overload conditions.
- Low ESR ceramic capacitor can be used as output capacitor.
- HTSOP-J8, TO252-3, SOT223-4(F) (*1) 3type package
  (*1 : SOT223-4, SOT223-4F)

## ●Key specification

- Ultra low quiescent current: 6μA (Typ)
- Output voltage: 3.3 V or 5.0 V (Typ)
- Output current capability: 200mA
- High output voltage accuracy: ±2%
- Low ESR ceramic capacitor can be used as output capacitor
- AEC-Q100 Qualified(*2)
  (*2:Grade1)

## ●Packages

W (Typ) x D (Typ) x H (Max)

- EFJ: HTSOP-J8 — 4.90mm x 6.00mm x 1.00mm



- FP: TO252-3 — 6.50mm x 9.50mm x 2.50mm



- FP3 : SOT223-4(F) — 6.53mm x 7.00mm x 1.80mm



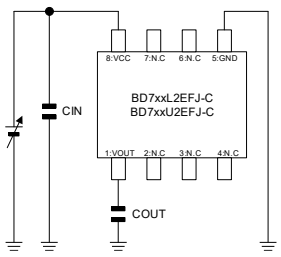
Figure 1. Package Outlook

## ●Applications

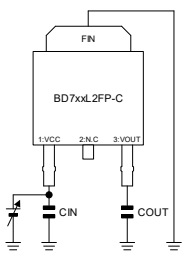
- Automotive (body, audio system, navigation system, etc.)

## ●Typical Application Circuits

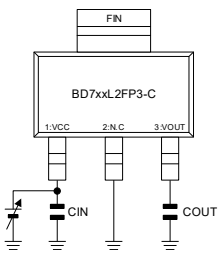
- Components externally connected: 0.1 μF ≤ CIN, 4.7 μF ≤ COUT (Min)
  *Electrolytic, tantalum and ceramic capacitors can be used.




HTSOP-J8




TO252-3



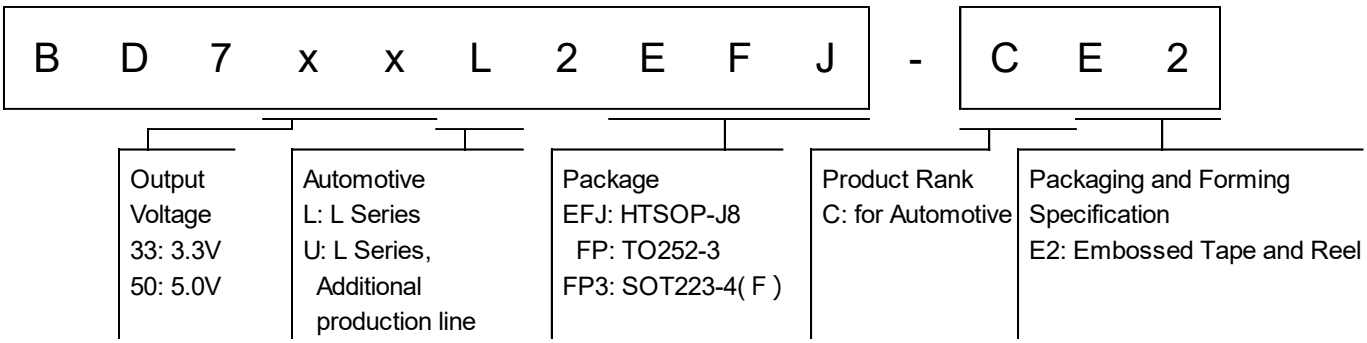

SOT223-4(F)

Figure 2. Typical Application Circuits

○Product structure : Silicon monolithic integrated circuit ○This product is not designed protection against radioactive rays


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●**Ordering Information**




●**Lineup**

| Output current ability | Output voltage (Typ) | Package type | Orderable Part Number | Remarks |
|---|---|---|---|---|
| 200 mA | 3.3 V | HTSOP-J8 | BD733L2EFJ-CE2 | Production LineA *(Note 1)* |
| | | HTSOP-J8 | BD733U2EFJ-CE2 | Production LineB *(Note 1)* |
| | | TO252-3 | BD733L2FP-CE2 | |
| | | SOT223-4(F) | BD733L2FP3-CE2 | |
| | 5.0 V | HTSOP-J8 | BD750L2EFJ-CE2 | Production LineA *(Note 1)* |
| | | HTSOP-J8 | BD750U2EFJ-CE2 | Production LineB *(Note 1)* |
| | | TO252-3 | BD750L2FP-CE2 | |
| | | SOT223-4(F) | BD750L2FP3-CE2 | |

*(Note 1)* For the purpose of improving production efficiency, Production Line A and B have a multi-line configuration.
Electric characteristics noted in Datasheet does not differ between Production Line A and B. Production Line B is recommended for new product.


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## ●Pin Configuration

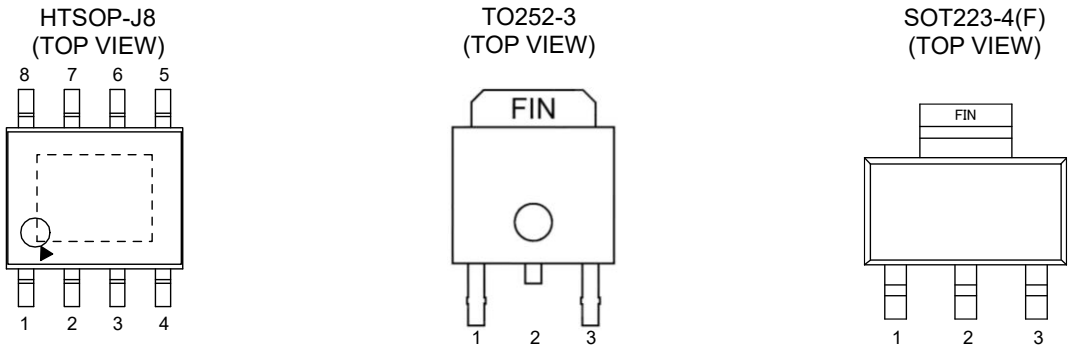



Figure 3. Pin Configuration

## ●Pin Description

■HTSOP-J8

| Pin No. | Pin Name | Function |
|---|---|---|
| 1 | VOUT | Output pin |
| 2 | N.C. | Not connected |
| 3 | N.C. | Not connected |
| 4 | N.C. | Not connected |
| 5 | GND | GND |
| 6 | N.C. | Not connected |
| 7 | N.C. | Not connected |
| 8 | VCC | Supply voltage input pin |

(※N.C. terminals are not need to connect to GND.
(※Exposed die pad is need to be connected to GND in the inside of IC.)
(※Exposed die pad is connected to GND in the inside of IC.)

■TO252-3, SOT223-4(F)

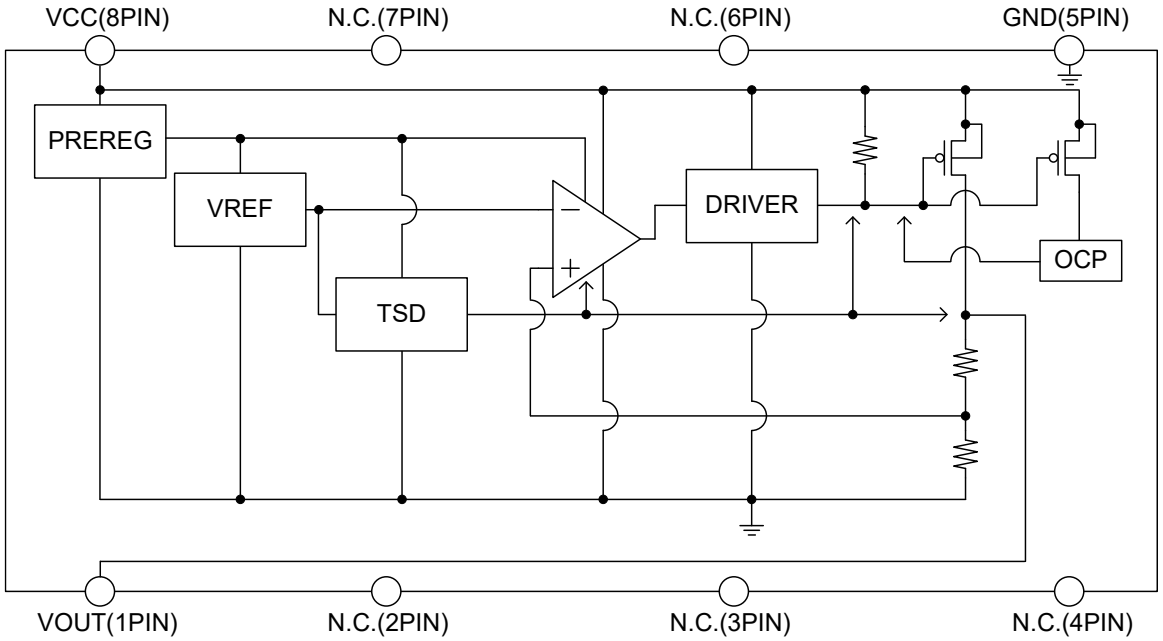
| Pin No. | Pin Name | Function |
|---|---|---|
| 1 | VCC | Supply voltage input pin |
| 2 | N.C./GND | TO252-3: N.C.<br>SOT223-4(F): GND |
| 3 | VOUT | Output pin |
| FIN | GND | GND |

(※N.C. terminals are not need to connect to GND.)


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## ●Block Diagram

■HTSOP-J8




■TO252-3, SOT223-4(F)

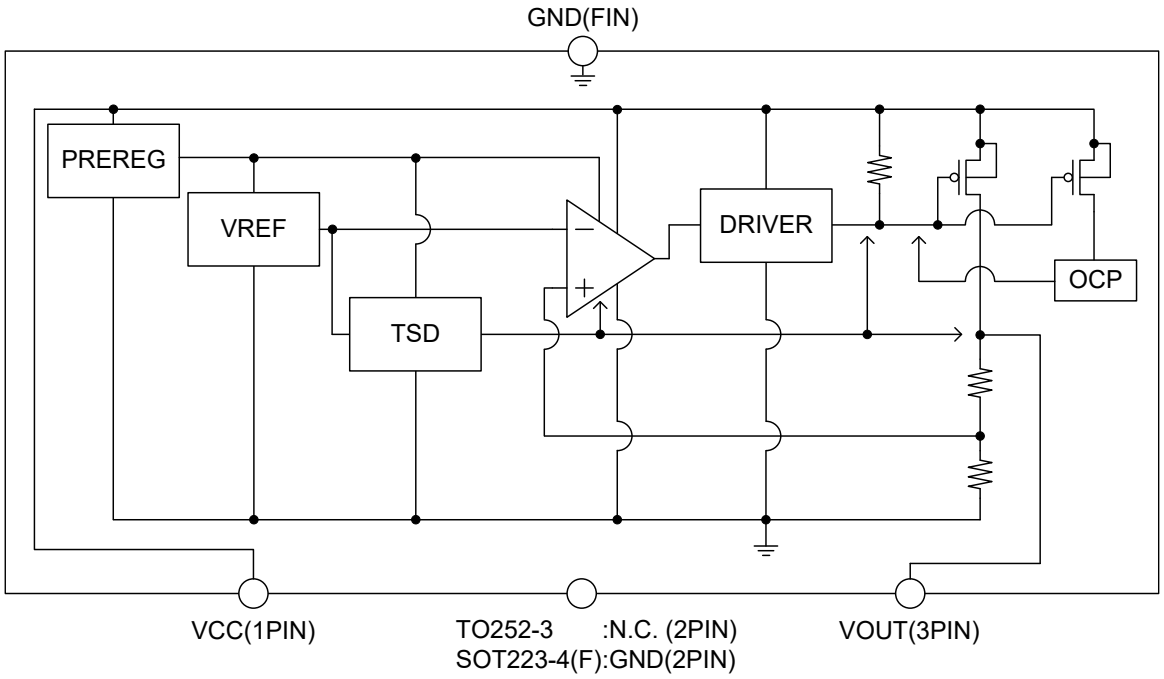



Figure 4. Block Diagram


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●**Absolute Maximum Ratings（Ta=25°C）**

| Parameter | Symbol | Ratings | Unit |
|---|---|---|---|
| Supply Voltage *1 | VCC | -0.3 to +50.0 | V |
| Operating Temperature Range | Topr | -40 to +125 | °C |
| Storage Temperature Range | Tstg | -55 to +150 | °C |
| Maximum Junction Temperature | Tjmax | 150 | °C |

*1 Pd should not be exceeded.

●**Operating Conditions（-40 < Ta < +125°C）**

■BD733L2EFJ-C, BD733U2EFJ-C, BD733L2FP-C, BD733L2FP3-C

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply Voltage *2 | VCC | 4.37 | 45.0 | V |
| Startup Voltage *3 | VCC | 3.0 | - | V |
| Output Current | IOUT | 0 | 200 | mA |

■BD750L2EFJ-C, BD750U2EFJ-C, BD750L2FP-C, BD750L2FP3-C

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply Voltage *2 | VCC | 5.8 | 45.0 | V |
| Startup Voltage *3 | VCC | 3.0 | - | V |
| Output Current | IOUT | 0 | 200 | mA |

*2 For output voltage, refer to the dropout voltage corresponding to the output current.
*3 When IOUT=0mA.


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●**Thermal Resistance**(*1)

| Parameter | Symbol | Thermal Resistance (Typ) | | Unit |
|---|---|---|---|---|
| | | 1s(*3) | 2s2p(*4) | |
| HTSOP-J8 | | | | |
| Junction to Ambient | $\theta_{JA}$ | 130 | 34 | °C/W |
| Junction to Top Characterization Parameter(*2) | $\Psi_{JT}$ | 15 | 7 | °C/W |
| TO252-3 | | | | |
| Junction to Ambient | $\theta_{JA}$ | 136 | 23 | °C/W |
| Junction to Top Characterization Parameter(*2) | $\Psi_{JT}$ | 17 | 3 | °C/W |
| SOT223-4(F) | | | | |
| Junction to Ambient | $\theta_{JA}$ | 164 | 71 | °C/W |
| Junction to Top Characterization Parameter(*2) | $\Psi_{JT}$ | 20 | 14 | °C/W |

(*1)Based on JESD51-2A(Still-Air).
(*2)The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(*3)Using a PCB board based on JESD51-3.

| Layer Number of Measurement Board | Material | Board Size |
|---|---|---|
| Single | FR-4 | 114.3mm x 76.2mm x 1.57mmt |

| Top | |
|---|---|
| Copper Pattern | Thickness |
| Footprints and Traces | 70µm |

(*4)Using a PCB board based on JESD51-5, 7.

| Layer Number of Measurement Board | Material | Board Size | Thermal Via(*5) | |
|---|---|---|---|---|
| | | | Pitch | Diameter |
| 4 Layers | FR-4 | 114.3mm x 76.2mm x 1.6mmt | 1.20mm | Φ0.30mm |

| Top | | 2 Internal Layers | | Bottom | |
|---|---|---|---|---|---|
| Copper Pattern | Thickness | Copper Pattern | Thickness | Copper Pattern | Thickness |
| Footprints and Traces | 70µm | 74.2mm x 74.2mm | 35µm | 74.2mm x 74.2mm | 70µm |

(*5) This thermal via connects with the copper pattern of all layers.


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**●Electrical Characteristics (BD733L2EFJ-C, BD733U2EFJ-C, BD733L2FP-C, BD733L2FP3-C)**

(Unless otherwise specified, -40 < Ta < +125°C, VCC=13.5V, IOUT=0mA, Reference value: Ta=25°C)

| Parameter | Symbol | Limit | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Bias current | Ib | - | 6 | 15 | μA | |
| Output voltage | VOUT | 3.23 | 3.30 | 3.37 | V | 8V < VCC < 16V<br>0mA < IOUT < 100mA |
| Dropout voltage | ΔVd | - | 0.6 | 1.0 | V | VCC=VOUT×0.95, IOUT=200mA |
| Ripple rejection | R.R. | 50 | 63 | - | dB | f=120Hz, ein=1Vrms,<br>IOUT=100mA |
| Line regulation | Reg I | - | 5 | 20 | mV | 8V < VCC < 16V |
| Load regulation | Reg L | - | 5 | 20 | mV | 10mA < IOUT < 200mA |

**●Electrical Characteristics (BD750L2EFJ-C, BD750U2EFJ-C, BD750L2FP-C, BD750L2FP3-C)**

(Unless otherwise specified, -40 < Ta < +125°C, VCC=13.5V, IOUT=0mA, Reference value: Ta=25°C)

| Parameter | Symbol | Limit | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Bias current | Ib | - | 6 | 15 | μA | |
| Output voltage | VOUT | 4.9 | 5.0 | 5.1 | V | 8V < VCC < 16V<br>0mA < IOUT < 100mA |
| Dropout voltage | ΔVd | - | 0.4 | 0.7 | V | VCC=VOUT×0.95, IOUT=200mA |
| Ripple rejection | R.R. | 50 | 60 | - | dB | f=120Hz, ein=1Vrms,<br>IOUT=100mA |
| Line regulation | Reg I | - | 5 | 20 | mV | 8V < VCC < 16V |
| Load regulation | Reg L | - | 5 | 20 | mV | 10mA < IOUT < 200mA |


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●**Typical Performance Curves**

■BD733L2EFJ-C, BD733U2EFJ-C, BD733L2FP-C, BD733L2FP3-C Reference data

Unless otherwise specified: -40 < Ta < +125°C, VCC=13.5V, IOUT=0mA

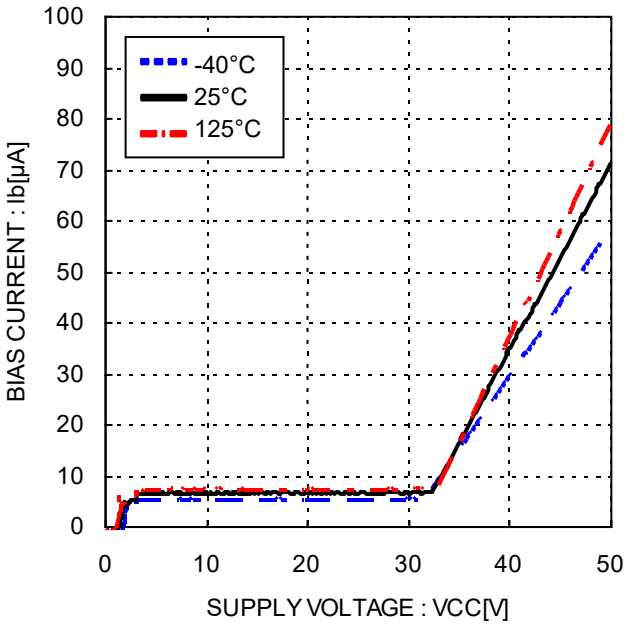



Figure 5. Bias current

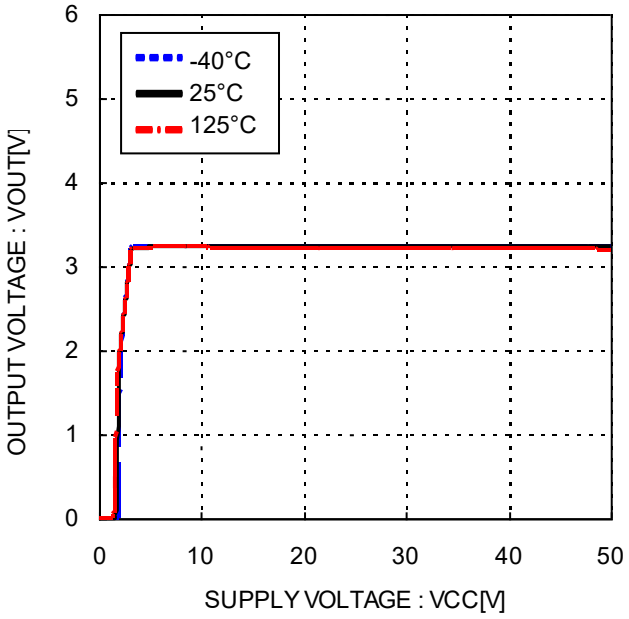



Figure 6. Output voltage vs. Supply voltage
IOUT=10mA

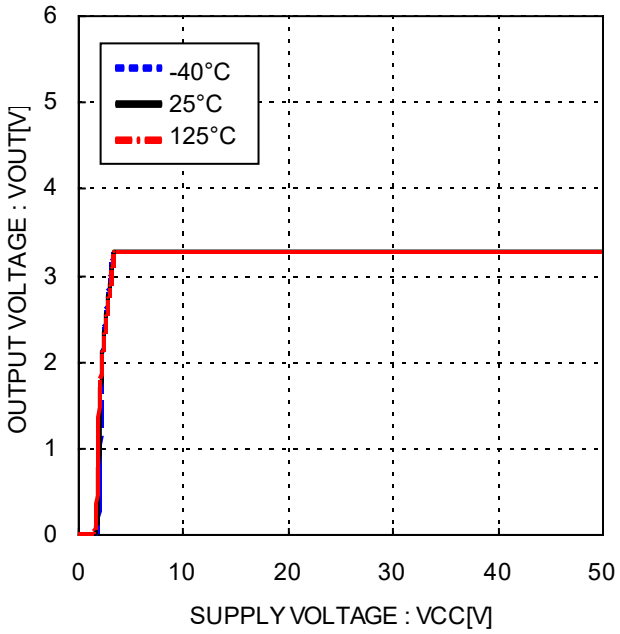



Figure 7. Output voltage vs. Supply voltage
IOUT=100mA

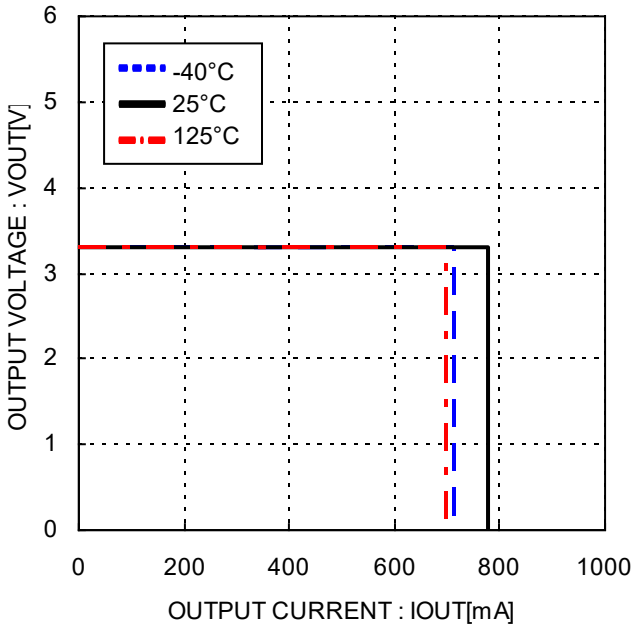



Figure 8. Output voltage vs. Load


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●**Typical Performance Curves – continued**

■BD733L2EFJ-C, BD733U2EFJ-C, BD733L2FP-C, BD733L2FP3-C Reference data

Unless otherwise specified: -40 < Ta < +125°C, VCC=13.5V, IOUT=0mA

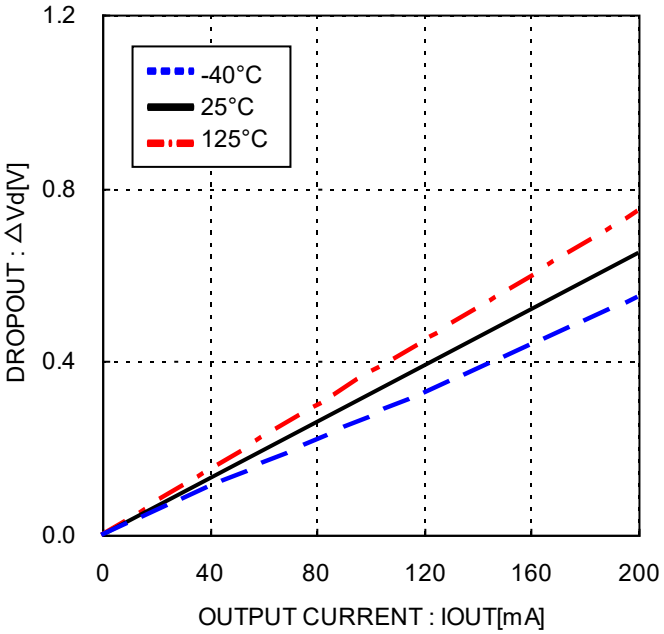



Figure 9. Dropout voltage

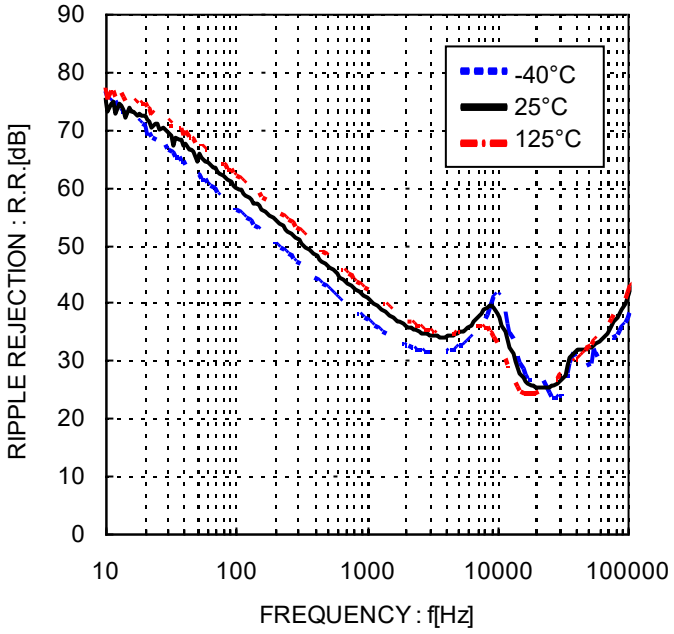



Figure 10. Ripple rejection
(ein=1Vrms,IOUT=100mA)

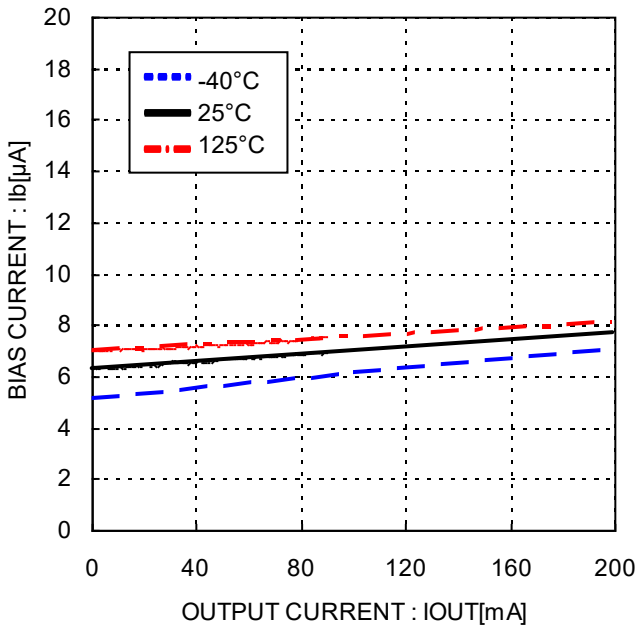



Figure 11. Total supply current vs. Load

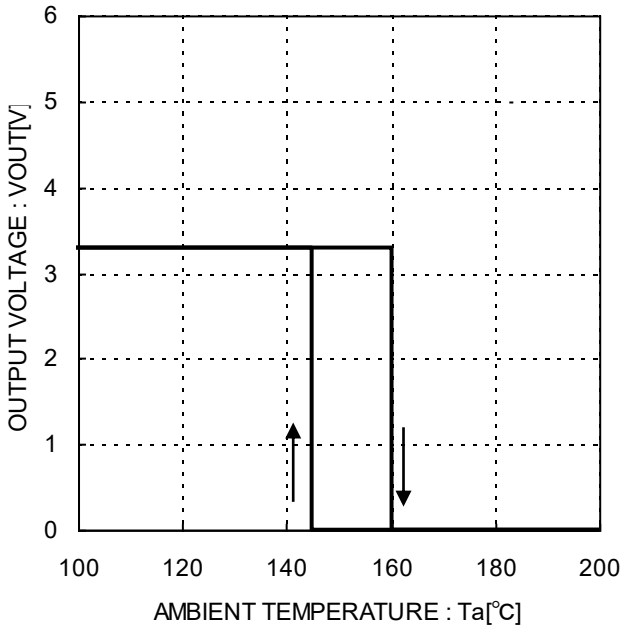



Figure 12. Thermal shutdown
(Output voltage vs. Temperature)


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●**Typical Performance Curves – continued**

■BD733L2EFJ-C, BD733U2EFJ-C, BD733L2FP-C, BD733L2FP3-C Reference data

Unless otherwise specified: -40 < Ta < +125°C, VCC=13.5V, IOUT=0mA

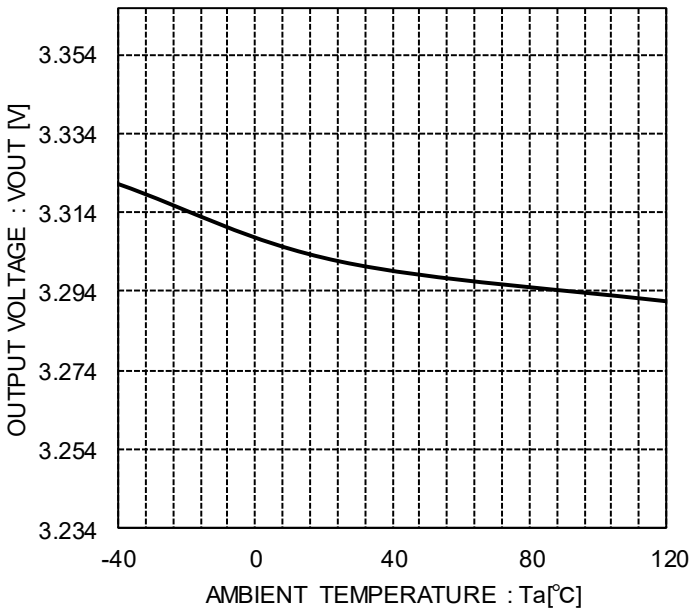



Figure 13. Output voltage vs. Temperature

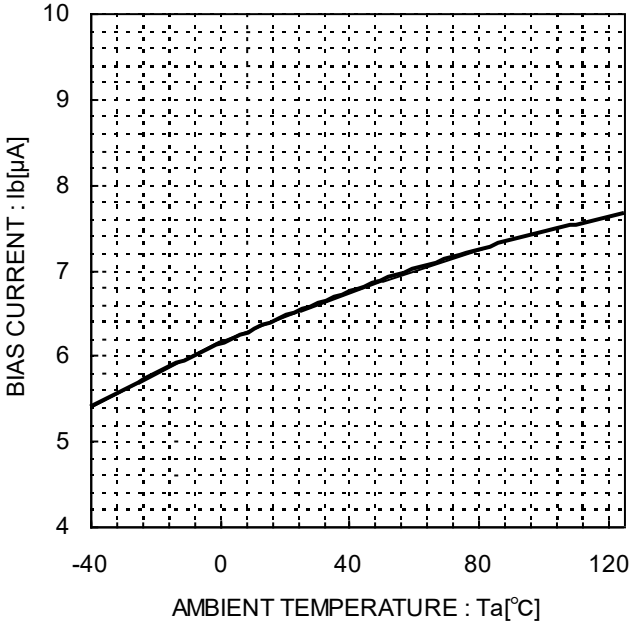



Figure 14. Bias current vs. Temperature


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●**Typical Performance Curves – continued**

■BD750L2EFJ-C, BD750U2EFJ-C, BD750L2FP-C, BD750L2FP3-C Reference data

Unless otherwise specified: -40 < Ta < +125°C, VCC=13.5V, IOUT=0mA

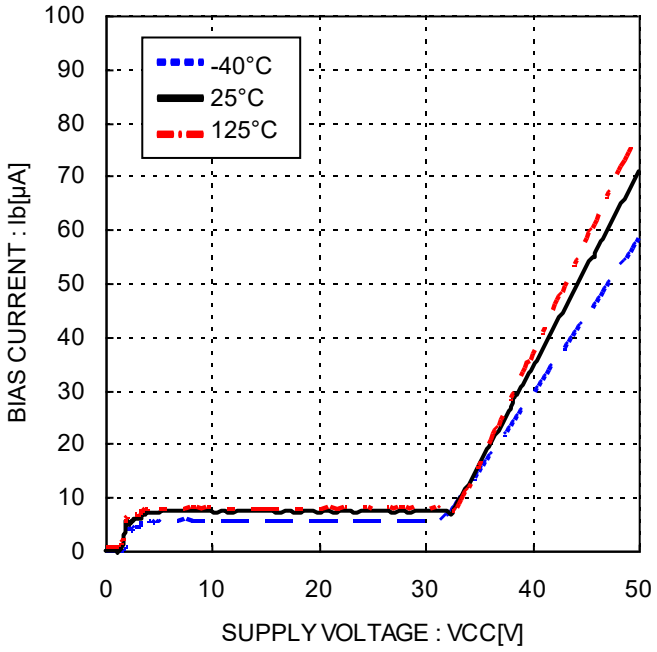



Figure 15. Bias current

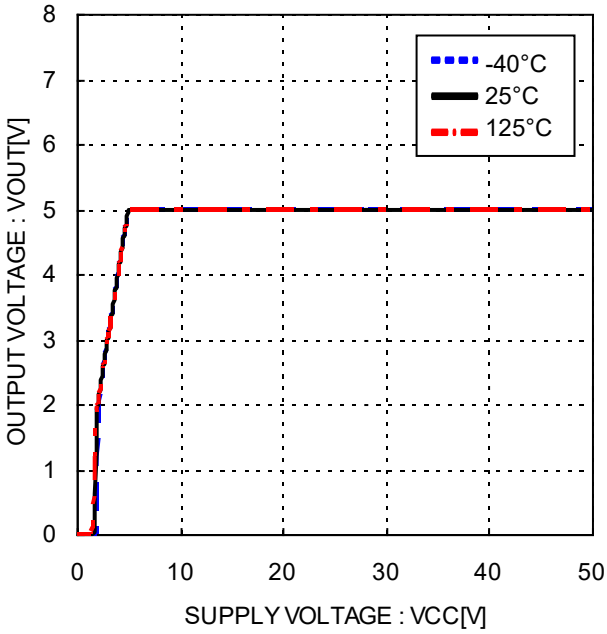



Figure 16. Output voltage vs. Supply voltage

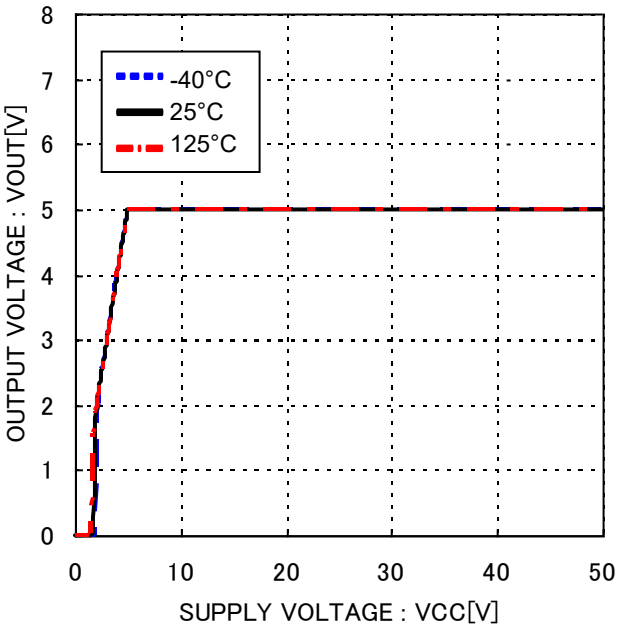



Figure 17. Output voltage vs. Supply voltage
IOUT=100mA

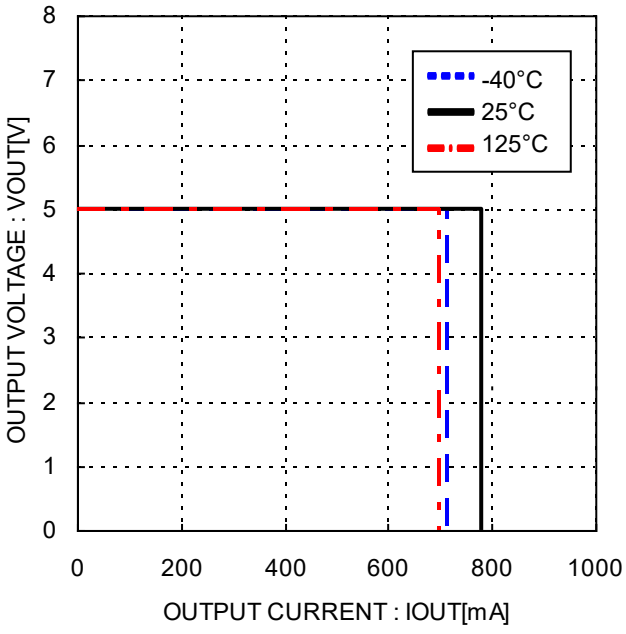



Figure 18. Output voltage vs. Load


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●**Typical Performance Curves – continued**

■BD750L2EFJ-C, BD750U2EFJ-C, BD750L2FP-C, BD750L2FP3-C Reference data

Unless otherwise specified: -40 < Ta < +125°C, VCC=13.5V, IOUT=0mA

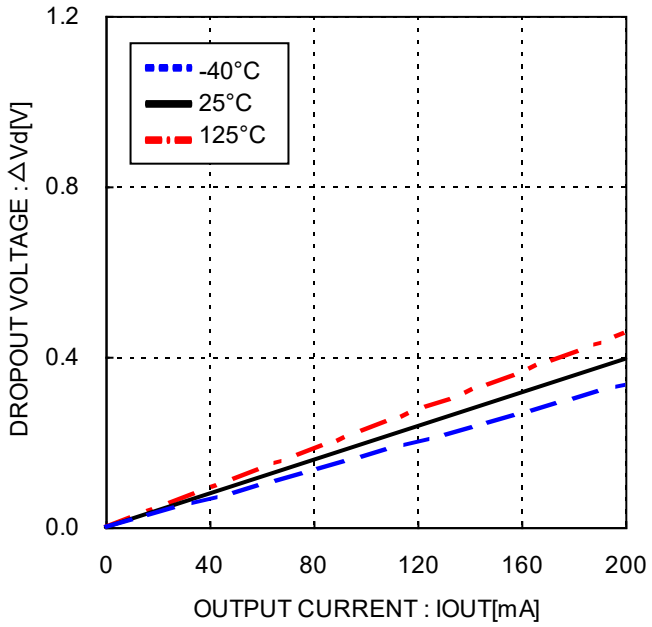



Figure 19. Dropout voltage

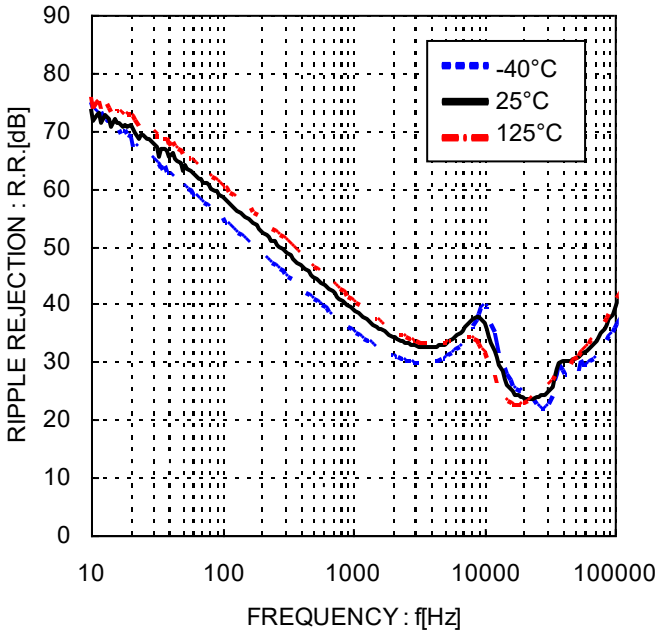



Figure 20. Ripple rejection
(ein=1Vrms,IOUT=100mA)

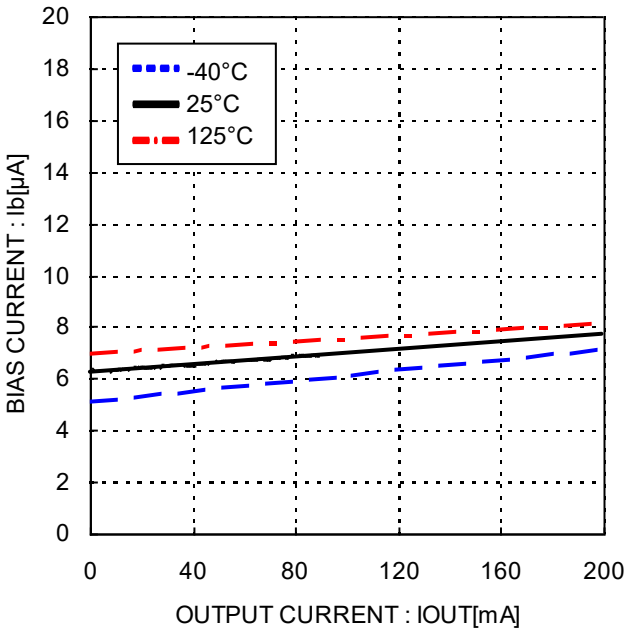



Figure 21. Total supply current vs. Load

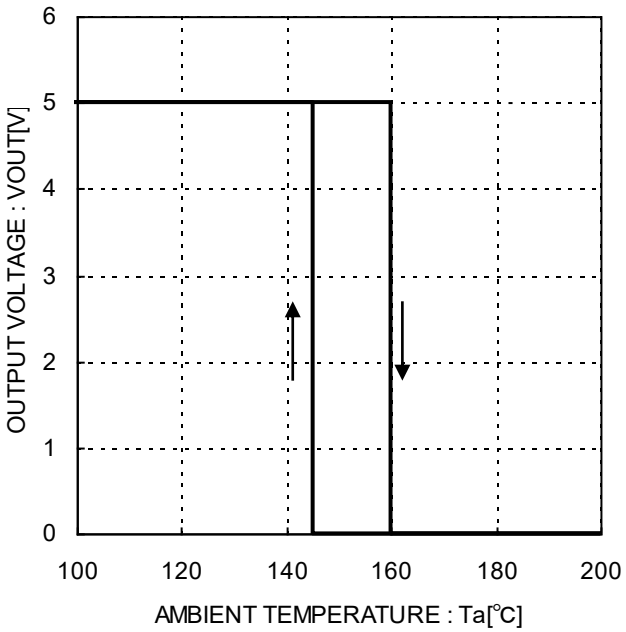



Figure 22. Thermal shutdown
(Output voltage vs. Temperature)


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●**Typical Performance Curves – continued**

■BD750L2EFJ-C, BD750U2EFJ-C, BD750L2FP-C, BD750L2FP3-C Reference data

Unless otherwise specified: -40 < Ta < +125°C, VCC=13.5V, IOUT=0mA

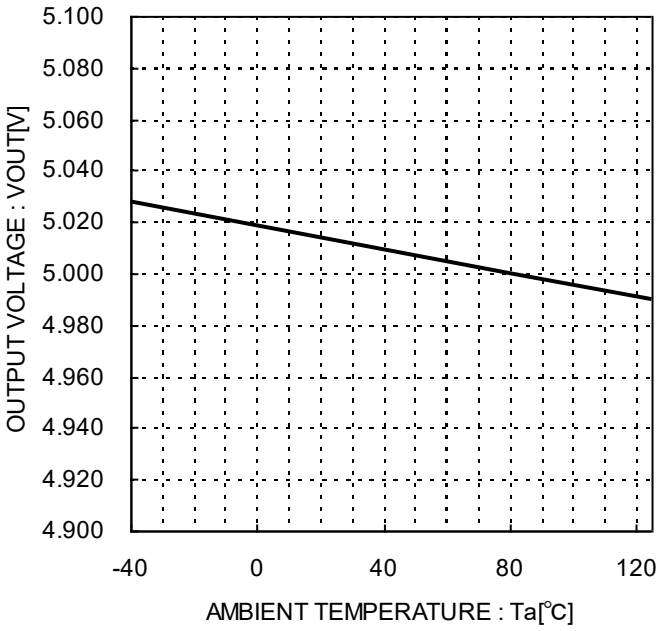



Figure 23. Output voltage vs. Temperature

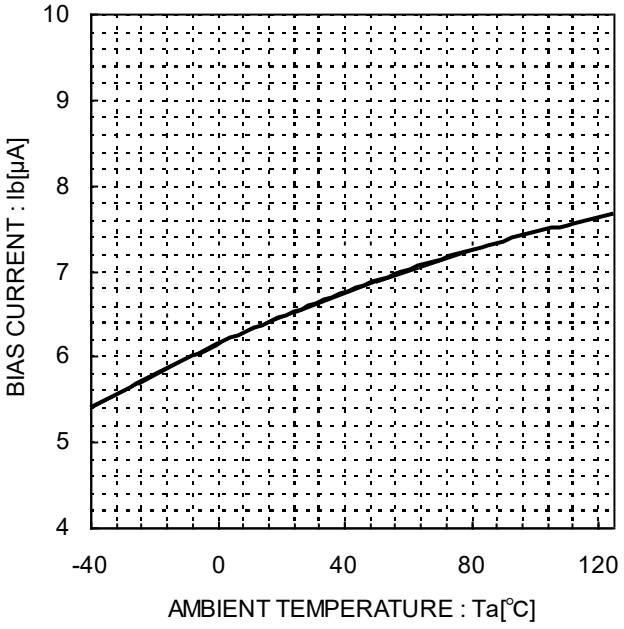
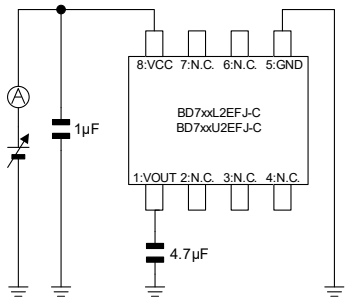


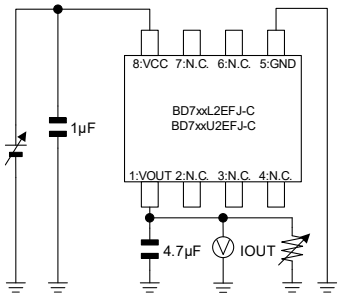

Figure 24. Bias current vs. Temperature


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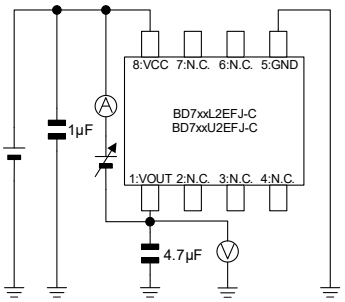
**●Measurement Circuit (BD7xxL2EFJ-C BD7xxU2EFJ-C Series) HTSOP-J8**



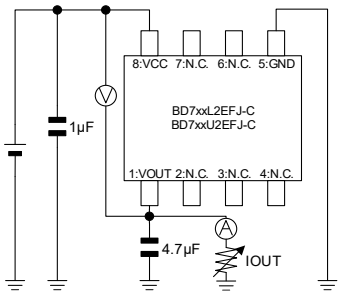

Measurement setup for Figure 5, 14, 15, 24



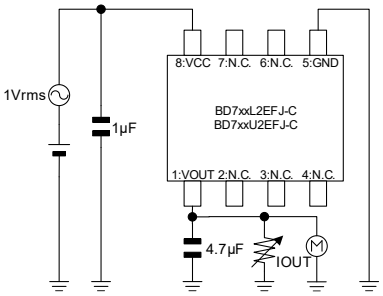

Measurement setup for Figure 6, 7, 12, 13, 16, 17, 22, 23



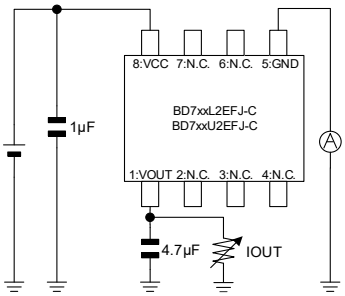

Measurement setup for Figure 8, 18




Measurement setup for Figure 9, 19

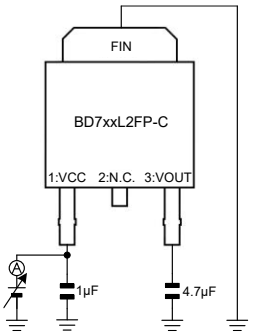



Measurement setup for Figure 10, 20

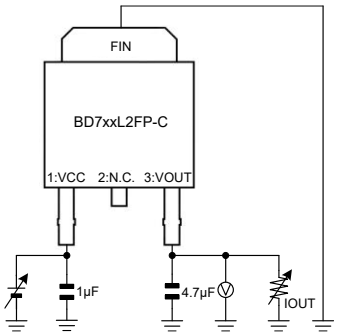



Measurement setup for Figure 11, 21

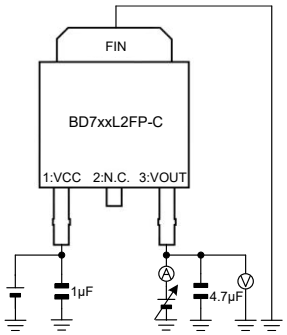
**●Measurement Circuit (BD7xxL2FP-C Series) TO252-3**



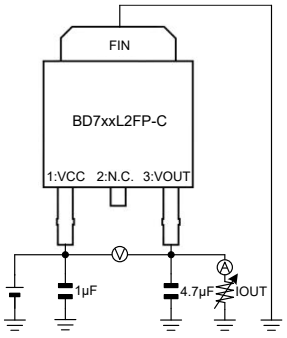

Measurement setup for Figure 5, 14, 15, 24



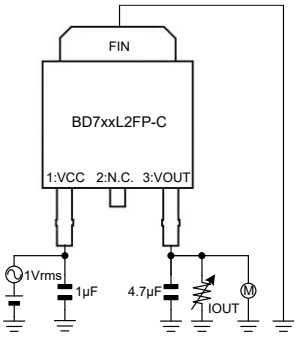

Measurement setup for Figure 6, 7, 12, 13, 16, 17, 22, 23



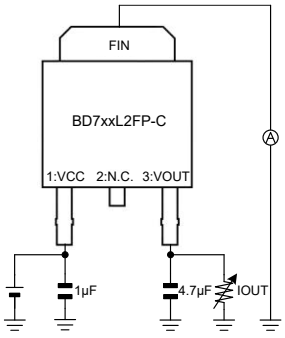

Measurement setup for Figure 8, 18




Measurement setup for Figure 9, 19



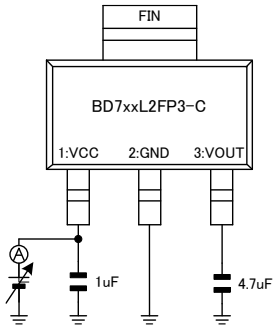

Measurement setup for Figure 10, 20



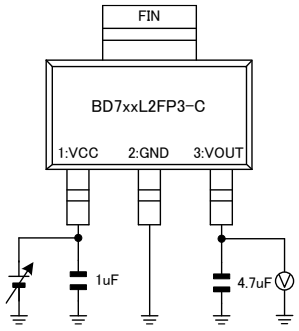

Measurement setup for Figure 11, 21


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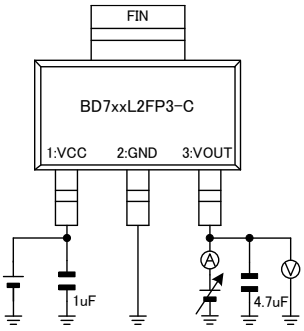
**●Measurement Circuit (BD7xxL2FP3-C Series) SOT223-4(F)**



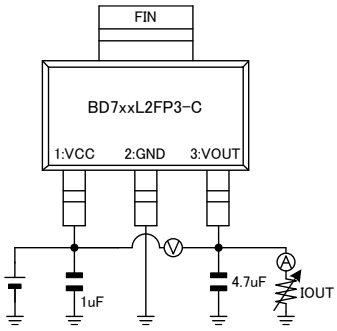

Measurement setup for Figure 5, 14, 15, 24



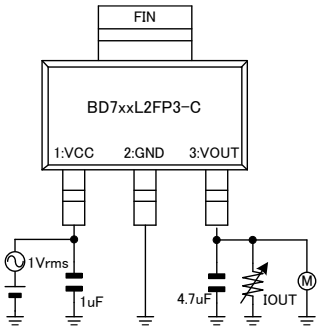

Measurement setup for
Figure 6, 7, 12, 13, 16, 17, 22, 23



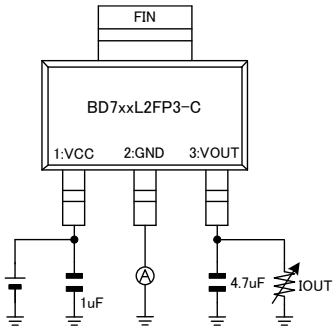

Measurement setup for Figure 8, 18




Measurement setup for Figure 9, 19




Measurement setup for Figure 10, 20




Measurement setup for Figure 11, 21


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## ●Selection of Components Externally Connected

・VCC pin

Insert capacitors with a capacitance of 0.1μF or higher between the VCC and GND pin. Choose the capacitance according to the line between the power smoothing circuit and the VCC pin. Selection of the capacitance also depends on the application. Verify the application and allow for sufficient margins in the design. We recommend using a capacitor with excellent voltage and temperature characteristics.

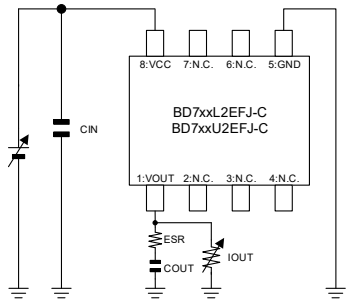
・Output pin capacitor

In order to prevent oscillation, a capacitor needs to be placed between the output pin and GND pin. We recommend using a capacitor with a capacitance of 4.7μF or higher. Electrolytic, tantalum and ceramic capacitors can be used. When selecting the capacitor ensure that the capacitance of 4.7μF or higher is maintained at the intended applied voltage and temperature range. Due to changes in temperature the capacitor's capacitance can fluctuate possibly resulting in oscillation. For selection of the capacitor refer to the IOUT vs. ESR data. The stable operation range given in the reference data is based on the standalone IC and resistive load. For actual applications the stable operating range is influenced by the PCB impedance, input supply impedance and load impedance. Therefore verification of the final operating environment is needed.

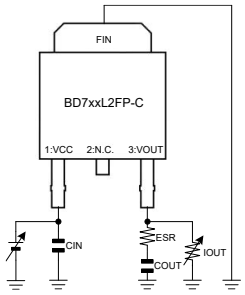
When selecting a ceramic type capacitor, we recommend using X5R, X7R or better with excellent temperature and DC-biasing characteristics and high voltage tolerance.

Also, in case of rapidly changing input voltage and load current, select the capacitance in accordance with verifying that the actual application meets with the required specification.

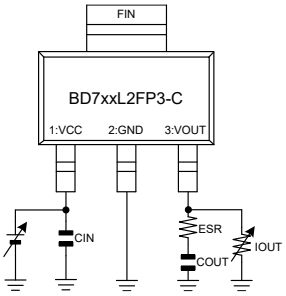
## ●Measurement setup



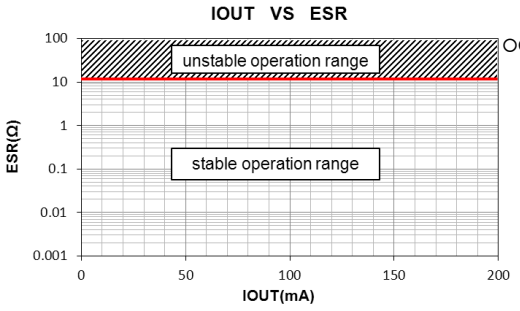

HTSOP-J8

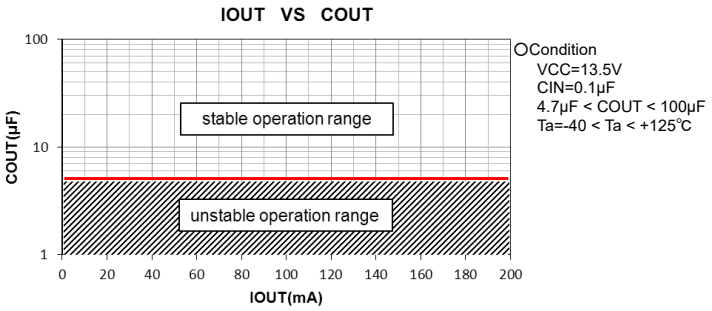



TO252-3




SOT223-4(F)





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## ●Power Dissipation

■HTSOP-J8

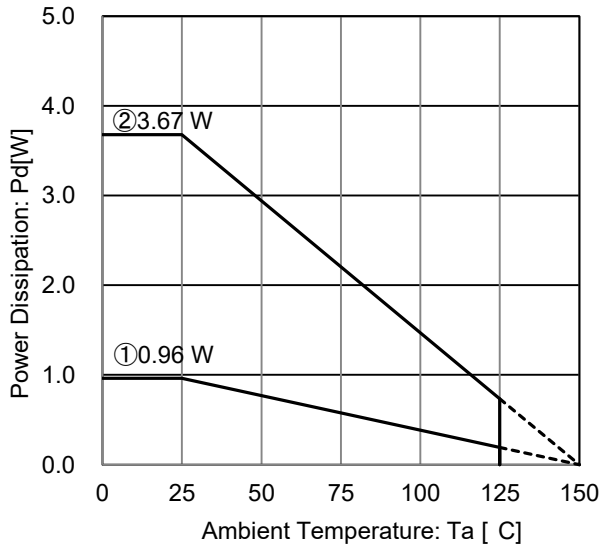



Figure 25. HTSOP-J8 Package Data

IC mounted on ROHM standard board based on JEDEC.
① : 1 - layer PCB
(Copper foil area on the reverse side of PCB: 0 mm x 0 mm)
Board material: FR4
Board size: 114.3 mm x 76.2 mm x 1.57 mmt
Mount condition: PCB and exposed pad are soldered.
Top copper foil: ROHM recommended
footprint + wiring to measure, 2 oz. copper.

② : 4 - layer PCB
(2 inner layers and Copper foil area on the reverse side of PCB: 74.2 mm x 74.2 mm)
Board material: FR4
Board size: 114.3 mm x 76.2 mm x 1.60 mmt
Mount condition: PCB and exposed pad are soldered.
Top copper foil: ROHM recommended
footprint + wiring to measure, 2 oz. copper.
2 inner layers copper foil area of PCB
: 74.2 mm x 74.2 mm, 1 oz. copper.
Copper foil area on the reverse side of PCB
: 74.2 mm x 74.2 mm, 2 oz. copper.

Condition①: $\theta_{JA}$ = 130 C / W, $\Psi_{JT}$ (top center) = 15 °C / W
Condition②: $\theta_{JA}$ = 34 C / W, $\Psi_{JT}$ (top center) = 7 °C / W

■TO252-3

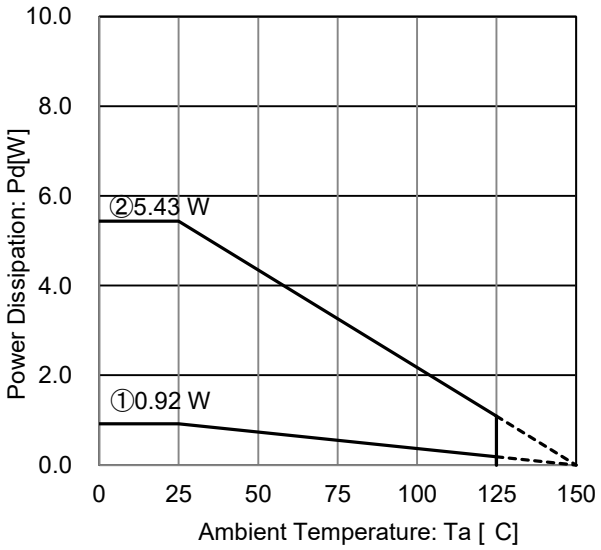



Figure 26. TO252-3 Package Data

IC mounted on ROHM standard board based on JEDEC.
① : 1 - layer PCB
(Copper foil area on the reverse side of PCB: 0 mm x 0 mm)
Board material: FR4
Board size: 114.3 mm x 76.2 mm x 1.57 mmt
Mount condition: PCB and exposed pad are soldered.
Top copper foil: ROHM recommended
footprint + wiring to measure, 2 oz. copper.

② : 4 - layer PCB
(2 inner layers and Copper foil area on the reverse side of PCB: 74.2 mm x 74.2 mm)
Board material: FR4
Board size: 114.3 mm x 76.2 mm x 1.60 mmt
Mount condition: PCB and exposed pad are soldered.
Top copper foil: ROHM recommended
footprint + wiring to measure, 2 oz. copper.
2 inner layers copper foil area of PCB
: 74.2 mm x 74.2 mm, 1 oz. copper.
Copper foil area on the reverse side of PCB
: 74.2 mm x 74.2 mm, 2 oz. copper.

Condition①: $\theta_{JA}$ = 136 C / W, $\Psi_{JT}$ (top center) = 17 °C / W
Condition②: $\theta_{JA}$ = 23 °C / W, $\Psi_{JT}$ (top center) = 3 °C / W


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■SOT223-4(F)

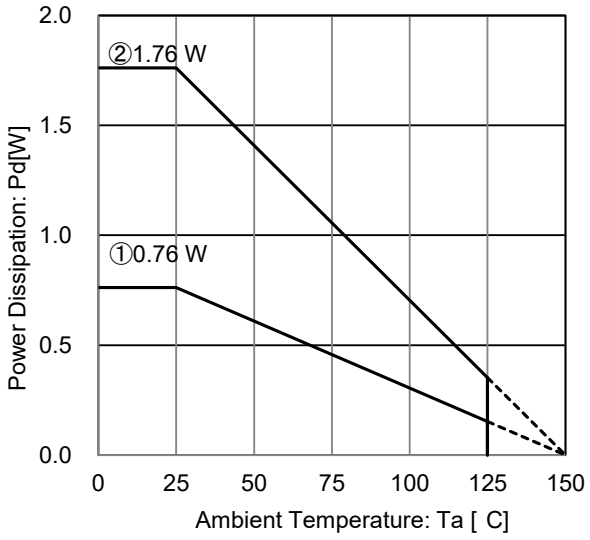



Figure 27. SOT223-4(F) Package Data

IC mounted on ROHM standard board based on JEDEC.

① : 1 - layer PCB
(Copper foil area on the reverse side of PCB: 0 mm x 0 mm)
Board material: FR4
Board size: 114.3 mm x 76.2 mm x 1.57 mm
Mount condition: PCB and exposed pad are soldered.
Top copper foil: ROHM recommended
footprint + wiring to measure, 2 oz. copper.

② : 4 - layer PCB
(2 inner layers and Copper foil area on the reverse side of PCB: 74.2 mm x 74.2 mm)
Board material: FR4
Board size: 114.3 mm x 76.2 mm x 1.60 mm
Mount condition: PCB and exposed pad are soldered.
Top copper foil: ROHM recommended
footprint + wiring to measure, 2 oz. copper.
2 inner layers copper foil area of PCB
: 74.2 mm x 74.2 mm, 1 oz. copper.
Copper foil area on the reverse side of PCB
: 74.2 mm x 74.2 mm, 2 oz. copper.

Condition①: $\theta_{JA}$ = 164 C / W, $\Psi_{JT}$ (top center) = 20 °C / W
Condition②: $\theta_{JA}$ = 71 C / W, $\Psi_{JT}$ (top center) = 14 °C / W


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Refer to the heat mitigation characteristics illustrated in Figure 25 to Figure 27 when using the IC in an environment of $T_a \geq 25°C$. The characteristics of the IC are greatly influenced by the operating temperature, and it is necessary to operate under the maximum junction temperature Timax.
Even if the ambient temperature Ta is at 25°C it is possible that the junction temperature Tj reaches high temperatures. Therefore, the IC should be operated within the power dissipation range.

The following method is used to calculate the power consumption Pc (W)

$$Pc=(VCC-VOUT)\times IOUT+VCC\times Ib$$
$$\text{Power dissipation } Pd \geq Pc$$

VCC : Input voltage
VOUT : Output voltage
IOUT : Load current
Ib : Bias current
Ishort : Shorted current

The load current Lo is obtained by operating the IC within the power dissipation range.

$$IOUT \leq \frac{Pd-VCC\times Ib}{VCC-VOUT}$$

(Refer to Figure 11 and Figure 21 for the Ib)

Thus, the maximum load current IOUTmax for the applied voltage VCC can be calculated during the thermal design process.

●HTSOP-J8

■Calculation example 1) with Ta=125°C, VCC=13.5V, VOUT=3.3V

$$IOUT \leq \frac{0.73-13.5\times Ib}{10.2}$$
$$IOUT \leq 71.5mA \quad (Ib: 6\mu A)$$

θja=34°C/W → -29.4mW/°C
25°C=3.67W → 125°C=0.73W

At Ta=125°C with Figure 25 ② condition, the calculation shows that ca 71.5mA of output current is possible at 10.2V potential difference across input and output.

■Calculation example 2) with Ta=125°C, VCC=13.5V, VOUT=5.0V

$$IOUT \leq \frac{0.73-13.5\times Ib}{8.5}$$
$$IOUT \leq 85.8mA \quad (Ib: 6\mu A)$$

θja=34°C/W → -29.4mW/°C
25°C=3.67W → 125°C=0.73W

At Ta=125°C with Figure 25 ② condition, the calculation shows that ca 85.8mA of output current is possible at 8.5V potential difference across input and output.

The thermal calculation shown above should be taken into consideration during the thermal design in order to keep the whole operating temperature range within the power dissipation range.
In the event of shorting (i.e. VOUT and GND pins are shorted) the power consumption Pc of the IC can be calculated as follows:

$$Pc=VCC\times(Ib+Ishort)$$ (Refer to Figure 8 and Figure 18 for the Ishort)


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●TO252-3

■Calculation example 3) with Ta=125°C, VCC=13.5V, VOUT=3.3V

$$IOUT \leq \frac{1.08 - 13.5 \times Ib}{10.2}$$

IOUT ≤ 105mA (Ib: 6μA)

θja=23°C/W → -43.5mW/°C
25°C=5.43W → 125°C=1.08W

At Ta=125°C with Figure 26 ② condition, the calculation shows that ca 105mA of output current is possible at 10.2V potential difference across input and output.

■Calculation example 4) with Ta=125°C, VCC=13.5V, VOUT=5.0V

$$IOUT \leq \frac{1.08 - 13.5 \times Ib}{8.5}$$

IOUT ≤ 127mA (Ib: 6μA)

θja=23°C/W → -43.5mW/°C
25°C=5.43W → 125°C=1.08W

At Ta=125°C with Figure 26 ② condition, the calculation shows that ca 127mA of output current is possible at 8.5V potential difference across input and output.

The thermal calculation shown above should be taken into consideration during the thermal design in order to keep the whole operating temperature range within the power dissipation range.
In the event of shorting (i.e. VOUT and GND pins are shorted) the power consumption Pc of the IC can be calculated as follows:

Pc=VCC×(Ib+Ishort) (Refer to Figure 8 and Figure 18 for the Ishort)


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●SOT223-4(F)

■Calculation example 5) with Ta=125°C, VCC=13.5V, VOUT=3.3V

$$IOUT \leq \frac{0.35 - 13.5 \times Ib}{10.2}$$

$$IOUT \leq 34.3mA \quad (Ib: 6\mu A)$$

θja=71°C/W → -14.1mW/°C
25°C=1.76W → 125°C=0.35W

At Ta=125°C with Figure 27 ② condition, the calculation shows that ca 34.3mA of output current is possible at 10.2V potential difference across input and output.

■Calculation example 6) with Ta=125°C, VCC=13.5V, VOUT=5.0V

$$IOUT \leq \frac{0.35 - 13.5 \times Ib}{8.5}$$

$$IOUT \leq 41.1mA \quad (Ib: 6\mu A)$$

θja=71°C/W → -14.1mW/°C
25°C=1.76W → 125°C=0.35W

At Ta=125°C with Figure 27 ② condition, the calculation shows that ca 41.1mA of output current is possible at 8.5V potential difference across input and output.

The thermal calculation shown above should be taken into consideration during the thermal design in order to keep the whole operating temperature range within the power dissipation range.
In the event of shorting (i.e. VOUT and GND pins are shorted) the power consumption Pc of the IC can be calculated as follows:

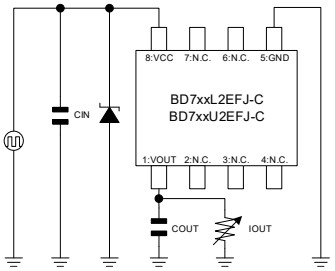
$Pc = VCC \times (Ib + Ishort)$ (Refer to Figure 8 and Figure 18 for the Ishort)


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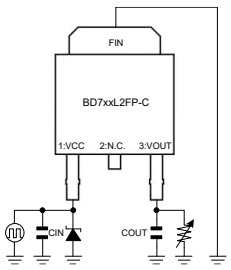
## ●Application Examples

・Applying positive surge to the VCC pin

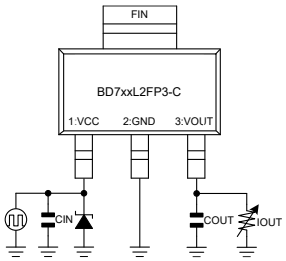
If the possibility exists that surges higher than 50V will be applied to the VCC pin, a zenar diode should be placed between the VCC pin and GND pin as shown in the figure below.




HTSOP-J8



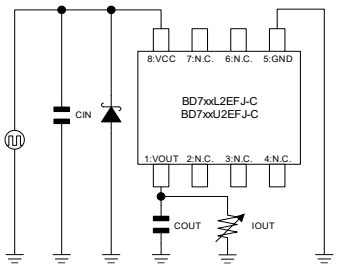

TO252-3



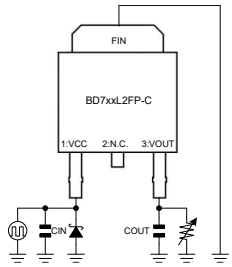

SOT223-4(F)

・Applying negative surge to the VCC pin

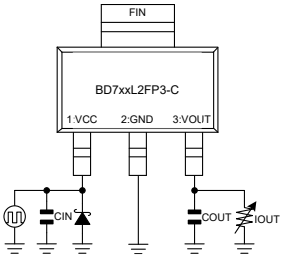
If the possibility exists that negative surges lower than the GND are applied to the VCC pin, a Shottky diode should be place between the VCC pin and GND pin as shown in the figure below.




HTSOP-J8



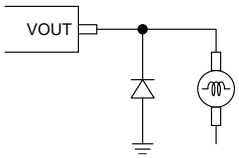

TO252-3




SOT223-4(F)

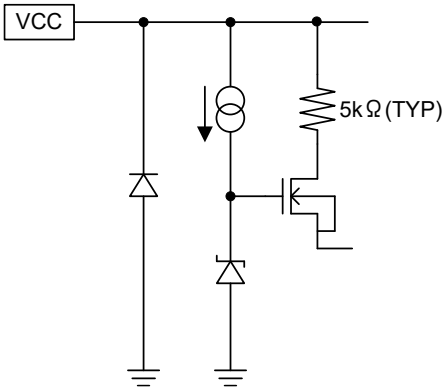
・Implementing a protection diode

If the possibility exists that a large inductive load is connected to the output pin resulting in back-EMF at time of startup and shutdown, a protection diode should be placed as shown in the figure below.

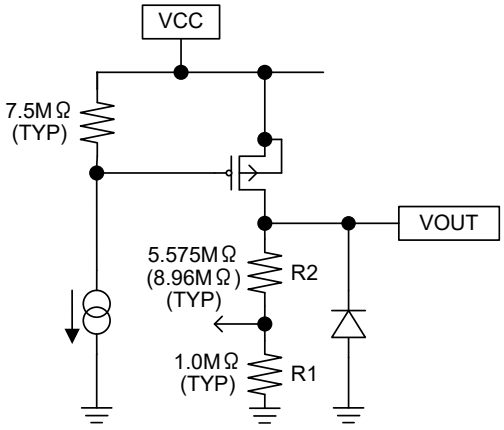



## ●I/O equivalence circuits

○Input terminal




○Output terminal *inside of () shows 5V





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## ●Operational Notes

1) Absolute maximum ratings

Exceeding the absolute maximum rating for supply voltage, operating temperature or other parameters can result in damages to or destruction of the chip. In this event it also becomes impossible to determine the cause of the damage (e.g. short circuit, open circuit, etc.). Therefore, if any special mode is being considered with values expected to exceed the absolute maximum ratings, implementing physical safety measures, such as adding fuses, should be considered.

2) The electrical characteristics given in this specification may be influenced by conditions such as temperature, supply voltage and external components. Transient characteristics should be sufficiently verified.

3) GND electric potential

Keep the GND pin potential at the lowest (minimum) level under any operating condition. Furthermore, ensure that, including the transient, none of the pin's voltages are less than the GND pin voltage.

4) GND wiring pattern

When both a small-signal GND and a high current GND are present, single-point grounding (at the set standard point) is recommended. This in order to separate the small-signal and high current patterns and to ensure that voltage changes stemming from the wiring resistance and high current do not cause any voltage change in the small-signal GND. Similarly, care must be taken to avoid wiring pattern fluctuations in any connected external component GND.

5) Inter-pin shorting and mounting errors

Ensure that when mounting the IC on the PCB the direction and position are correct. Incorrect mounting may result in damaging the IC. Also, shorts caused by dust entering between the output, input and GND pin may result in damaging the IC.

6) Inspection using the set board

The IC needs to be discharged after each inspection process as, while using the set board for inspection, connecting a capacitor to a low-impedance pin may cause stress to the IC. As a protection from static electricity, ensure that the assembly setup is grounded and take sufficient caution with transportation and storage. Also, make sure to turn off the power supply when connecting and disconnecting the inspection equipment.

7) Thermal design

The power dissipation under actual operating conditions should be taken into consideration and a sufficient margin should be allowed for in the thermal design. On the reverse side of the package this product has an exposed heat pad for improving the heat dissipation. Use both the front and reverse side of the PCB to increase the heat dissipation pattern as far as possible. The amount of heat generated depends on the voltage difference across the input and output, load current, and bias current. Therefore, when actually using the chip, ensure that the generated heat does not exceed the Pd rating. Should by any condition the maximum junction temperature rating be exceeded by the temperature increase of the chip, it may result in deterioration of the properties of the chip. The thermal impedance in this specification is based on recommended PCB and measurement condition by JEDEC standard. Verify the application and allow sufficient margins in the thermal design.

(Tjmax: maximum junction temperature=150°C, Ta: ambient temperature (°C), θja: junction-to-ambient thermal resistance (°C/W), Pd: power dissipation rating (W), Pc: power consumption (W), VCC: input voltage, VOUT: output voltage, IOUT: load current, Ib: bias current)

Power dissipation rating Pd (W)=(Tjmax－Ta)/θja
Power consumption Pc (W)=(VCC-VOUT)×IOUT＋VCC×Ib

8) Rapid variation in VCC voltage and load current

In case of a rapidly changing input voltage, transients in the output voltage might occur due to the use of a MOSFET as output transistor. Although the actual application might be the cause of the transients, the IC input voltage, output current and temperature are also possible causes. In case problems arise within the actual operating range, use countermeasures such as adjusting the output capacitance.


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9) Minute variation in output voltage

In case of using an application susceptible to minute changes to the output voltage due to noise, changes in input and load current, etc., use countermeasures such as implementing filters.

10) Overcurrent protection circuit

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

11) Thermal shutdown (TSD)

This IC incorporates and integrated thermal shutdown circuit to prevent heat damage to the IC. Normal operation should be within the power dissipation rating, if however the rating is exceeded for a continued period, the junction temperature (Tj) will rise and the TSD circuit will be activated and turn all output pins OFF. After the Tj falls below the TSD threshold the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

12) In some applications, the VCC and pin potential might be reversed, possibly resulting in circuit internal damage or damage to the elements. For example, while the external capacitor is charged, the VCC shorts to the GND. Use a capacitor with a capacitance with less than 1000μF. We also recommend using reverse polarity diodes in series or a bypass between all pins and the VCC pin.

13) This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements.

For example, in case a resistor and a transistor are connected to the pins as shown in the figure below then:

○ The P/N junction functions as a parasitic diode when GND > pin A for the resistor, or GND > pin B for the transistor.

○ Also, when GND > pin B for the transistor (NPN), the parasitic diode described above combines with the N layer of the other adjacent elements to operate as a parasitic NPN transistor.

Parasitic diodes inevitably occur in the structure of the IC. Their operation can result in mutual interference between circuits and can cause malfunctions and, in turn, physical damage to or destruction of the chip. Therefore do not employ any method in which parasitic diodes can operate such as applying a voltage to an input pin that is lower than the (P substrate) GND.

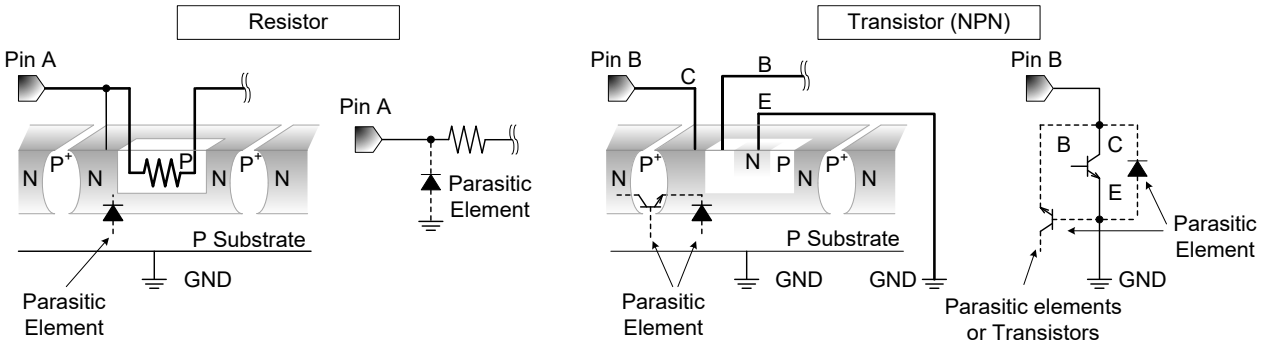
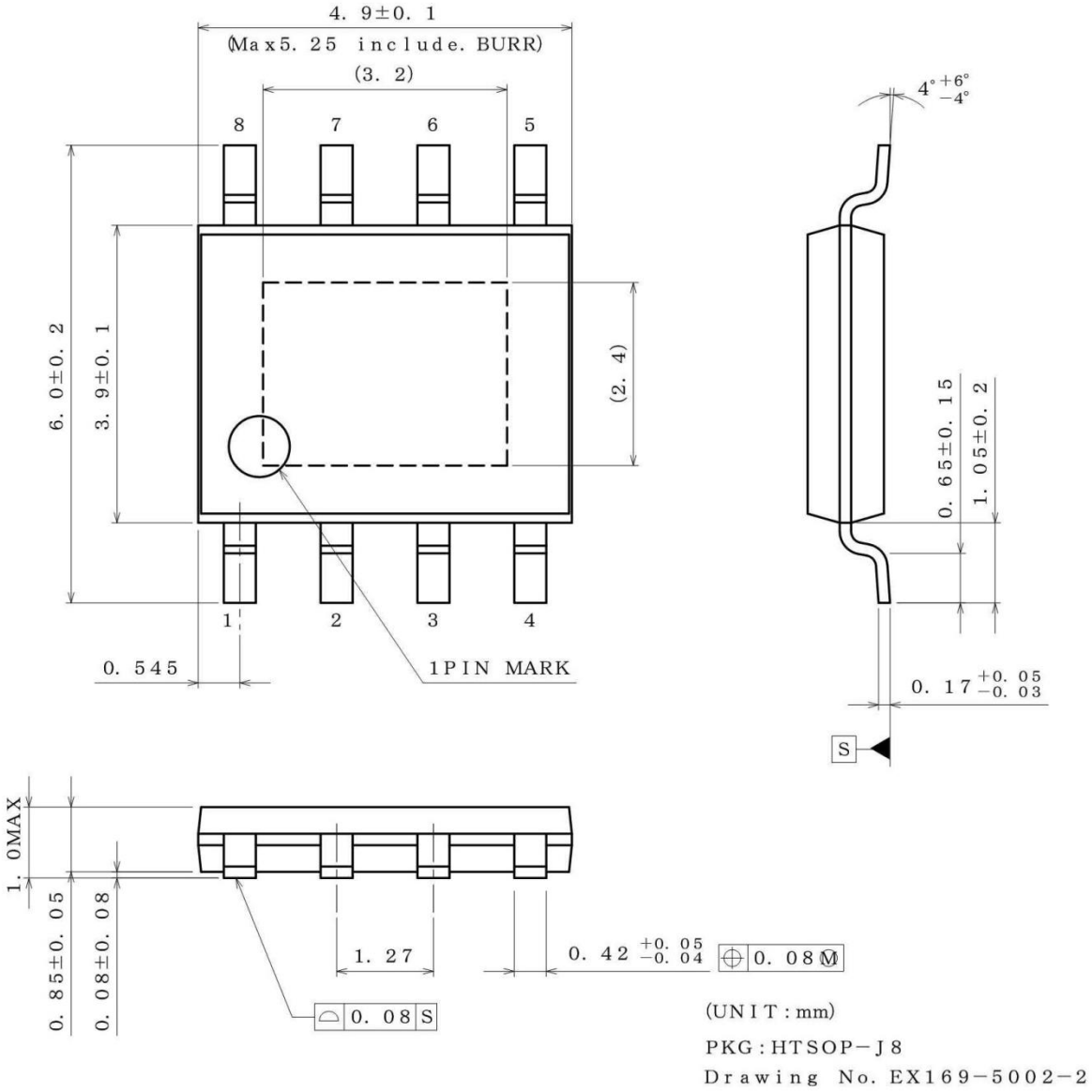



Figure 28. Example of the Parasitic Device Structures


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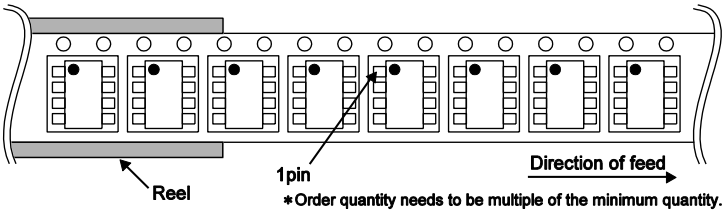
●**Physical Dimension, Tape and Reel Information**

| Package Name | HTSOP-J8 |
|---|---|




**<Tape and Reel information>**

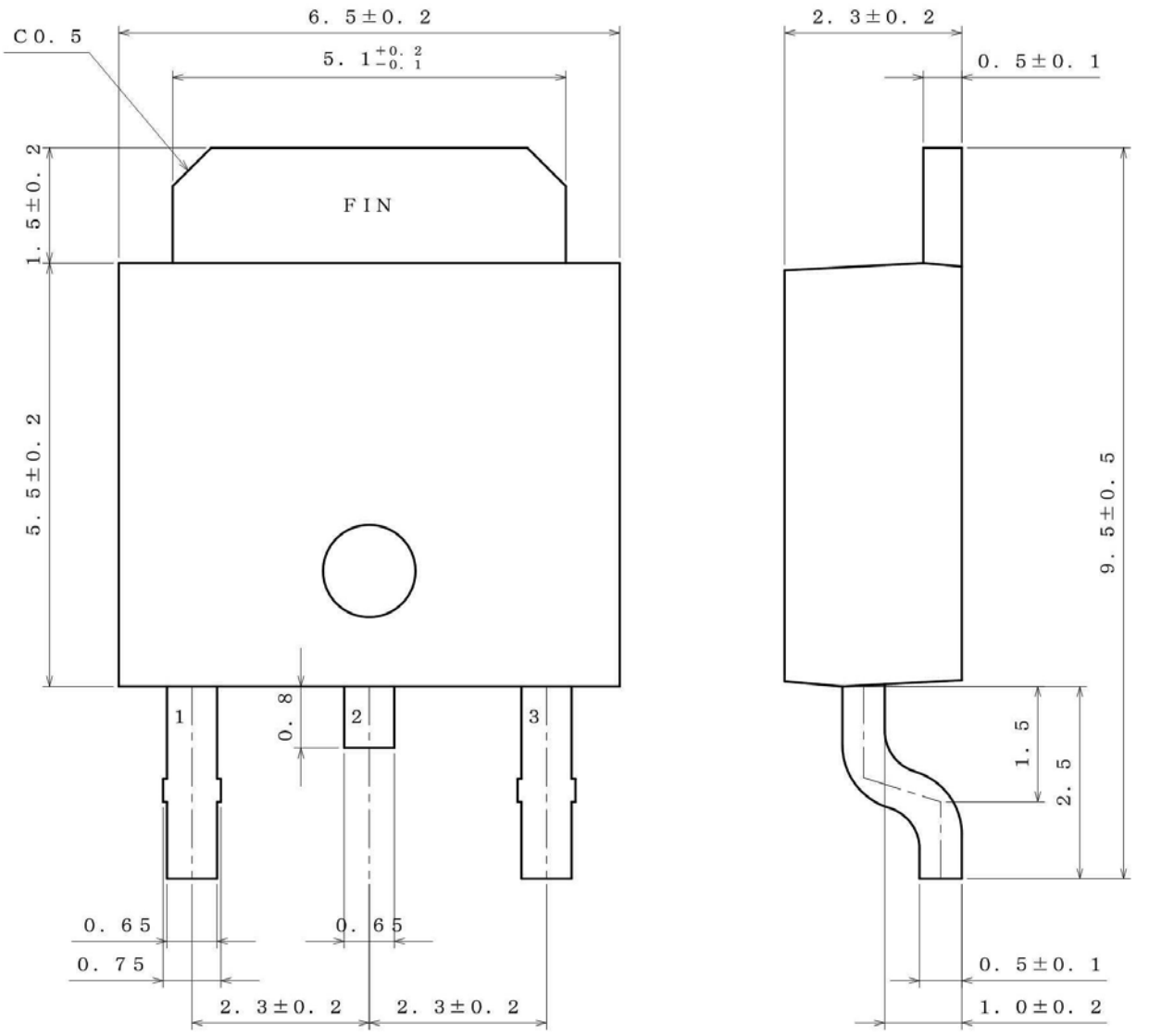
| | |
|---|---|
| Tape | Embossed carrier tape |
| Quantity | 2500pcs |
| Direction of feed | E2<br>( The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand ) |




*Order quantity needs to be multiple of the minimum quantity.


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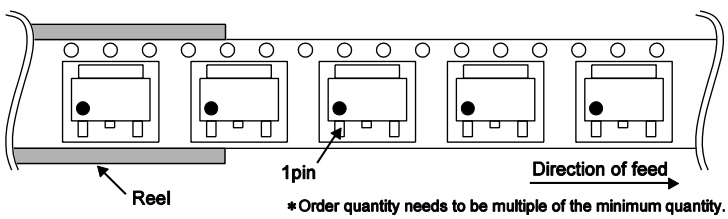
| Package Name | TO252-3 |
|---|---|




(UNITS;mm)
PKG:TO252-3
Drawing No. EX535-5001-1

<Tape and Reel information>

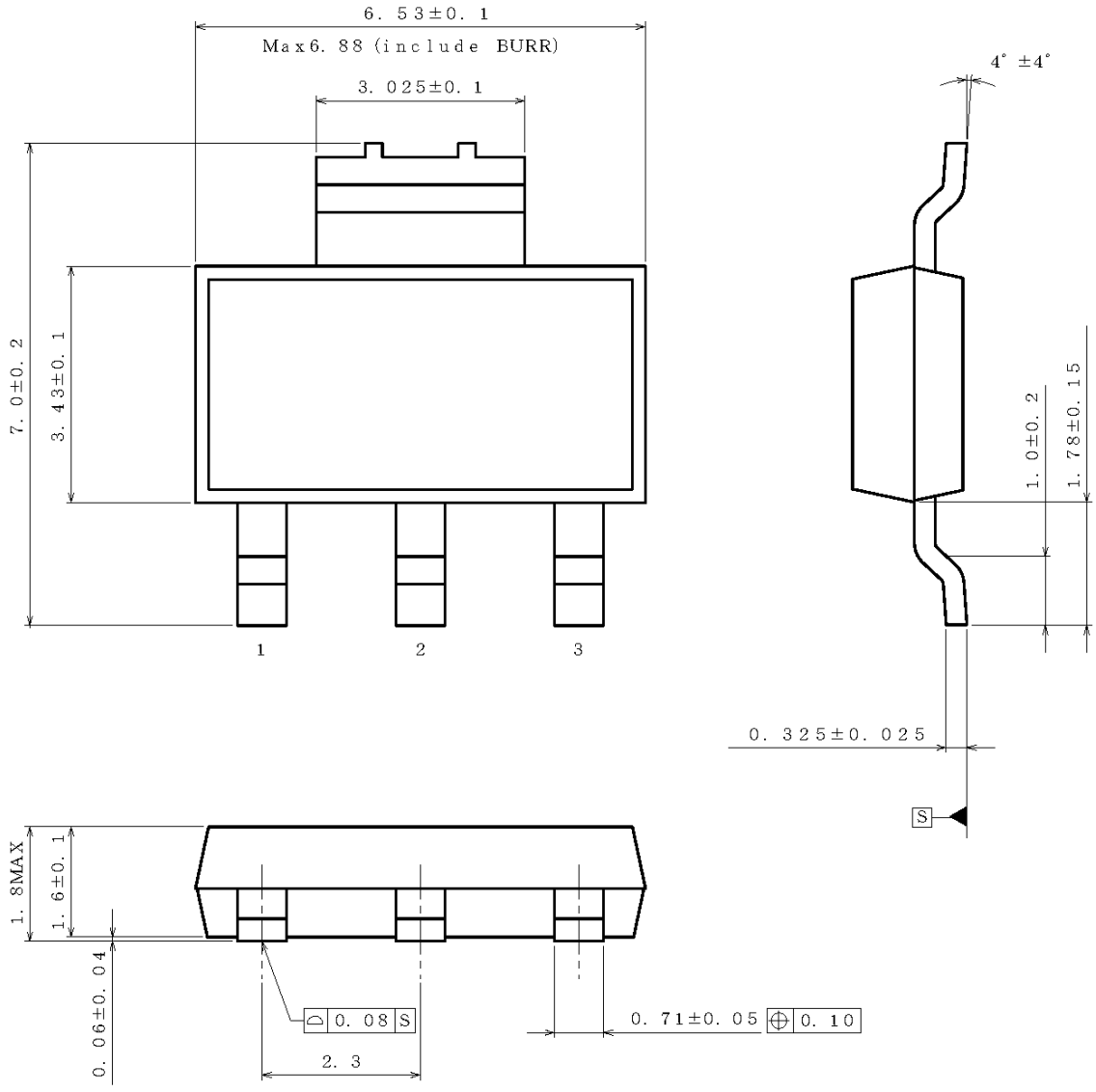
| | |
|---|---|
| Tape | Embossed carrier tape |
| Quantity | 2000pcs |
| Direction of feed | E2<br>( The direction is the 1pin of product is at the lower left when you hold reel on the left hand and you pull out the tape on the right hand ) |




*Order quantity needs to be multiple of the minimum quantity.


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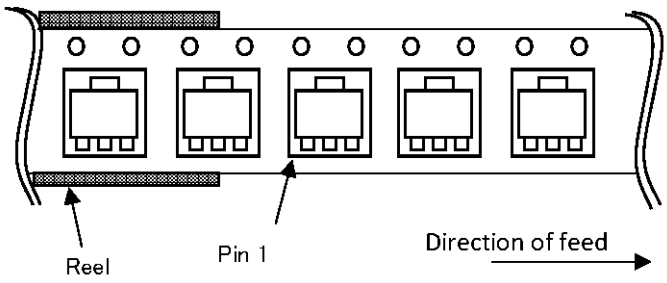
| Package Name | SOT223-4 |
|---|---|




(UNIT:mm)
PKG : SOT223-4
Drawing No. EX571-5002

< Tape and Reel Information >

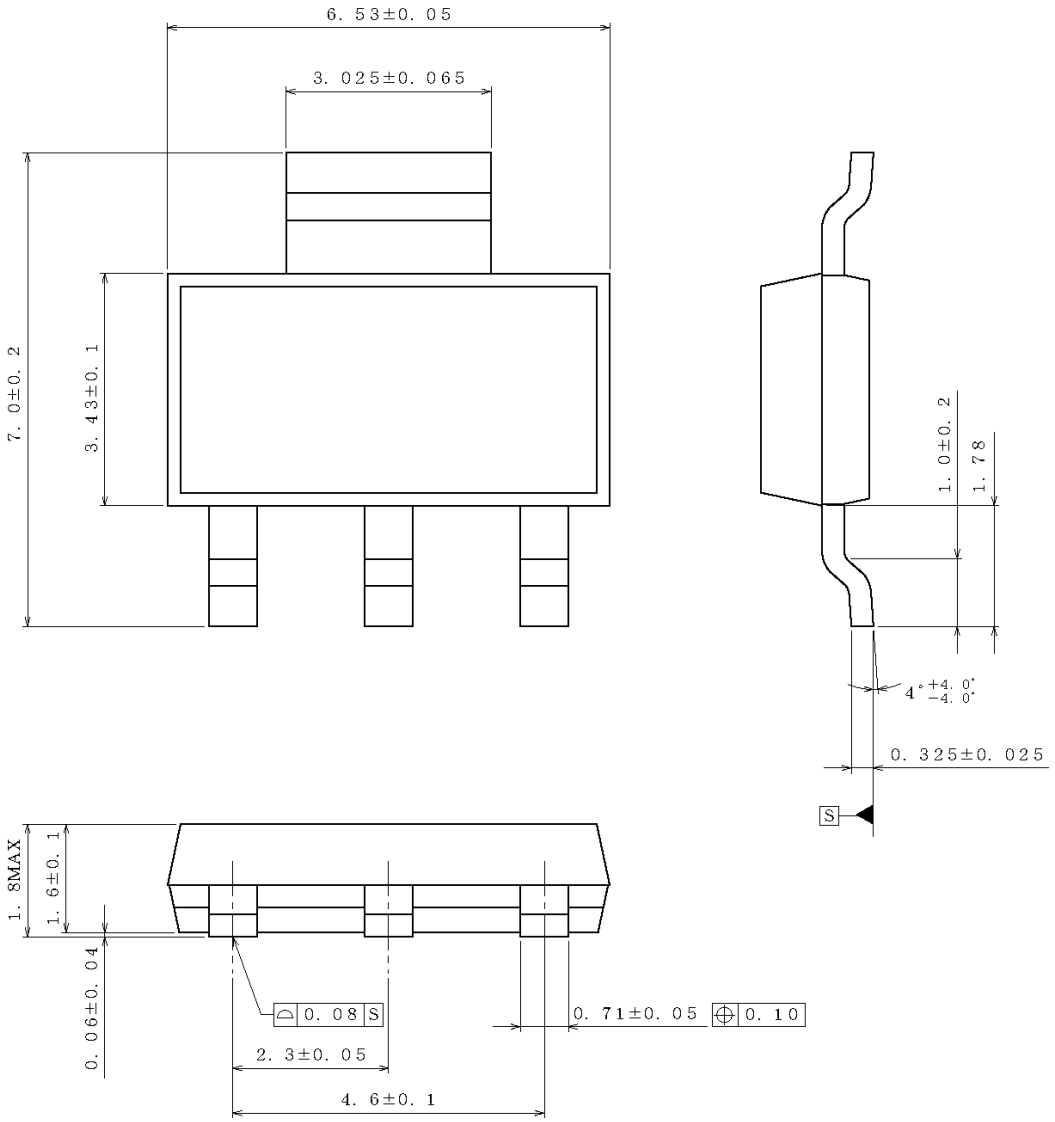
| Tape | Embossed carrier tape |
|---|---|
| Quantity | 2000pcs |
| Direction of feed | E2<br>( The direction is the 1pin of product is at the lower left when you hold reel on the left hand and you pull out the tape on the right hand ) |





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| Package Name | SOT223-4F |
|---|---|

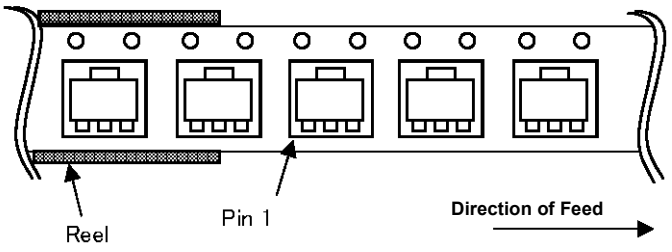



(UNIT:mm)

Drawing No. EX561-5001

< Tape and Reel Information >

| Tape | Embossed carrier tape |
|---|---|
| Quantity | 2000pcs |
| Direction of feed | E2<br>( The direction is the 1pin of product is at the lower left when you hold reel on the left hand and you pull out the tape on the right hand ) |

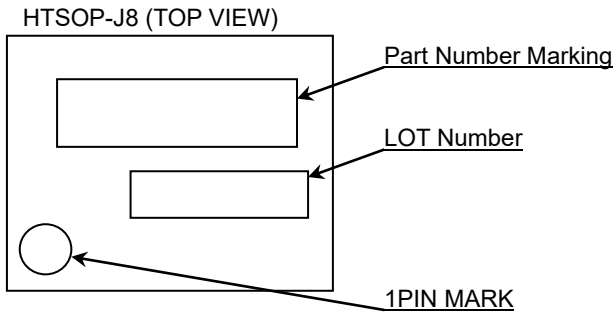




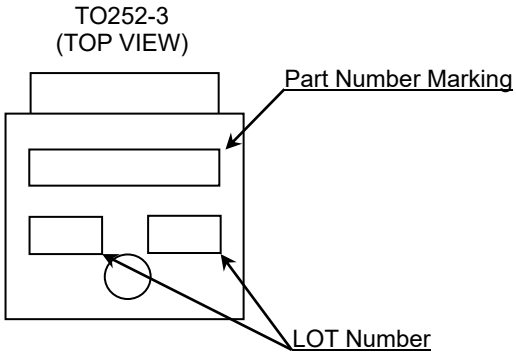
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●**Marking Diagrams**

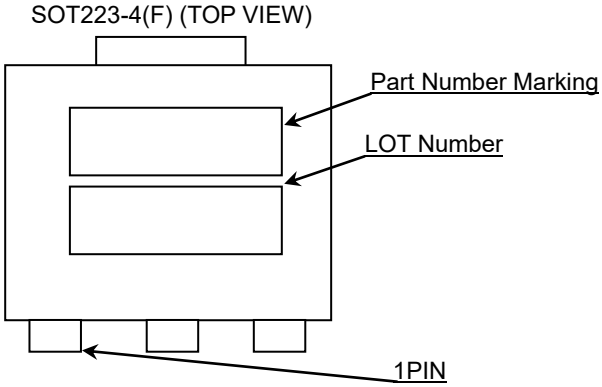
**HTSOP-J8**




**TO252-3**




**SOT223-4(F)**




| Orderable Part Number | Part Number Marking | Output Voltage (V) | Package |
|---|---|---|---|
| BD733L2EFJ-CE2 | D733L2 | 3.3 | HTSOP-J8 |
| BD733U2EFJ-CE2 | D733U2 | | HTSOP-J8 |
| BD733L2FP-CE2 | BD733L2 | | TO252-3 |
| BD733L2FP3-CE2 | BD733L2 | | SOT223-4(F) |
| BD750L2EFJ-CE2 | D750L2 | 5.0 | HTSOP-J8 |
| BD750U2EFJ-CE2 | D750U2 | | HTSOP-J8 |
| BD750L2FP-CE2 | BD750L2 | | TO252-3 |
| BD750L2FP3-CE2 | BD750L2 | | SOT223-4(F) |


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●**Revision History**

| Date | Revision | Changes |
|---|---|---|
| 21.Aug.2012 | 001 | New Release |
| 24.Sep.2012 | 002 | New Release TO252-3 package. |
| 14.Mar.2013 | 003 | Page 1.Series name is changed.<br>Page 6. Append Thermal Resistance θja, θjc.<br>Page 8. Figure 5, Page 9. Figure 11 All Quiescent current are integrated into Bias Current.<br>Page 10. Figure 14, Page 11. Figure 15 All Quiescent current are integrated into Bias Current.<br>Page 12. Figure 21, Page 13. Figure 24 All Quiescent current are integrated into Bias Current.<br>Page 17, 18. Figure 25, 26, 27, 28<br>Power Dissipation is changed to be compliant with JEDEC standard.<br>Page 19, 20. Calculation examples are changed.<br>Page 25. “Application example” is deleted.<br>Figure 29 “ Example of the Parasitic Device Structures” is renewed. |
| 30.Sep.2013 | 004 | AEC-Q100 Qualified<br>Page 28. Physical Quantity is changed. |
| 01.May.2014 | 005 | TO263-3F is changed to the individual registration. |
| 14.Jul.2014 | 006 | Page 16. Output capacitor range was changed.<br>Page 28. HTSOP-J8 Marking Diagrams is changed. |
| 17.Feb.2017 | 007 | Improve the description, SOT223-4F to SOT223-4(F).<br>Page 1. AEC-Q100 Grade postscript.<br>Page 6. Thermal resistance is changed for JESD51-2A.<br>Page 10. Revised Figure 13.<br>Page 17, 18. Value of the power dissipation is changed.<br>Page 23. Revised 7) in Operational Notes with change of Thermal resistance.<br>Page 27. Add Physical Dimension, Tape and Reel Information of SOT223-4 package. |
| 19.Nov.2021 | 008 | Add BD7xxU2EFJ-C Series. |


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# Notice

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| JAPAN | USA | EU | CHINA |
|---|---|---|---|
| CLASSⅢ | CLASSⅢ | CLASSⅡb | CLASSⅢ |
| CLASSⅣ | | CLASSⅢ | |

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   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

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6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification


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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

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   [a] the Products are exposed to sea winds or corrosive gases, including $Cl_2$, $H_2S$, $NH_3$, $SO_2$, and $NO_2$
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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