For Automotive
1A, 8.0V Output LDO Regulator

BD80C0AFPS-C

General Description

The BD80C0AFPS-C is a low-saturation regulator which is 8.0V output voltage and 1A output current capability. Electrolytic, tantalum and ceramic capacitors can be used as output capacitor to prevent oscillation. The IC has a built-in over current protection circuit that prevents the destruction of the IC due to output short circuits and a thermal shutdown circuit that protects the IC from thermal damage due to overloading.

Key Specifications

- Temperature Range (Ta): -40°C to +125°C
- Operating Input Range: 9.0V to 26.5V
- Circuit Current: 0.6mA (Typ)
- Output Current Capability: 1A
- High Output Voltage Accuracy: ±1%(Ta = +25 °C)
  ±3%(-40 °C ≤ Ta ≤ +125 °C)

Features

- AEC-Q100 Qualified*(Note 1)*
- Over Current Protection (OCP)
- Thermal Shutdown Protection (TSD)

(Note 1) Grade 1

Package
TO252S-3

W(Typ) x D(Typ) x H(Max)
6.50mm x 9.50mm x 1.30mm

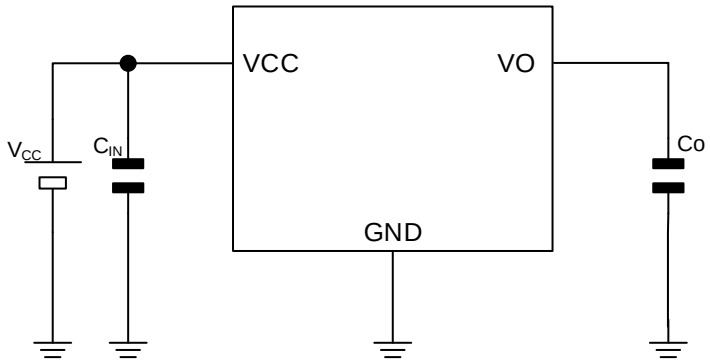


Applications

- Power Train
- Body
- Audio System
- Navigation System

Typical Application Circuit

- VCC and VO pin capacitors: 1 µF ≤ C_{IN} (Min), 1 µF ≤ C_O (Min)
  Please refer to the "Application and Implemention".



Typical Application Circuit

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays.

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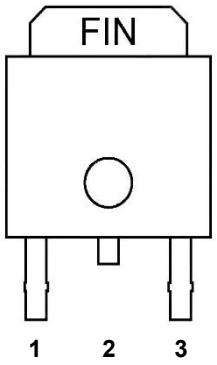
Pin Configurations

TO252S-3
(TOP VIEW)

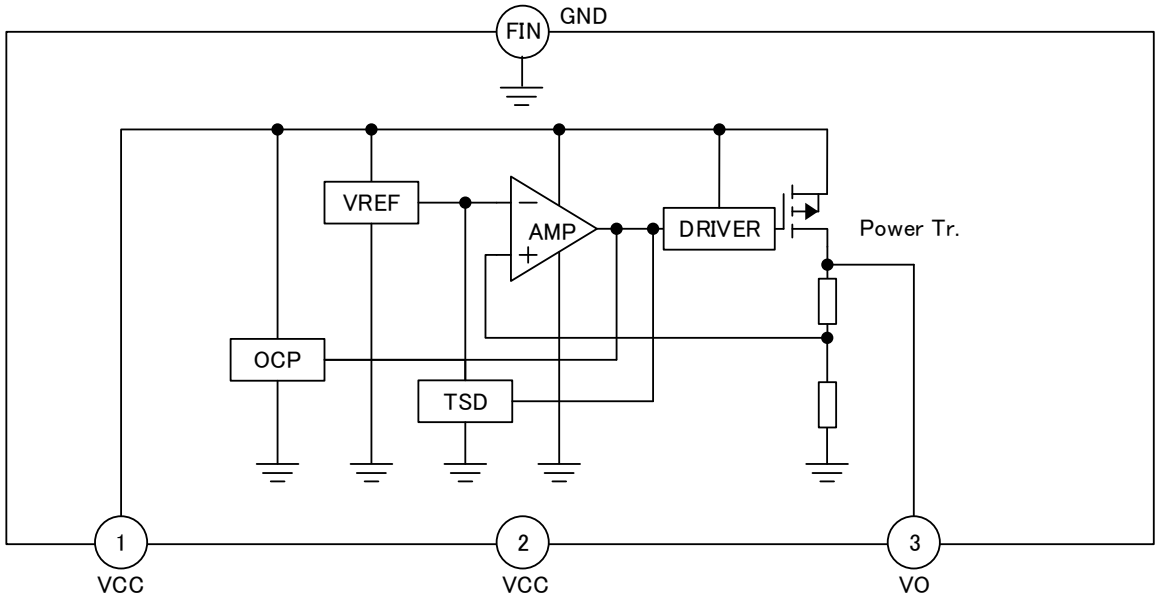


Pin Descriptions

Pin No.	Pin Name	Function
1	VCC	Power Supply Pin
2	VCC*(Note 1)*	Pin 2 is connected to Pin 1 inside
3	VO	Output Pin
FIN	GND	GND Pin

(Note 1) the connection at the outside is unnecessary.

Block Diagram



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Description of Blocks

Block Name	Function	Description of Blocks
TSD	Thermal Shutdown Protection	In case maximum power dissipation is exceeded or the ambient temperature is higher than the Maximum Junction Temperature, overheating causes the chip temperature (Tj) to rise. The TSD protection circuit detects this and forces the output to turn off in order to protect the device from overheating.
VREF	Reference Voltage	Generate the Reference Voltage
AMP	Error Amplifier	The Error Amplifier amplifies the difference between the internal voltage reference(VREF) and the sensed feedback voltage from the output, and regulates the output MOS-FET(Power Tr.) via the DRIVER.
DRIVER	Output MOS-FET Driver	Drive the Output MOS-FET (Power Tr.)
OCP	Over Current Protection	If the output current increases higher than the maximum Output Current, the output current is limited in order to protect the device from damage caused by over current.

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Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply Voltage*(Note 1)*	V_{CC}	-0.3 to +35.0	V
Output Voltage	V_O	-0.3 to +16.0	V
Operating Ambient Temperature Range	Ta	-40 to +125	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	+150	°C

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution 2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB boards with thermal resistance and power dissipation taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

(Note 1) Do not exceed Tjmax.

Thermal Resistance*(Note 1)*

Parameter	Symbol	Thermal Resistance(Typ)		Unit
		1s*(Note 3)*	2s2p*(Note 4)*	
TO252S-3				
Junction to Ambient	θ_{JA}	155.4	24.3	°C/W
Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT}	8	3	°C/W

(Note 1) Based on JESD51-2A(Still-Air)

(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 3) Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

(Note 4) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size	Thermal Via*(Note 5)*	
			Pitch	Diameter
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt	1.20mm	Φ0.30mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

(Note 5) This thermal via connects with the copper pattern of all layers.

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Operating Conditions(-40°C ≤ Ta ≤ +125°C)

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	9.0	26.5	V
Startup Voltage (Io = 0 mA)	V_{CC}	3.8	-	V
Output Current	I_O	0	1.0	A
Input Capacitor	C_{IN}	1.0	-	μF
Output Capacitor	C_O	1.0	1000	μF
Output Capacitor Equivalent Series Resistance	ESR(C_O)	-	20	Ω

Electrical Characteristics

Unless otherwise specified, -40 °C ≤ Ta ≤ +125 °C, V_{CC} = 13.5 V, I_O = 0 mA

Paremeter	Symbol	Guaranteed Limit			Unit	Conditions
		Min	Typ	Max		
Circuit Current	Ib	-	0.6	2.5	mA	
Output Voltage	V_O	7.92	8.00	8.08	V	I_O = 500 mA, Ta = +25 °C
		7.76	8.00	8.24	V	I_O = 500 mA
Dropout Voltage	ΔVd	-	0.3	0.5	V	V_{CC} = 7.6V, I_O = 500 mA
Ripple Rejection	R.R.	40	50	-	dB	f = 120 Hz, ein = 1 Vrms, I_O = 100 mA
Line Regulation	Reg.I	-	20	80	mV	9.0 V ≤ V_{CC} ≤ 26.5 V
Load Regulation	Reg.L	-	V_O × 0.010	V_O × 0.020	V	5 mA ≤ I_O ≤1 A

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Typical Performance Curves

Unless otherwise specified, -40°C ≤ Ta ≤ +125°C, V_{CC}=13.5V, I_O=0mA

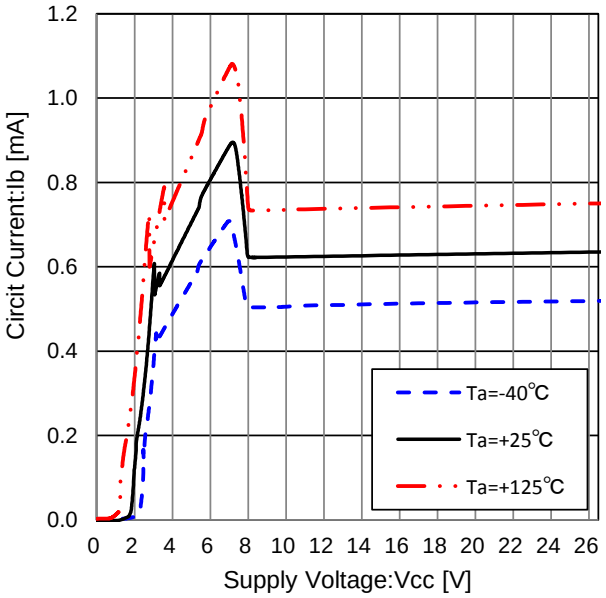

Figure 1. Circuit Current vs Supply Voltage

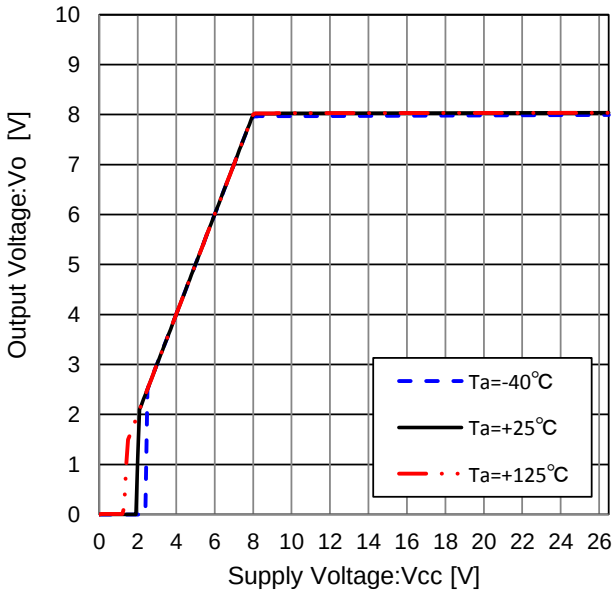

Figure 2. Output Voltage vs Supply voltage
(Io=0mA)

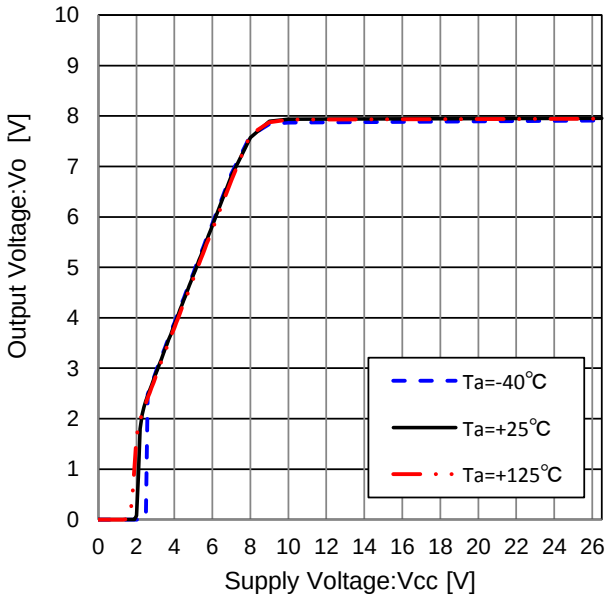

Figure 3. Output Voltage vs Supply voltage
(Io=500mA)

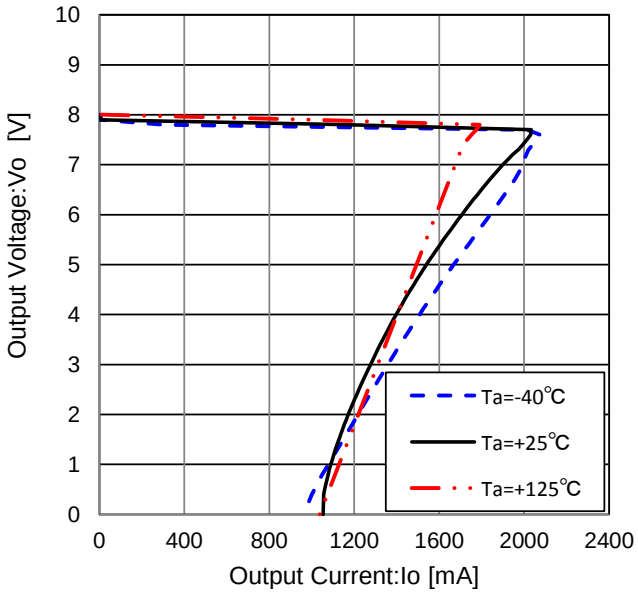

Figure 4. Output Voltage vs Output Current
(OCP characteristic)

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Typical Performance Curves - continued

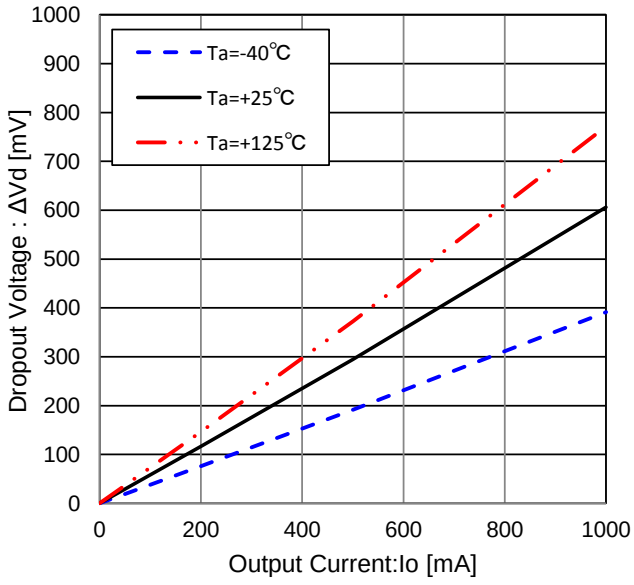

Figure 5. Dropout Voltage
(V_{CC}=V_O×0.95V=7.6V)

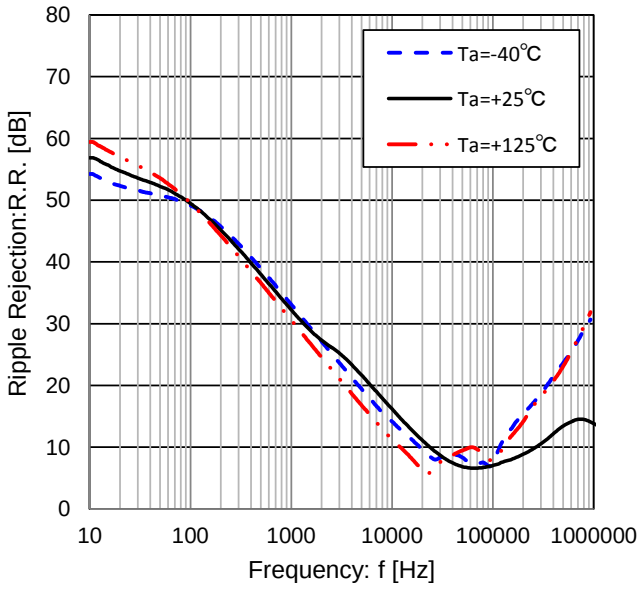

Figure 6. Ripple Rejection
(ein=1Vrms, I_O=100mA)

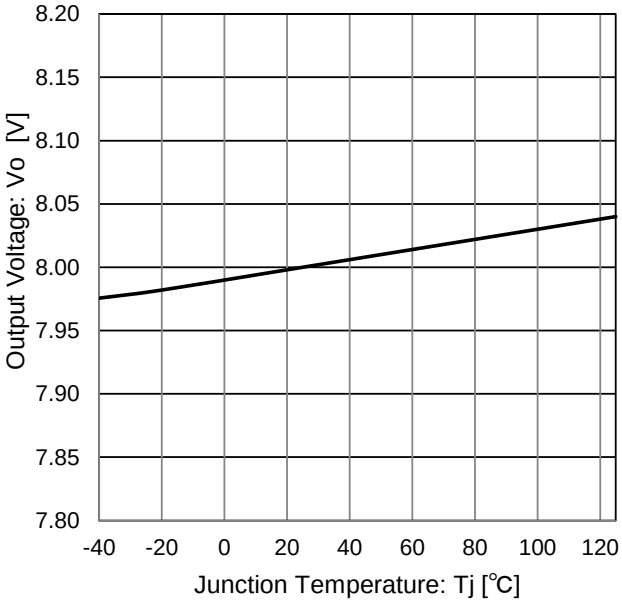

Figure 7. Output Voltage vs Junction Temperature

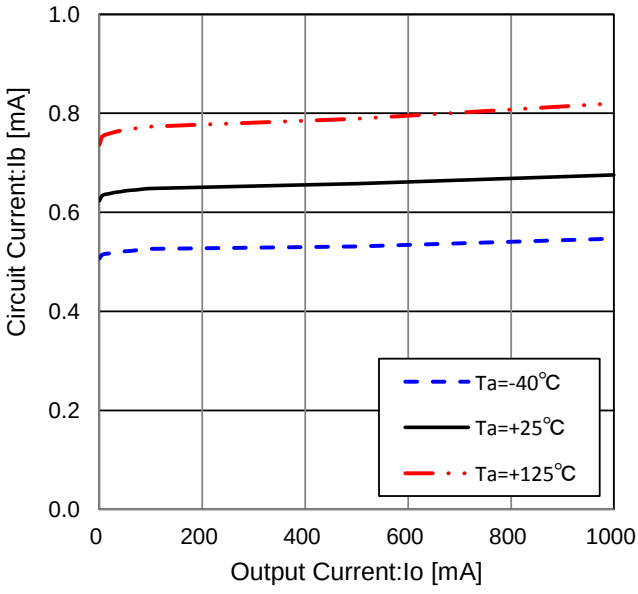

Figure 8. Circuit Current vs Output Current

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Typical Performance Curves - continued

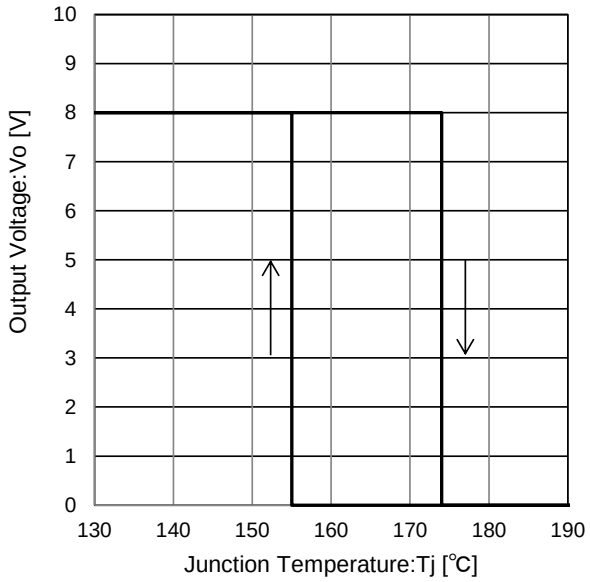

Figure 9. Output Voltage vs Junction Temperature
(Thermal Shutdown Circuit Characteristic)

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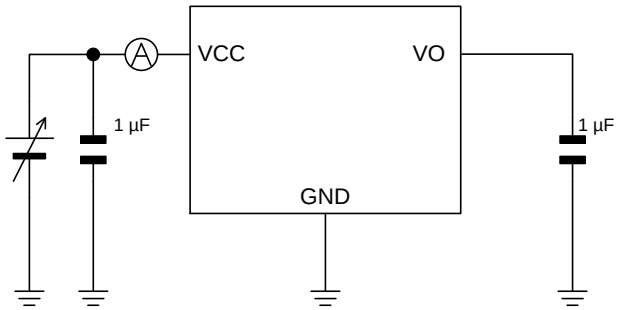
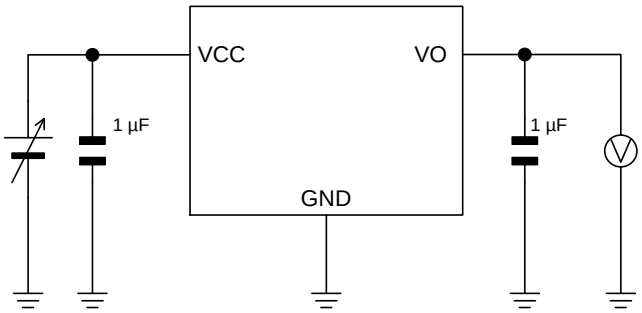
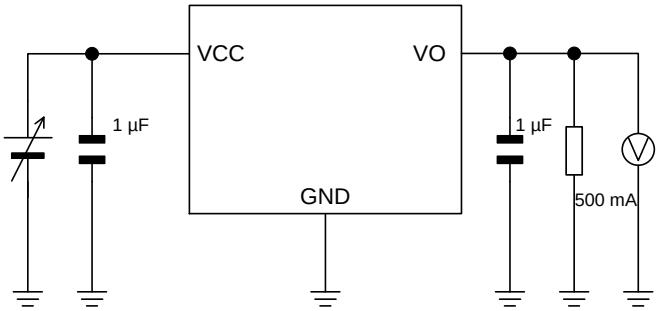
Measurement Circuit for Typical Performance Curves



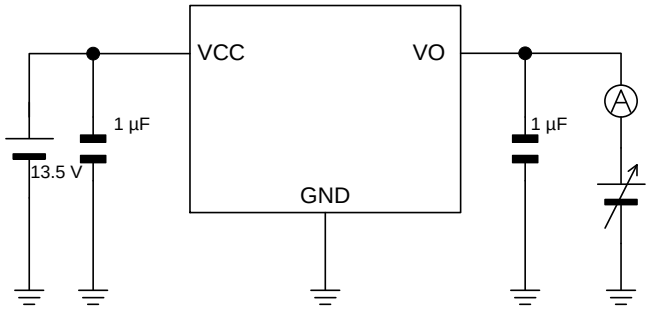
Measurement Setup
for Figure 1



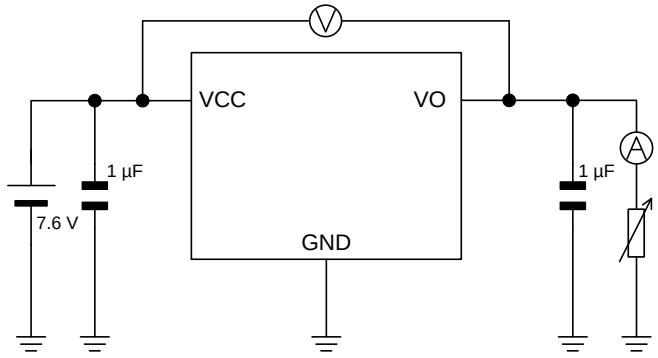
Measurement Setup
for Figure 2



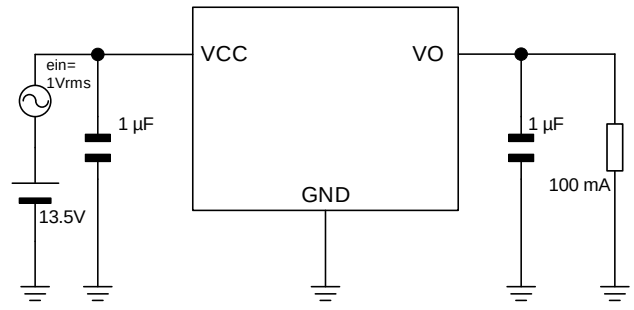
Measurement Setup
for Figure 3



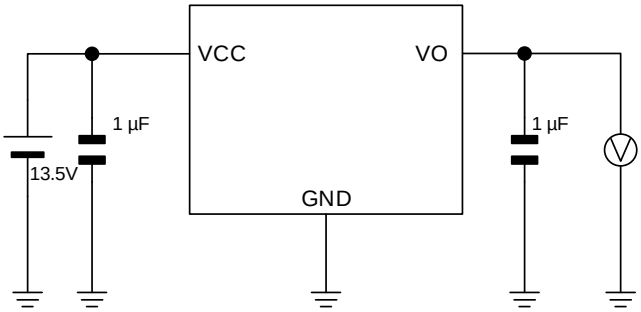
Measurement Setup
for Figure 4



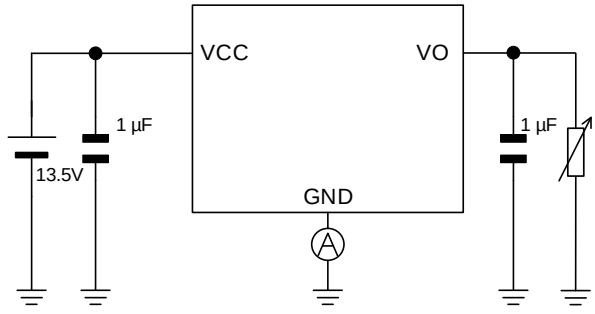
Measurement Setup
for Figure 5



Measurement Setup
for Figure 6



Measurement Setup
for Figure 7, 9



Measurement Setup
for Figure 8

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Application and Implementation

Notice: The following information is provided only as reference for application and implementation, and does not guarantee its operation on specific function, accuracy or the external components in the application. On application, after a thorough confirmation such as of characteristics of the capacitor, conduct the appropriate verification necessary in the actual application and design with sufficient margin.

Selection of External Components

Input Pin Capacitor

Inserting capacitors with a capacitance of 1 μF or higher between the VCC and GND pin is necessary and can realize stable IC operation. We recommend using ceramic capacitor generally featuring good high frequency characteristic. When selecting a ceramic capacitor, please consider about temperature and DC-biasing characteristics. Place capacitors as close as possible between the VCC and GND pin.

When input impedance is high, e.g. in case there is distance from battery, line voltage drop needs to be prevented by large capacitor. Choose the capacitance according to the line impedance between the power smoothing circuit and the VCC pin. Selection of the capacitance also depends on the applications. Verify the application and allow sufficient margins in the design.

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Application and Implementation - continued

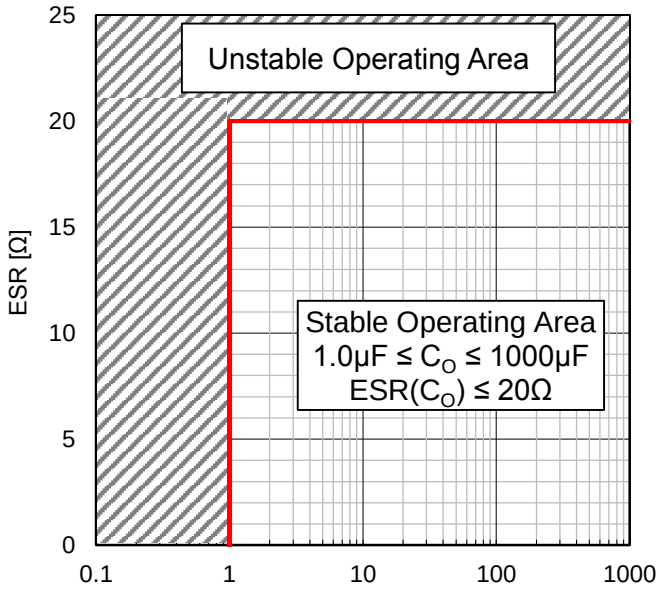
Output Pin Capacitor

In order to prevent oscillation, a capacitor needs to be placed between the VO and GND pin. It is necessary to use a capacitor with a capacitance of 1µF (Min) or higher. Electrolytic, tantalum and ceramic capacitors can be used. When selecting the capacitor ensure that the capacitance of 1µF or higher is maintained at the intended applied voltage and temperature range. Due to changes in temperature the capacitor's capacitance can fluctuate possibly resulting in oscillation.

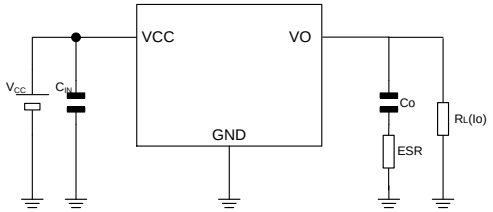
For selection of the capacitor refer to the graph. As described in the graph, this product is designed to achieve stable and regulated operation with capacitance value from 1µF to 1000µF and with ESR value within approximately 0Ω to 20Ω.The stable operating range in the graph is given by the measurement data with a standalone IC and resistive load. For actual applications the stable operating range is influenced by the PCB impedance, input supply impedance and load impedance. Therefore the electrostatic capacity and other characteristics should be dimensioned in accordance and should be verified in the real application and the final operating environment that the output stability requirements are fulfilled.

When selecting a ceramic type capacitor, we recommend using X5R, X7R or better with excellent temperature and DC-biasing characteristics and high voltage tolerance.

Also, in case of rapidly fluctuation of input voltage and load current, select the capacitance in accordance with verifying that the actual application meets with the required specification. Place capacitors as close as possible the VO pin.



ESR vs Output Capacitance C_O,Stable Available Area
(-40°C ≤ Ta ≤ +125 °C, 9V ≤ V_{CC} ≤ 35V, I_O = 0mA to 1A)



Measurement Circuit Figure

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Application and Implementation - continued

Linear Regulators Surge Voltage Protection

The following provides instructions on surge voltage exceeding absolute maximum ratings polarity protection for ICs.

Positive surge to the input

If there is any potential risk that positive surges higher than absolute maximum ratings 35V will be applied to the input, a Zener Diode should be inserted between the VCC and the GND to protect the device as shown in the Figure 10.

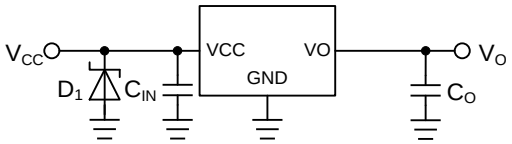

Figure 10. Surges Higher than 35V will be Applied to the Input

Negative surge to the input

If there is any potential risk that negative surges below the absolute maximum ratings -0.3V will be applied to the input, a Schottky Diode should be inserted between the VCC and the GND to protect the device as shown in the Figure 11.

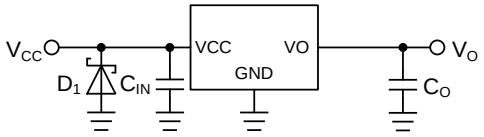

Figure 11. Surges Lower than -0.3 V will be Applied to the Input

Linear Regulators Reverse Voltage Protection

A linear regulator integrated circuit (IC) requires that the input voltage to be always higher than the output voltage. Output voltage, however, may become higher than the input voltage under specific situations or circuit configurations. In such circumstances reverse voltage and current may cause damage to the IC. A reverse polarity connection of power supply or certain inductor components can also cause a polarity reversal between the input and output pins. The following provides instructions on reversed voltage polarity protection for ICs.

Reverse Input /Output Voltage

In MOS type linear regulator, a parasitic body diode exists in the drain-source junction region of its internal power MOS-FET. Reverse input/output voltage triggers the reverse current flow from the output to the input through the body diode. The inverted current may damage or destroy the semiconductor elements of the regulator since the effect of the parasitic body diode is usually disregarded for the regulator behavior (see Figure 12).

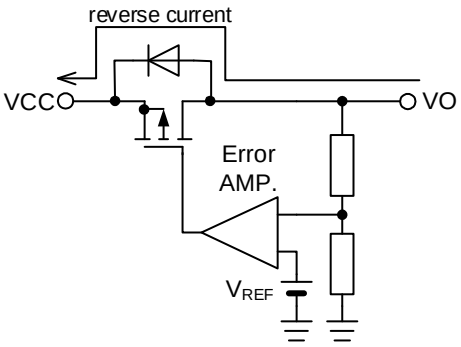

Figure 12. Reverse Current Path in an MOS Linear Regulator

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Application and Implementation – continued

An effective solution to this is an external bypass diode connected between the input and output to prevent the reverse current flow inside the IC (see Figure 13). Note that the bypass diode must be turned on prior to the IC's internal circuit. Bypass diodes in the internal circuits of MOS linear regulators must have low forward voltage V_F. Some ICs are configured with current-limit thresholds to shutdown high reverse current. However even when the output is off, if reverse leakage current of bypass diode is high, leakage current flow from the input to the output; therefore, it is necessary to choose diode with small reverse current. Specifically, select a diode with a rated peak reverse voltage greater than the input to output voltage differential and with rated forward current greater than the reverse current in actual application.

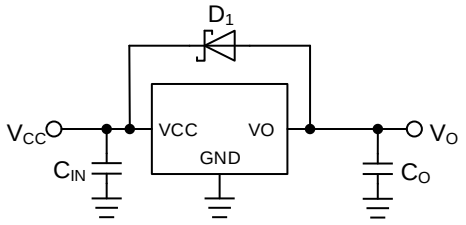

Figure 13. Bypass Diode for Reverse Current Diversion

The lower forward voltage (V_F) of Schottky barrier diodes cater to requirements of MOS linear regulators, however the main drawback is in their relatively high reverse current (I_R). In case of selecting Schottky barrier diodes, it is recommended to select product with low reverse current. The V_R-I_R characteristics have positive temperatures characteristic, which the details shall be checked with the datasheet of the products.

Even in case input/output voltage is inverted, if V_{CC} is open circuit as shown in the following Figure 14, the only current that flows in the reverse current path is the bias current of the IC. In this case a reverse current bypass diode is not required as the amperage is too low to damage or deteriorate the parasitic element.

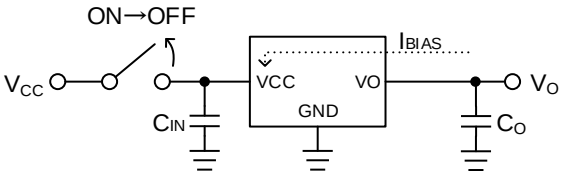

Figure 14. Open V_{CC}

Protection against Input Reverse Voltage

Accidental reverse polarity at the input connection applies a large current to the ESD protection diode for between the input pin of the IC and the GND pin, which may destroy the IC (see Figure 15).

A Schottky barrier diode or rectifier diode connected in series to the power supply as shown in Figure 16 is the simplest solution to prevent this from happening. The solution, however, is unsuitable for a circuit powered by batteries because there is a power loss calculated as $V_F \times I_O$, as the forward voltage V_F of the diode drops forward direction connection. The lower V_F of a Schottky barrier diode contributes to rather smaller power loss than rectifier diodes. Because diodes generate heat select diode with enough margin in power dissipation. At reverse connection diode allows a reverse current however for negligible amount.

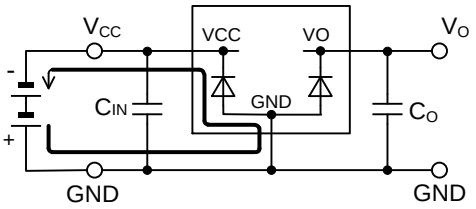

Figure 15. Current Path in Reverse Input Connection

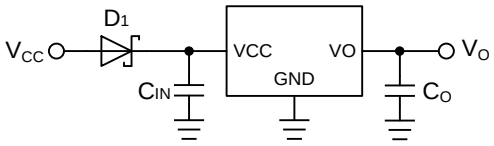

Figure 16. Protection against Reverse Polarity 1

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Application and Implementation - continued

Figure 17 shows a circuit in which a P-channel MOS-FET is connected in series to the power. The body diodeQ_1 (parasitic element) is located in the drain-source junction area of the MOS-FET. The voltage drop in a forward connection is calculated from the on state resistance of the MOS-FET times the output current I_O. Therefore it is smaller than the voltage drop by the diode (see Figure 17) and results in less of a power loss. No current flows in a reverse connection where the MOS-FET remains off such as Figure 17.

If the gate-source voltage exceeds max rating of MOS-FET gate-source junction with derating curve in consideration, reduce the gate-source junction voltage by connecting resistor voltage divider as shown in Figure 18.

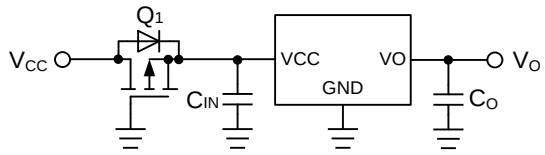

Figure 17. Protection against Reverse Polarity 2

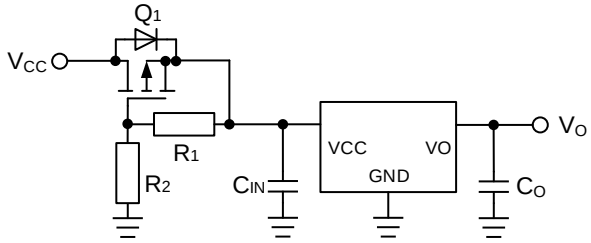

Figure 18. Protection against Reverse Polarity 3

Protection against Reverse Output Voltage when Output Connect to an Inductor

If the output load is inductive, electrical energy accumulated in the inductive load is released to the ground when the output voltage is turned off. IC integrates ESD protection diodes between the IC output and ground pins, which a large current may flows in such condition finally resulting on destruction of the IC. To prevent this situation, connect a Schottky barrier diode in parallel to the diode (see Figure 19).

Further, if a long wire is in use for the connection between the output pin of the IC and the load, observe the waveform on an oscilloscope, since it is possible that the load becomes inductive. An additional diode is required for a motor load that is affected by its counter electromotive force, as it produces an electrical current in a similar way.

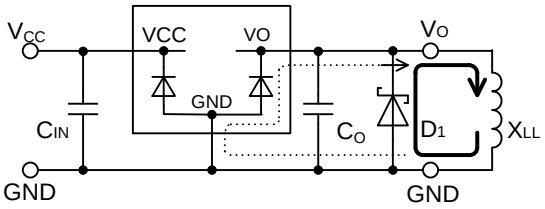

Figure 19. Current Path in Inductive Load (Output: Off)

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Power Dissipation

TO252S-3

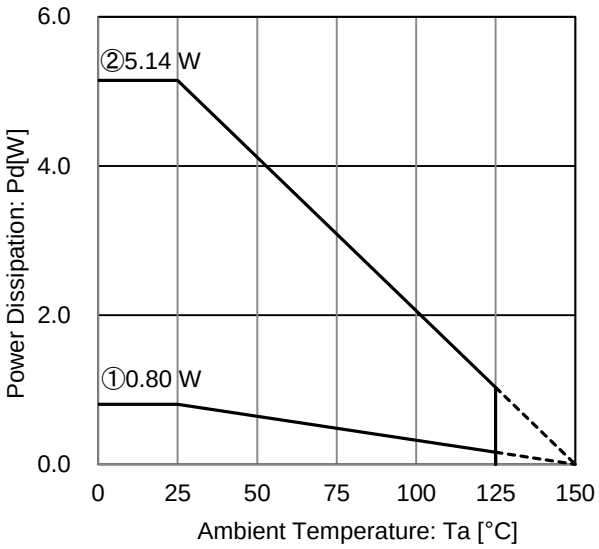

Figure 20. Power Dissipation (TO252S-3)

IC mounted on ROHM standard board based on JEDEC.
1 : 1-layer PCB
(Copper foil area on the reverse side of PCB: 0mm × 0mm)
Board material: FR4
Board size: 114.3mm × 76.2mm × 1.57mmt
Mount condition: PCB and exposed pad are soldered.
Top copper foil: ROHM recommended footprint
+ wiring to measure, 2 oz. copper.

2 : 4-layer PCB
(Copper foil area on the reverse side of PCB: 74.2mm × 74.2mm)
Board material: FR4
Board size: 114.3mm × 76.2mm × 1.60mmt
Mount condition: PCB and exposed pad are soldered.
Top copper foil: ROHM recommended footprint
+ wiring to measure, 2 oz. copper.
2 inner layers copper foil area of PCB:
74.2mm × 74.2mm, 1 oz. copper.
Copper foil area on the reverse side of PCB:
74.2mm × 74.2mm, 2 oz. copper.

Condition 1 : θ_{JA} = 155.4°C/W, Ψ_{JT} (top center) = 8°C/W
Condition 2 : θ_{JA} = 24.3°C/W, Ψ_{JT} (top center) = 3°C/W

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Thermal Design

This product exposes a frame on the back side of the package for thermal efficiency improvement. The power consumption of the IC is decided by the dropout voltage condition, the load current and the circuit current. Refer to power dissipation curves illustrated in Figure 20 when using the IC in an environment of Ta ≥ +25°C. Even if the ambient temperature Ta is at +25°C, depending on the input voltage and the load current, chip junction temperature can be very high. Consider the design to be Tj ≤ Tjmax = +150°C in all possible operating temperature range.
Should by any condition the maximum junction temperature Tjmax = +150°C rating be exceeded by the temperature increase of the chip, it may result in deterioration of the properties of the chip. The thermal impedance in this specification is based on recommended PCB and measurement condition by JEDEC standard. Verify the application and allow sufficient margins in the thermal design by the following method to calculate the junction temperature Tj. Tj can be calculated by either of the two following methods.

1. The following method is used to calculate the junction temperature Tj with ambient temperature Ta.

$$Tj = Ta + P_C \times \theta_{JA}$$

Where:
- Tj is the Junction Temperature
- Ta is the Ambient Temperature
- P_C is the Power Consumption
- θ_{JA} is the Thermal Resistance (Junction to Ambient)

2. The following method is also used to calculate the junction temperature Tj with top center of case's (mold) temperature T_T.

$$Tj = T_T + P_C \times \Psi_{JT}$$

Where:
- Tj is the Junction Temperature
- T_T is the Top Center of Case's (mold) Temperature
- P_C is the Power consumption
- Ψ_{JT} is the Thermal Resistance (Junction to Top Center of Case)

3. The following method is used to calculate the power consumption Pc (W).

$$Pc = (V_{CC} - V_O) \times I_O + V_{CC} \times Ib$$

Where:
- P_C is the Power Consumption
- V_{CC} is the Input Voltage
- V_O is the Output Voltage
- I_O is the Load Current
- Ib is the Quiescent Current

Calculation Example (TO252S-3)
If V_{CC} = 13.5V, V_O = 8.0V, I_O = 500mA, Ib = 0.65mA, the power consumption Pc can be calculated as follows:

$$\begin{aligned} P_C &= (V_{CC} - V_O) \times I_O + V_{CC} \times Ib \\ &= (13.5V - 8.0V) \times 500mA + 13.5V \times 0.65mA \\ &= 2.759W \end{aligned}$$

At the ambient temperature Ta = +80°C, the thermal impedance (Junction to Ambient) θ_{JA} = 23.0 °C / W(4-layer PCB)

$$\begin{aligned} Tj &= Ta + P_C \times \theta_{JA} \\ &= 80°C + 2.759W \times 24.3°C / W \\ &= 147.0°C \end{aligned}$$

When operating the IC, the top center of case's (mold) temperature T_T = +100°C, Ψ_{JT} = 3°C / W(4-layer PCB)

$$\begin{aligned} Tj &= T_T + P_C \times \Psi_{JT} \\ &= 100°C + 2.759W \times 3°C / W \\ &= 108.3°C \end{aligned}$$

For optimum thermal performance, it is recommended to expand the copper foil area of the board, increasing the layer and thermal via between thermal land pads.

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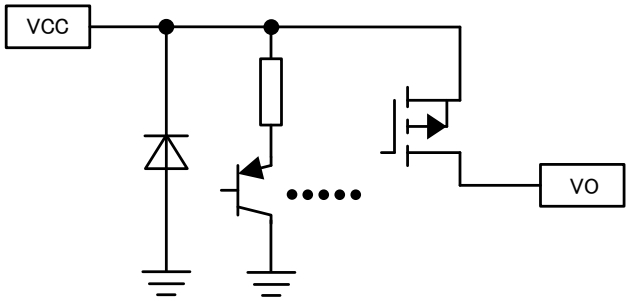
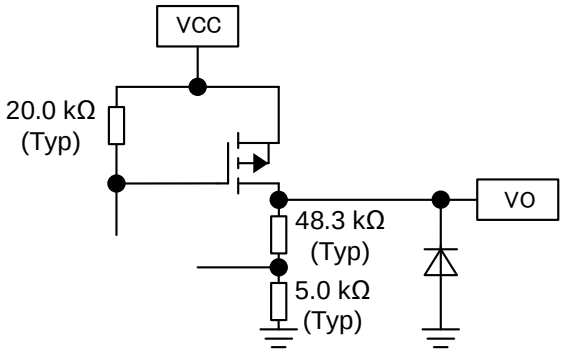
I/O Equivalence Circuit

VCC

VO


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Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Thermal Consideration

The power dissipation under actual operating conditions should be taken into consideration and a sufficient margin should be allowed in the thermal design. On the reverse side of the package this product has an exposed heat pad for improving the heat dissipation. The amount of heat generation depends on the voltage difference between the input and output, load current, and bias current. Therefore, when actually using the chip, ensure that the generated heat does not exceed the Pd rating.

If Junction temperature is over Tjmax (=+150°C), IC characteristics may be worse due to rising chip temperature. Heat resistance in specification is measurement under PCB condition and environment recommended in JEDEC. Ensure that heat resistance in specification is different from actual environment.

8. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

9. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

10. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

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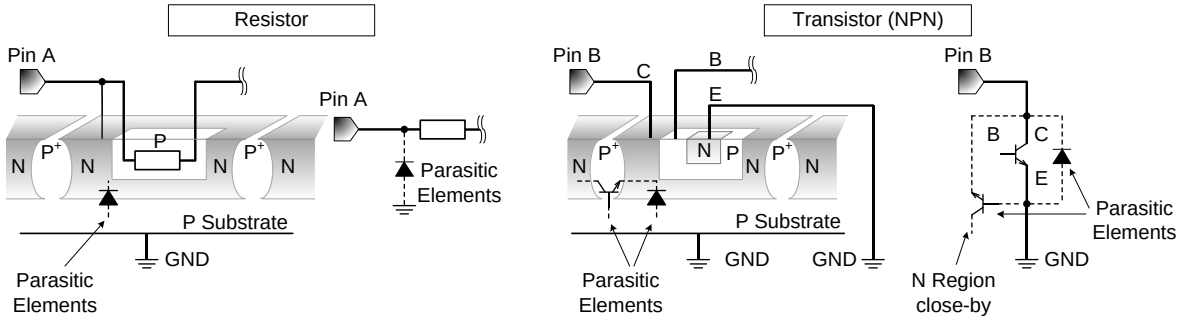
Operational Notes – continued

11. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.



12. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

13. Thermal Shutdown Protection Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

14. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

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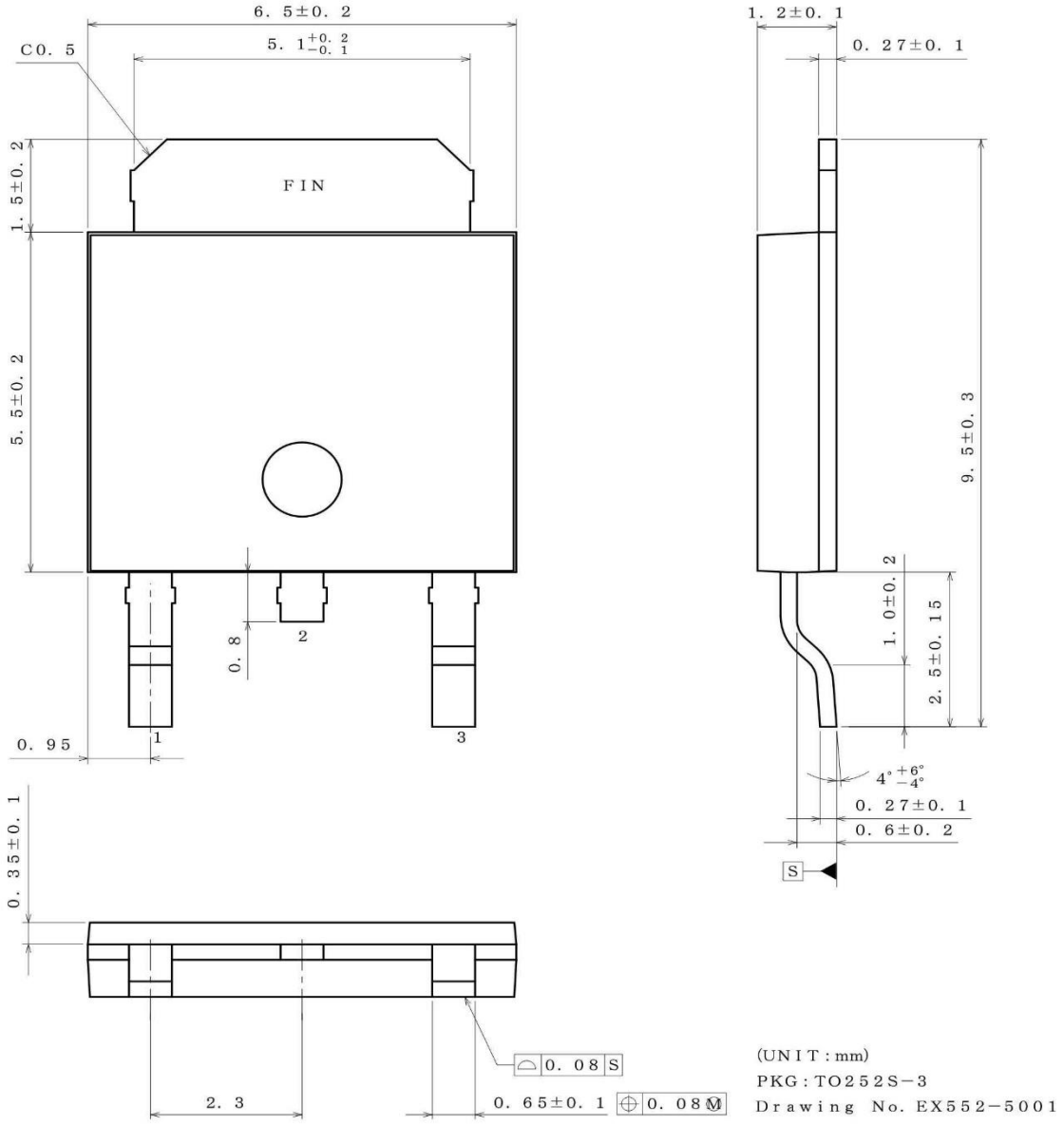
Physical Dimension and Packing Information

Package Name	TO252S-3



< Tape and Reel Information >

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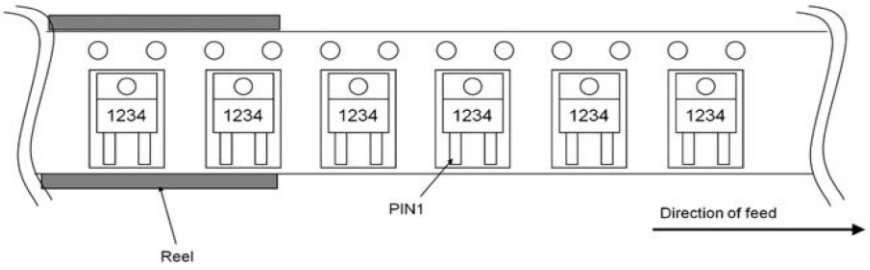
Quantity	2000pcs
Direction of feed	E2



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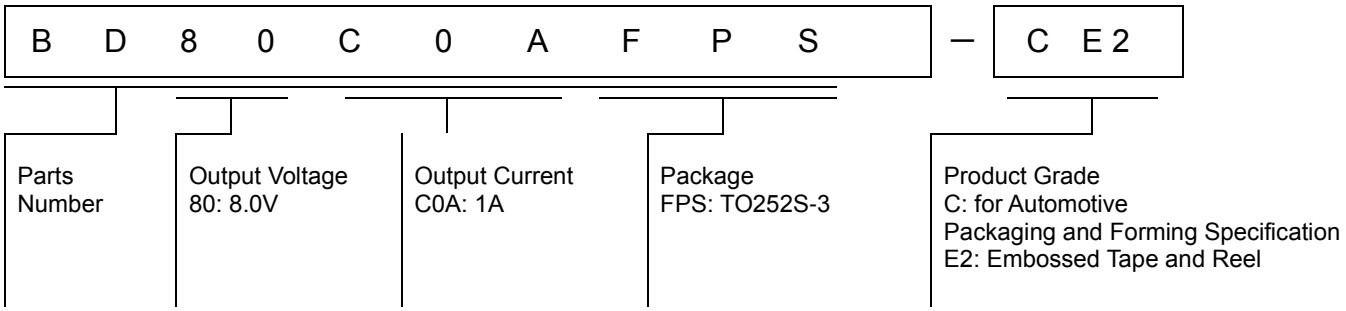
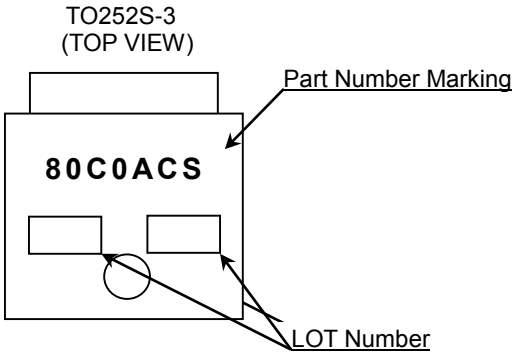
Ordering Information



Marking Diagram



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Revision History

Date	Revision	Changes
22.Dec.2017	001	New Release

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CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

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5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
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2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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