Single-Output LDO Regulators

35V Voltage Resistance 2A LDO Regulators

BDxxFD0 series

Description

The BDxxFD0 series are low-saturation regulators. The series' output voltages are Variable, and fixed type. These series have a built-in over-current protection circuit that prevents the destruction of the IC due to output short circuits and a thermal shutdown circuit that protects the IC from thermal damage due to overloading.

Features

- Output current capability: 2A
- Output voltage: Variable, Fixed (1.5V / 1.8V / 2.5V / 3.0V / 3.3V / 5.0V / 8.0V / 9.0V / 12V / 15V / 16V)
- ±1% (±1.5%:BD15/18/25FD0W) High output voltage accuracy (Ta=25°C)
- Low saturation with PDMOS output
- Built-in over-current protection circuit that prevents the destruction of the IC due to output short circuits
- Built-in thermal Shutdown circuit for protecting the IC from thermal damage due to overloading
- Low ESR Capacitor
- HRP5/TO263-5 package

Packages

W(Typ) x D(Typ) x H(Max)

HRP5 9.395mm x 10.540mm x 2.005mm



TO263-5 10.16mm×15.10mm×4.70mm



Key Specifications

- Supply Voltage(Vo ≥ 3.0V): Vo+1.0V to 32.0V
- Supply Voltage(Vo < 3.0V): 4.0V to 32.0V
- Output Voltage(BD00FD0W): 1.5V to 16.0V
- Output Current: 2A
- Output Voltage Precision(Note 1): ±1%(Ta=25°C)
- Operating Temperature Range: -40°C to +105°C

(Note 1) BD15/18/25FD0W are ±1.5% (Ta=25°C)

Applications

General Purpose

Ordering Part Number

B	D	x	x	F	D	0	W	x	x	x	-	x	x

Output voltage
00: Variable
15:1.5V
18:1.8V
25:2.5V
30:3.0V
33:3.3V
50:5.0V
80:8.0V
90:9.0V
J2:12.0V
J5:15.0V
J6:16.0V

Input Voltage, Current capacity
FD0: 35V, 2A

Enable
W: With CTL(Enable)

Package
HFP: HRP5
FP2: TO263-5

Packaging and forming specification
TR: Embossed tape and reel(HRP5)
E2: Embossed tape and reel(TO263-5)

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Lineup

Ordering Part Number	Output Voltage	Package
BD00FD0WHFP-TR	Variable	HRP5 2000pcs/Reel
BD15FD0WHFP-TR	1.5V	
BD18FD0WHFP-TR	1.8V	
BD25FD0WHFP-TR	2.5V	
BD30FD0WHFP-TR	3.0V	
BD33FD0WHFP-TR	3.3V	
BD50FD0WHFP-TR	5.0V	
BD80FD0WHFP-TR	8.0V	
BD90FD0WHFP-TR	9.0V	
BDJ2FD0WHFP-TR	12V	
BDJ5FD0WHFP-TR	15V	
BDJ6FD0WHFP-TR	16V	

Ordering Part Number	Output Voltage	Package
BD00FD0WFP2-E2	Variable	TO263-5 500pcs/Reel
BD15FD0WFP2-E2	1.5V	
BD18FD0WFP2-E2	1.8V	
BD25FD0WFP2-E2	2.5V	
BD30FD0WFP2-E2	3.0V	
BD33FD0WFP2-E2	3.3V	
BD50FD0WFP2-E2	5.0V	
BD80FD0WFP2-E2	8.0V	
BD90FD0WFP2-E2	9.0V	
BDJ2FD0WFP2-E2	12V	
BDJ5FD0WFP2-E2	15V	
BDJ6FD0WFP2-E2	16V	

Typical Application Circuits

<Output Voltage Variable Type>

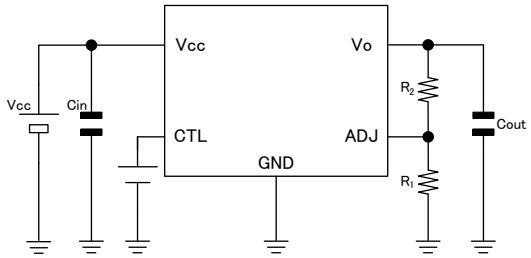


Figure 1. Typical Application Circuit
Output Voltage Variable Type

<Output Voltage Fixation Type>

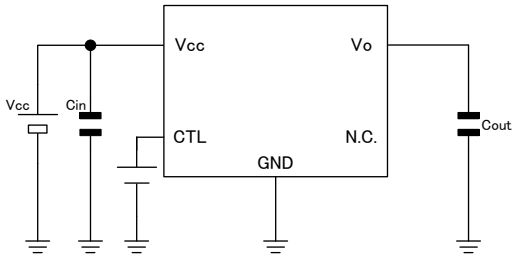


Figure 2. Typical Application Circuit
Output Voltage Fixation Type

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Pin Configurations/Pin Descriptions

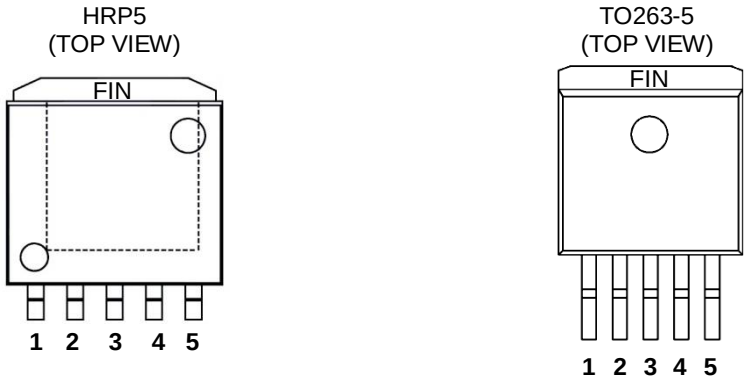


Figure 3. Pin Configurations

Variable output voltage type

Pin No	Terminal Name	Function
1	CTL	Control terminal By setting this pin to High, you can turn the device on. By setting this pin to Low, you can turn the device off.
2	Vcc	Input Power source terminal Connect a ceramic capacitor between Vcc and GND. Place the capacitor close to the terminal.
3	GND	Ground It is connected to the FIN terminal at the ground of the circuit.
4	Vo	Output terminal Connect a capacitor between Vo and GND. Place the capacitor close to the terminal. Refer to Operational Notes 15 for capacitance and ESR value.
5	ADJ	Output voltage setting terminal Connect a resistor between Vo and ADJ,ADJ and GND.
FIN	FIN	Heat dissipating FIN It is recommended that FIN is soldered to a copper foil part with a large area. It is electrically connected to GND inside the package.

Fixed output voltage type

Pin No	Terminal Name	Function
1	CTL	Control terminal By setting this pin to High, you can turn the device on. By setting this pin to Low, you can turn the device off.
2	Vcc	Input Power source terminal Connect a ceramic capacitor between Vcc and GND. Place the capacitor close to the terminal.
3	GND	Ground It is connected to the FIN terminal at the ground of the circuit.
4	Vo	Output terminal Connect a capacitor between Vo and GND. Place the capacitor close to the terminal. Refer to Operational Notes 15 for capacitance and ESR value.
5	N.C.	Unused terminal Connect to open or GND.
FIN	FIN	Heat dissipating FIN It is recommended that FIN is soldered to a copper foil part with a large area. It is electrically connected to GND inside the package.

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Block diagrams

< BD00FD0WHFP/FP2 (Output Voltage Variable Type) >

■HRP5/TO263-5

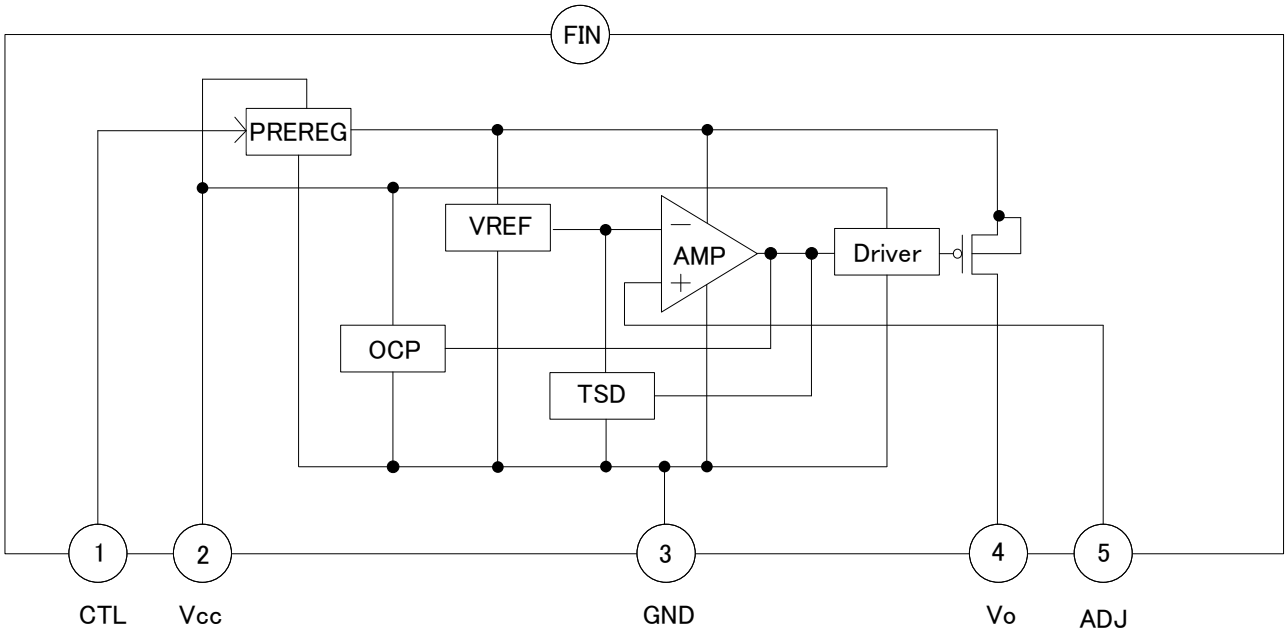


Figure 4. Block diagram
BD00FD0WHFP/FP2 (Output Voltage Variable Type)

< BDxxFD0WHFP/FP2 (Output Voltage Fixation Type) >

■HRP5/TO263-5

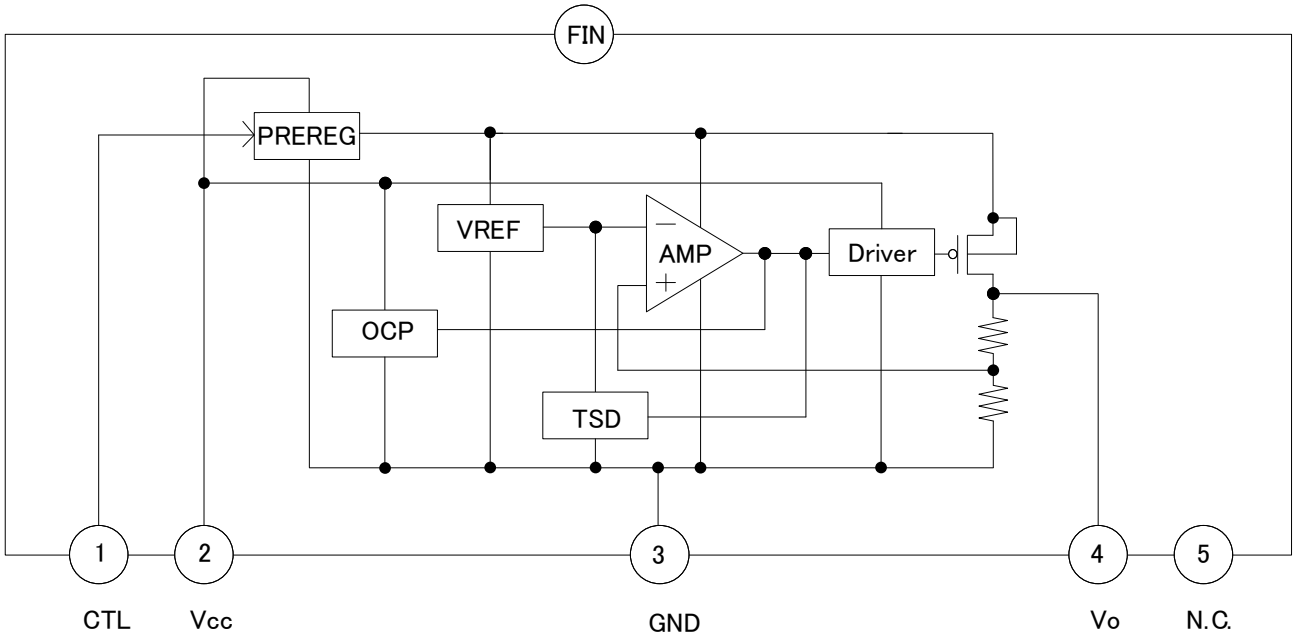


Figure 5. Block diagram
BDxxFD0WHFP/FP2(Output Voltage Fixation Type)

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Description of Blocks

Block Name	Function	Description of Blocks
PREREG	Internal Power Supply	A logical “High” (V_{thH} ≥ 2.0 V) at the CTL enables Power Supply for Internal Circuit
TSD	Thermal Shutdown Protection	To protect the device from overheating. If the chip temperature (Tj) reaches ca. 175 °C (Typ), the output is turned off.
VREF	Reference Voltage	Generate the Reference Voltage
AMP	Error Amplifier	The Error Amplifier amplifies the difference between the feed back voltage of the output voltage and the reference v.
Driver	Output MOS FET Driver	Drive the Output MOS FET
OCP	Over Current Protection	To protect the device from damage caused by over current. If the output current reaches current ability (Typ : 2500mA), the output is turned off.

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Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply Voltage (Note 1)	Vcc	-0.3 to +35.0	V
Output Control Voltage (Note 2)	V_{CTL}	-0.3 to +35.0	V
Operating Temperature Range	Ta	-40 to +105	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	150	°C

(Note 1) Do not exceed Tjmax.
(Note 2) The order of starting up power supply (Vcc) and CTL pin doesn't have either in the problem within the range of the operation power-supply voltage ahead.
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (-40°C ≤ Ta ≤ +105°C)

Parameter	Symbol	Min	Max.	Unit
Supply Voltage (Vo ≥ 3.3V)	Vcc	Vo+1	32.0	V
Supply Voltage (Vo ≤ 3.0V)	Vcc	4.0	32.0	V
Startup Voltage (Io=0mA)	Vcc	-	3.8	V
Output Control Voltage	V_{CTL}	0	32.0	V
Output Current	Io	0	2.0	A
Output Voltage (BD00FD0W) (Note 3)	Vo	1.5	18.0	V

(Note 3) Refer to Notes15 for use when you use BD00FD0W by output voltage 1.5V ≤ Vo < 3.0V.

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Electrical Characteristics

Unless otherwise specified, Ta=25°C, Vcc= 13.5V(Note 1), Io=0mA, V_{CTL}=5.0V
The resistor of between ADJ and Vo =56.7kΩ, ADJ and GND =10kΩ (BD00FD0W)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Shutdown Current	Isd	-	0	10	μA	V_{CTL}=0V, Vcc<10V
Circuit Current	Ib	-	0.5	1.0	mA	
ADJ Terminal Voltage (BD00FD0W)	VADJ	0.742	0.750	0.758	V	Io=500mA, Vcc=13.5V
Output Voltage (BD15/18/25FD0W)	Vo	Vo × 0.985	Vo	Vo × 1.015	V	Io=500mA Vo ≤ 2.5V
Output Voltage (BD30 to J6FD0W) (Note 2)	Vo	Vo × 0.99	Vo	Vo × 1.01	V	Io=500mA Vo ≥ 3.0V
Dropout Voltage	ΔVd	-	0.40	0.55	V	Vcc=Vo×0.95, Io=1A, Vo ≥ 5.0V
Ripple Rejection (BD00 to 50FD0W) (Note 3)	R.R.	45	55	-	dB	f=120Hz, Input Voltage Ripple =1Vrms, Io=500mA
Ripple Rejection (BD80 to J6FD0W) (Note 4)	R.R.	40	50	-	dB	f=120Hz, Input Voltage Ripple =1Vrms, Io=500mA
Line Regulation (Note 5)	Reg.I	-	20	80	mV	Vo+1.0V ≤ Vcc ≤ 26.5V Vo ≥ 3.3V
Line Regulation (Note 6)	Reg.I	-	20	80	mV	4.0V ≤ Vcc ≤ 26.5V Vo ≤ 3.0V
Load Regulation (Note 5)	Reg.L	-	Vo × 0.007	Vo × 0.014	V	5mA ≤ Io ≤ 1A Vo ≥ 3.3V
Load Regulation (Note 6)	Reg.L	-	Vo × 0.020	Vo × 0.040	V	5mA ≤ Io ≤ 1A Vo ≤ 3.0V
CTL ON Mode Voltage	V_{thH}	2.0	-	-	V	ACTIVE MODE
CTL OFF Mode Voltage	V_{thL}	-	-	0.8	V	OFF MODE
CTL Bias Current	I_{CTL}	-	25	50	μA	

(Note 1) In case of Vo>10V, Vcc=Vo+5V
(Note 2) BD30/33/50/80/90/J2/J5/J6FD0W
(Note 3) BD00/15/18/25/30/33/50FD0W
(Note 4) BD80/90/J2/J5/J6FD0W
(Note 5) BD00/33/50/80/90/J2/J5/J6FD0W
(Note 6) BD15/18/25/30FD0W

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Thermal Resistance (Note 1)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s (Note 3)	2s2p (Note 4)	
HRP5				
Junction to Ambient	θ_{JA}	119.3	22.0	°C/W
Junction to Top Characterization Parameter (Note 2)	Ψ_{JT}	8	3	°C/W
TO263-5				
Junction to Ambient	θ_{JA}	80.7	20.3	°C/W
Junction to Top Characterization Parameter (Note 2)	Ψ_{JT}	8	2	°C/W

(Note 1) Based on JESD51-2A(Still-Air)
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.
(Note 4) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via (Note 5)	
			Pitch	Diameter
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt	1.20mm	Φ0.30mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

(Note 5) This thermal via connects with the copper pattern of all layers. The placement and dimensions obey a land pattern.

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Reference Data

BD00FD0WHFP/FP2 (Vo=5.0V)
Unless otherwise specified, Ta=25°C, Vcc=13.5V, V_{CTL}=5.0V, Io=0mA, Vo=5.0V
(The resistor of between ADJ and Vo =56.7kΩ, ADJ and GND =10.0kΩ)

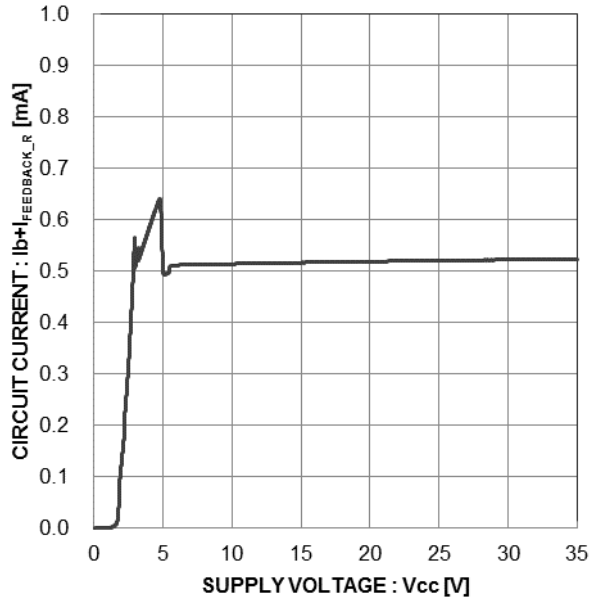


Figure 6. Circuit Current
($I_{FEEDBACK_R}$ ≈ 75μA)

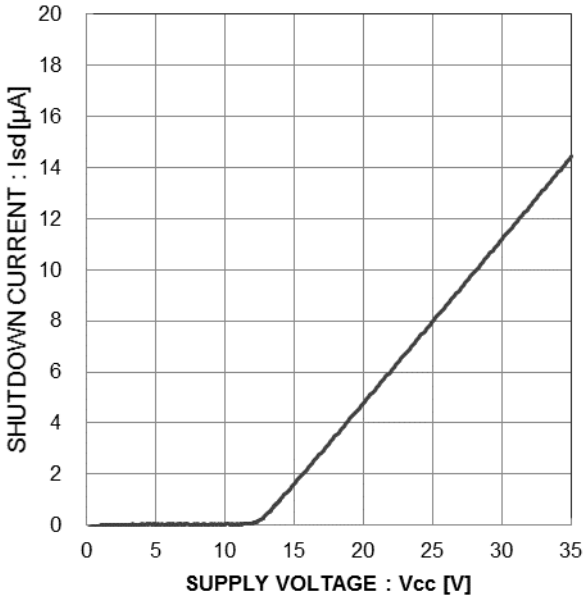


Figure 7. Shutdown Current
(V_{CTL}=0V)

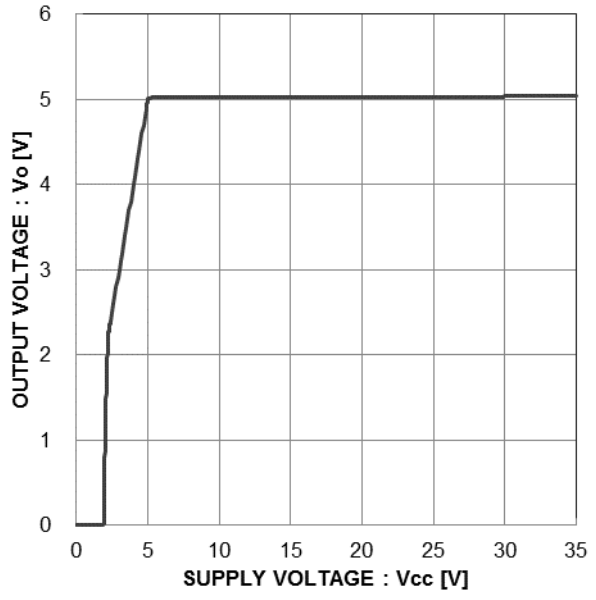


Figure 8. Line Regulation
(Io=0mA)

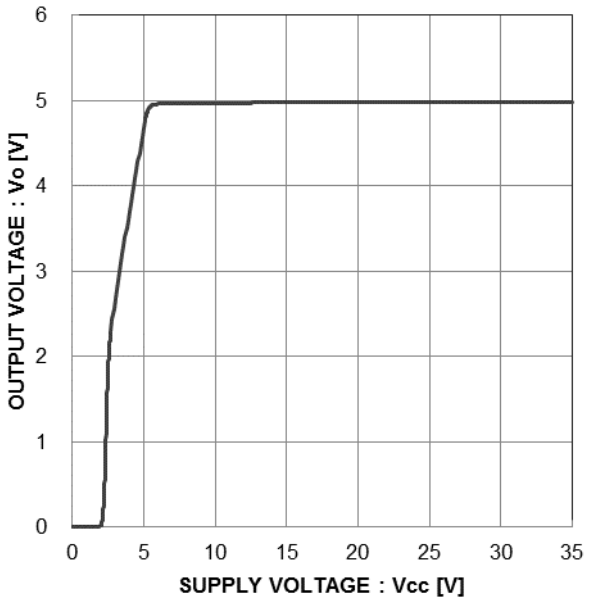


Figure 9. Line Regulation
(Io=1.0A)

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Reference Data - Continue

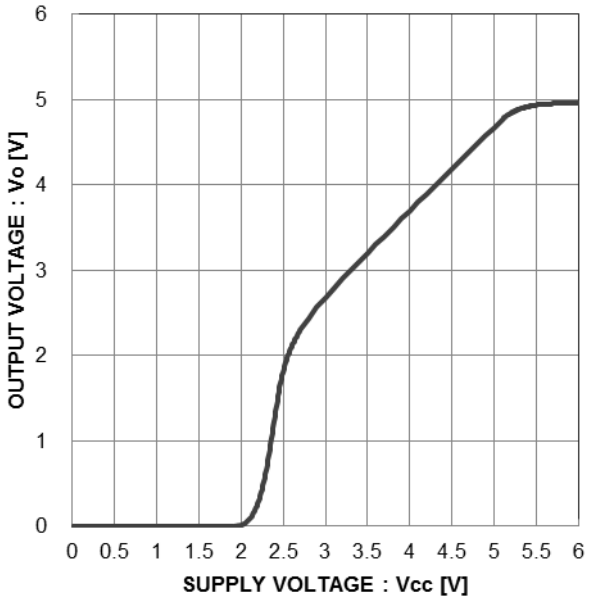


Figure 10. Start up voltage characteristic
(Io=1.0A, Vcc=0 to 6V)

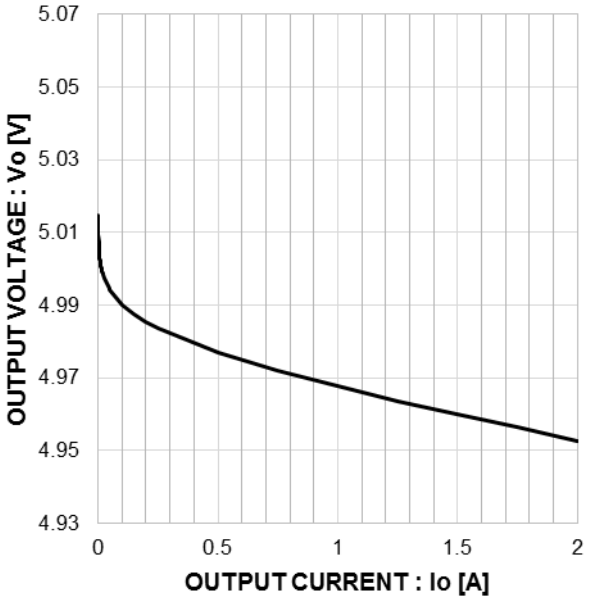


Figure 11. Load regulation
(Io=0 to 2A)

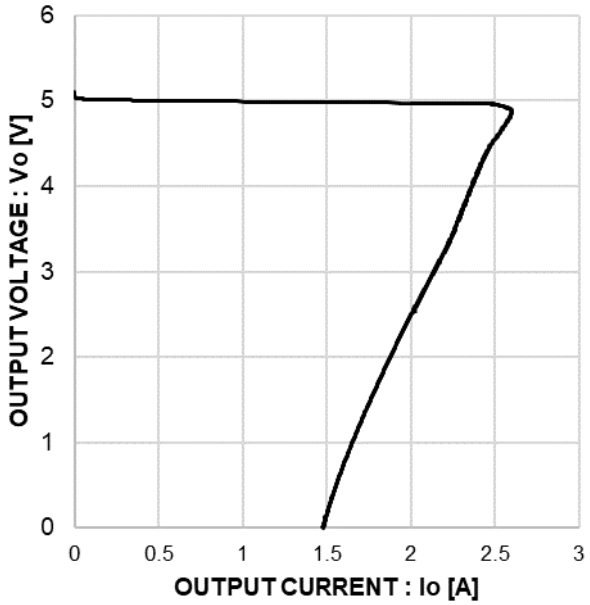


Figure 12. Over Current Protection Characteristic

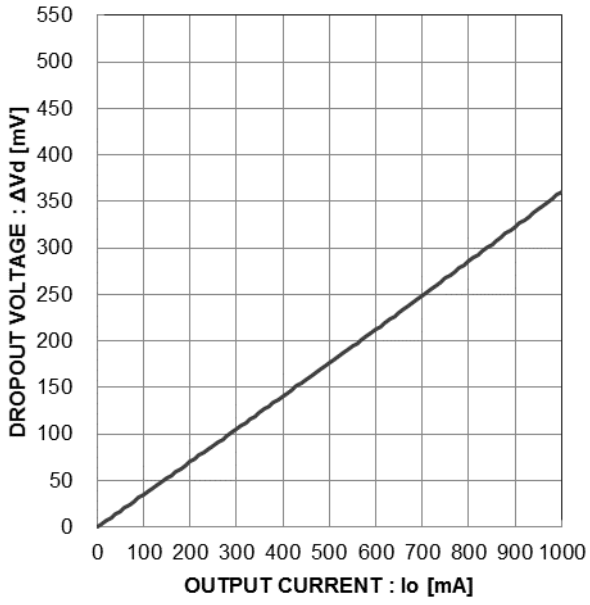


Figure 13. Dropout Voltage
(Vcc=4.75V)

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Reference Data - Continue

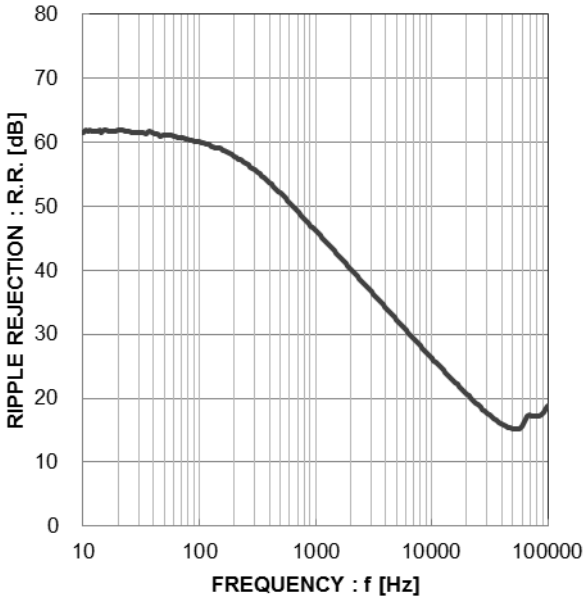


Figure 14. Ripple Rejection
(Io=500mA)

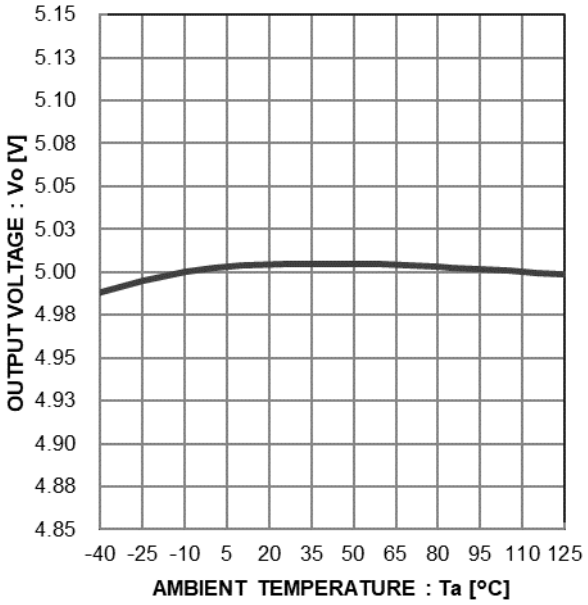


Figure 15. Output Voltage
Temperature Characteristic

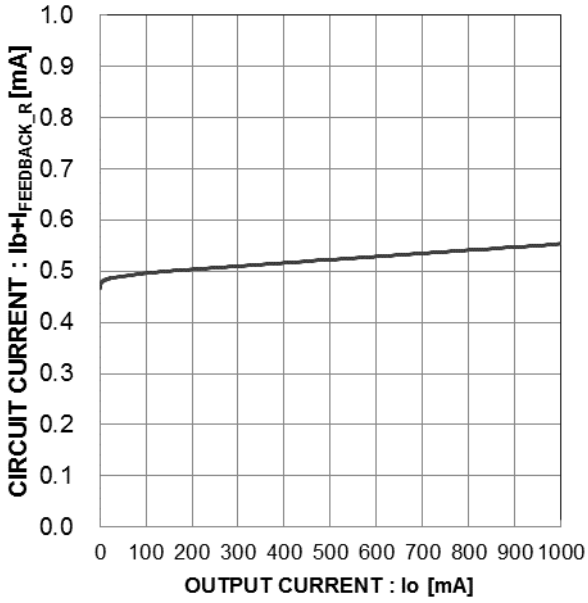


Figure 16. Output Current vs Circuit Current
(0mA ≤ Io ≤ 1000mA, $I_{FEEDBACK_R}$ ≈ 75µA)

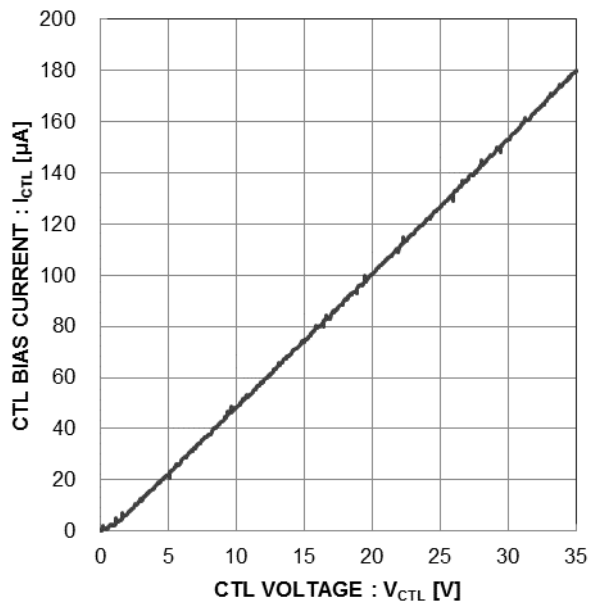


Figure 17. CTL voltage vs CTL current

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Reference Data - Continue

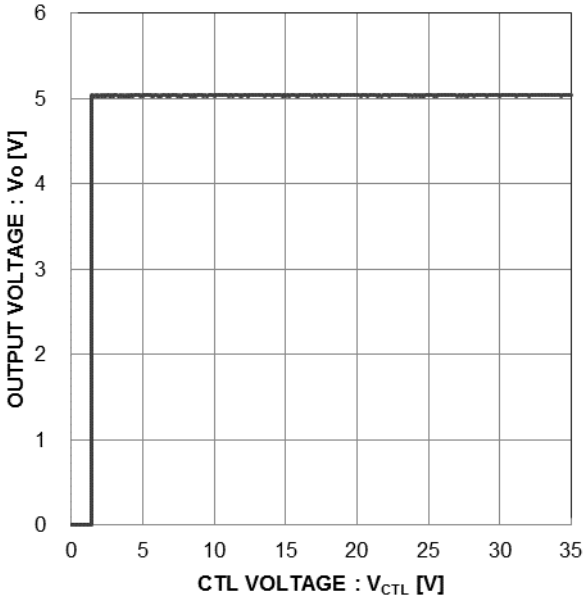


Figure 18. CTL voltage vs. Output Voltage

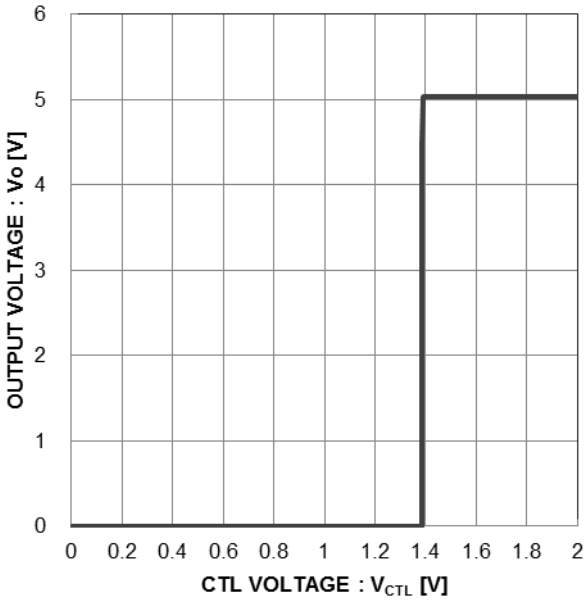


Figure 19. CTL voltage vs. Output Voltage
(V_{CTL}=0 to 2V)

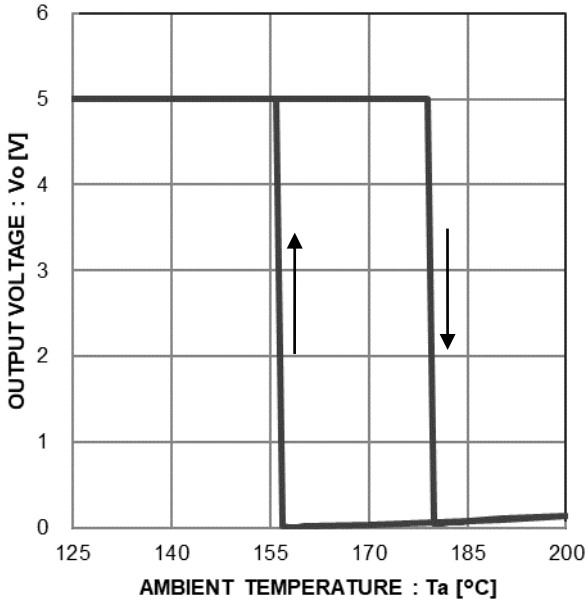
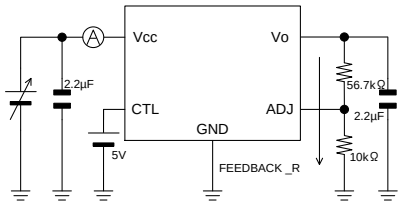


Figure 20. Thermal Shutdown Protection Characteristic

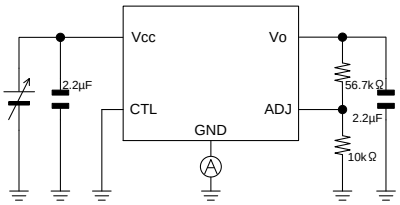
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Measurement setup for reference data

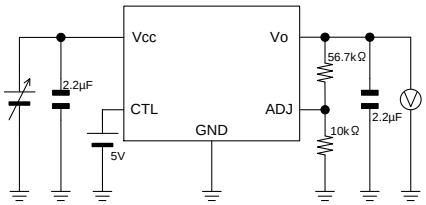
BD00FD0WHFP/FP2 (Vo=5.0V)



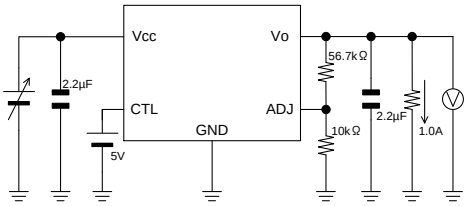
Measurement setup for Figure 6.



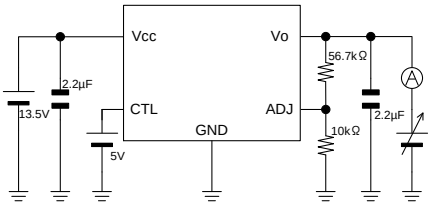
Measurement setup for Figure 7.



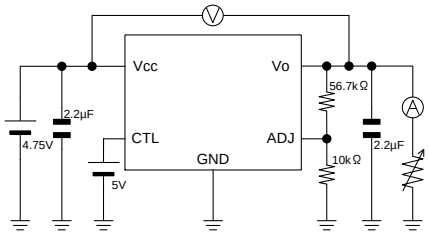
Measurement setup for Figure 8.



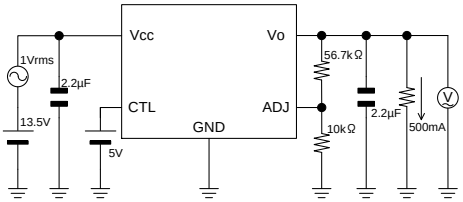
Measurement setup for Figure 9,10.



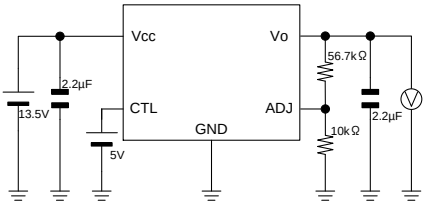
Measurement setup for Figure 11,12.



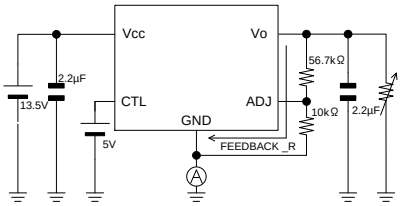
Measurement setup for Figure 13.



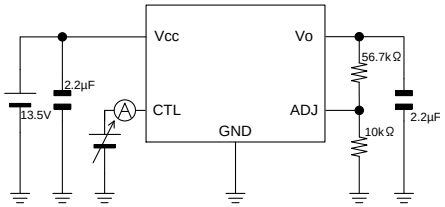
Measurement setup for Figure 14.



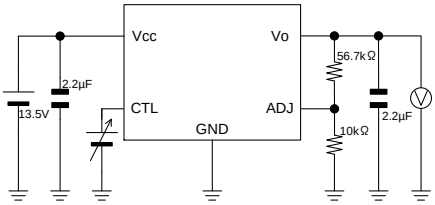
Measurement setup for Figure 15.



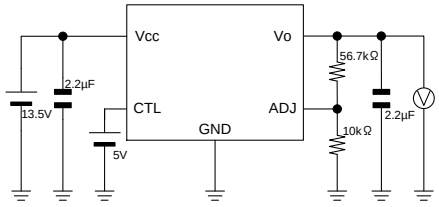
Measurement setup for Figure 16.



Measurement setup for Figure 17.



Measurement setup for Figure 18,19.



Measurement setup for Figure 20.

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Linear Regulators Surge Voltage Protection

The following provides instructions on surge voltage overs absolute maximum ratings polarity protection for ICs.

1. Applying positive surge to the input

If the possibility exists that surges higher than absolute maximum ratings 35 V will be applied to the input, a Zener Diode should be placed to protect the device in between the V_{IN} and the GND as shown in the figure 21.

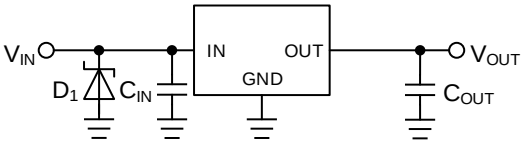


Figure 21. Surges Higher than 35 V will be Applied to the Input

2. Applying negative surge to the input

If the possibility exists that surges lower than absolute maximum ratings -0.3 V will be applied to the input, a Schottky Diode should be place to protect the device in between the V_{IN} and the GND as shown in the figure 22.

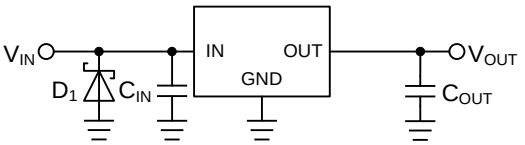


Figure 22. Surges Lower than -0.3 V will be Applied to the Input

Linear Regulators Reverse Voltage Protection

A linear regulator integrated circuit (IC) requires that the input voltage is always higher than the regulated voltage. Output voltage, however, may become higher than the input voltage under specific situations or circuit configurations, and that reverse voltage and current may cause damage to the IC. A reverse polarity connection or certain inductor components can also cause a polarity reversal between the input and output pins. The following provides instructions on reversed voltage polarity protection for ICs.

1. about Input /Output Voltage Reversal

In an MOS linear regulator, a parasitic element exists as a body diode in the drain-source junction portion of its power MOSFET. Reverse input/output voltage triggers the current flow from the output to the input through the body diode. The inverted current may damage or destroy the semiconductor elements of the regulator since the effect of the parasitic body diode is usually disregarded for the regulator behavior (Figure 23).

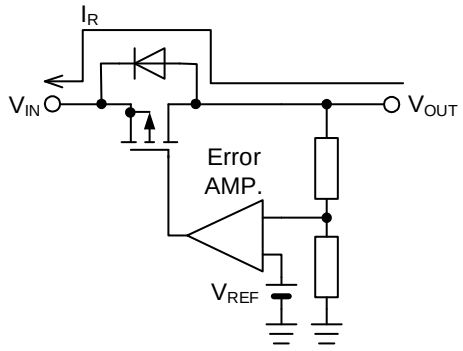


Figure 23. Reverse Current Path in an MOS Linear Regulator

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An effective solution to this is an external bypass diode connected in-between the input and output to prevent the reverse current flow inside the IC (see Figure 24.). Note that the bypass diode must be turned on before the internal circuit of the IC. Bypass diodes in the internal circuits of MOS linear regulators must have low forward voltage V_F. Some ICs are configured with current-limit thresholds to shut down high reverse current even when the output is off, allowing large leakage current from the diode to flow from the input to the output; therefore, it is necessary to choose one that has a small reverse current. Specifically, select a diode with a rated peak inverse voltage greater than the input to output voltage differential and rated forward current greater than the reverse current during use.

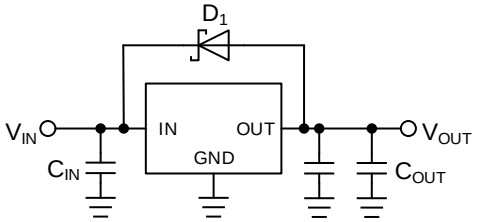


Figure 24. Bypass Diode for Reverse Current Diversion

The lower forward voltage (V_F) of Schottky barrier diodes cater to requirements of MOS linear regulators, however the main drawback is found in the level of their reverse current (I_R), which is relatively high. So, one with a low reverse current is recommended when choosing a Schottky diode. The V_R-I_R characteristics versus temperatures show increases at higher temperatures.

If V_{IN} is open in a circuit as shown in the following Figure 25. with its input/output voltage being reversed, the only current that flows in the reverse current path is the bias current of the IC. Because the amperage is too low to damage or destroy the parasitic element, a reverse current bypass diode is not required for this type of circuit.

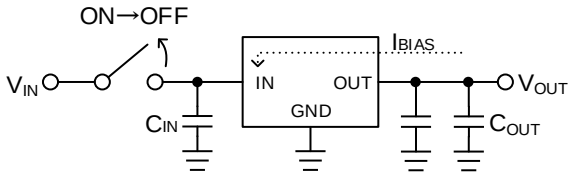


Figure 25. Open V_{IN}

2. Protection against Input Reverse Voltage

Accidental reverse polarity at the input connection flows a large current to the diode for electrostatic breakdown protection between the input pin of the IC and the GND pin, which may destroy the IC (see Figure 26.).

A Schottky barrier diode or rectifier diode connected in series with the power supply as shown in Figure 27. is the simplest solution to prevent this from happening. The solution, however, is unsuitable for a circuit powered by batteries because there is a power loss calculated as $V_F \times I_{OUT,}$ as the forward voltage V_F of the diode drops in a correct connection. The lower V_F of a Schottky barrier diode than that of a rectifier diode gives a slightly smaller power loss. Because diodes generate heat, care must be taken to select a diode that has enough allowance in power dissipation. A reverse connection allows a negligible reverse current to flow in the diode.

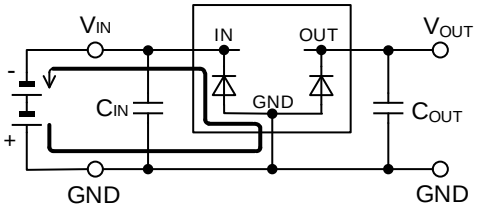


Figure 26. Current Path in Reverse Input Connection

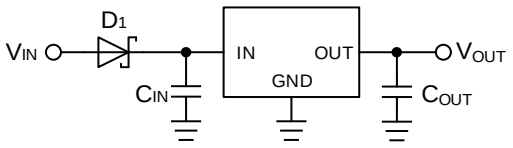


Figure 27. Protection against Reverse Polarity 1

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Figure 28. shows a circuit in which a P-channel MOSFET is connected in series with the power. The diode located in the drain-source junction portion of the MOSFET is a body diode (parasitic element). The voltage drop in a correct connection is calculated by multiplying the resistance of the MOSFET being turned on by the output current I_{OUT}, therefore it is smaller than the voltage drop by the diode (see Figure 27.) and results in less of a power loss. No current flows in a reverse connection where the MOSFET remains off.

If the voltage taking account of derating is greater than the voltage rating of MOSFET gate-source junction, lower the gate-source junction voltage by connecting voltage dividing resistors as shown in Figure 29.

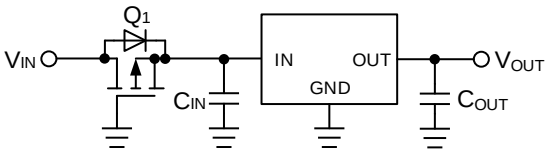


Figure 28. Protection against Reverse Polarity 2

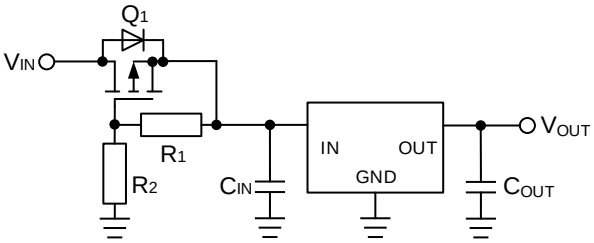


Figure 29. Protection against Reverse Polarity 3

3. Protection against Output Reverse Voltage when Output Connect to an Inductor

If the output load is inductive, electrical energy accumulated in the inductive load is released to the ground upon the output voltage turning off. In-between the IC output and ground pins is a diode for preventing electrostatic breakdown, in which a large current flows that could destroy the IC. To prevent this from happening, connect a Schottky barrier diode in parallel with the diode (see Figure 30.).

Further, if a long wire is in use for the connection between the output pin of the IC and the load, observe the waveform on an oscilloscope, since it is possible that the load becomes inductive. An additional diode is needed for a motor load that is affected by its counter electromotive force, as it produces an electrical current in a similar way.

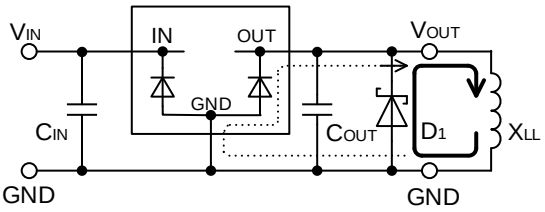


Figure 30. Current Path in Inductive Load (Output: Off)

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Thermal design

HRP5

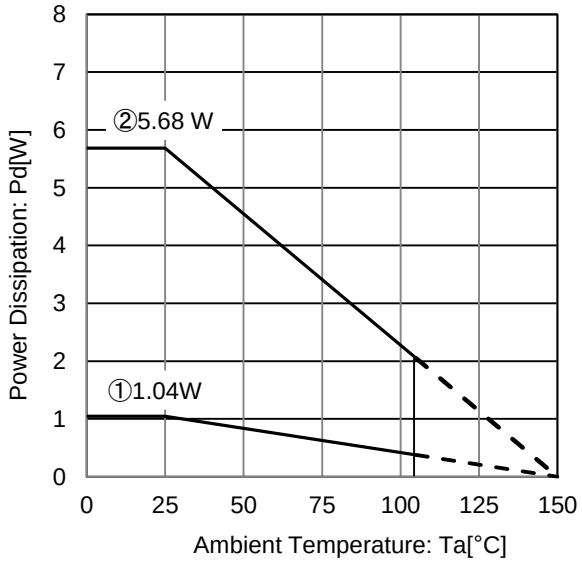


Figure 31. Power Dissipation (HRP5)

IC mounted on ROHM standard board based on JEDEC.

① : 1 - layer PCB
(Copper foil area on the reverse side of PCB: 0 mm x 0 mm)
Board material: FR4
Board size: 114.3 mm x 76.2 mm x 1.57 mmt
Mount condition: PCB and exposed pad are soldered.
Top copper foil: ROHM recommended
footprint + wiring to measure, 2 oz. copper.

② : 4 - layer PCB
(2 inner layers and Copper foil area on the reverse side of PCB:
74.2 mm x 74.2 mm)
Board material: FR4
Board size: 114.3 mm x 76.2 mm x 1.60 mmt
Mount condition: PCB and exposed pad are soldered.
Top copper foil: ROHM recommended
footprint + wiring to measure, 2 oz. copper.
2 inner layers copper foil area of PCB
: 74.2 mm x 74.2 mm, 1 oz. copper.
Copper foil area on the reverse side of PCB
: 74.2 mm x 74.2 mm, 2 oz. copper.

Condition①: θ_{JA} = 119.3 °C/W、Ψ_{JT} (top) = 8 °C/W
Condition②: θ_{JA} = 22.0 °C/W、Ψ_{JT} (top) = 3 °C/W

TO263-5

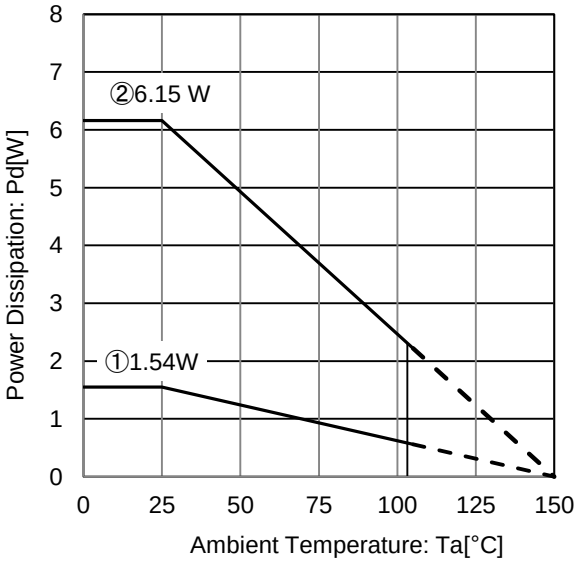


Figure 32. Power Dissipation (TO263-5)

IC mounted on ROHM standard board based on JEDEC.

① : 1 - layer PCB
(Copper foil area on the reverse side of PCB: 0 mm x 0 mm)
Board material: FR4
Board size: 114.3 mm x 76.2 mm x 1.57 mmt
Mount condition: PCB and exposed pad are soldered.
Top copper foil: ROHM recommended
footprint + wiring to measure, 2 oz. copper.

② : 4 - layer PCB
(2 inner layers and Copper foil area on the reverse side of PCB:
74.2 mm x 74.2 mm)
Board material: FR4
Board size: 114.3 mm x 76.2 mm x 1.60 mmt
Mount condition: PCB and exposed pad are soldered.
Top copper foil: ROHM recommended
footprint + wiring to measure, 2 oz. copper.
2 inner layers copper foil area of PCB
: 74.2 mm x 74.2 mm, 1 oz. copper.
Copper foil area on the reverse side of PCB
: 74.2 mm x 74.2 mm, 2 oz. copper.

Condition①: θ_{JA} = 80.7 °C/W、Ψ_{JT} (top) = 8 °C/W
Condition②: θ_{JA} = 20.3 °C/W、Ψ_{JT} (top) = 2 °C/W

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When operating at temperature more than Ta=25°C, please refer to the power dissipation characteristic curve shown in Figure 31.
The IC characteristics are closely related to the temperature at which the IC is used, so it is necessary to operate the IC at temperatures less than the maximum junction temperature Tjmax.

Figure 31. show the acceptable power dissipation characteristic curves of the HRP5 package. Even when the ambient temperature (Ta) is at normal temperature (25°C), the chip junction temperature (Tj) may be quite high so please operate the IC at temperatures less than the acceptable power dissipation.

The calculation method for power consumption Pc(W) is as follows

$$Pc = (Vcc - Vo) \times Io + Vcc \times Ib$$

Acceptable loss Pd ≥ Pc

Solving this for load current Io in order to operate within the acceptable loss

$$Io \leq \frac{Pd - Vcc \times Ib}{Vcc - Vo}$$

Vcc : Input voltage
Vo : Output voltage
Io : Load current
Ib : Circuit current

It is then possible to find the maximum load current Iomax with respect to the applied voltage Vcc at the time of thermal design.

Calculation Example) When HRP5, Ta=85°C, Vcc=13.5V, Vo=5.0V

$$Io \leq \frac{2.953 - 13.5 \times Ib}{8.5}$$

$$Io \leq 346.5.2\ mA \quad (Ib: 0.58mA)$$

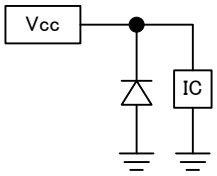
(Figure 31 ②θja=22°C /W →-45.5mW/°C
25°C =5.68W → 85°C =2.953W)

Please refer to the above information and keep thermal designs within the scope of acceptable loss for all operating temperature ranges.

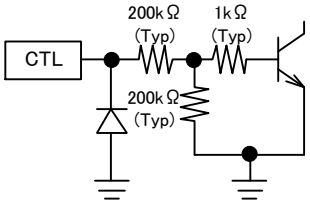
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I/O equivalence circuit

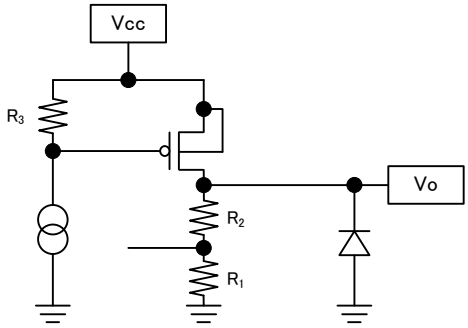
Vcc Terminal



CTL Terminal



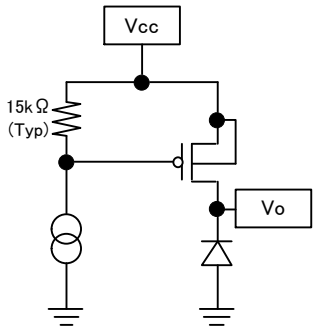
Vo Terminal BD15/18/25/30/33/50/80/90/J2/J5/J6FD0W



	R_1 (kΩ) (Typ)	R_2 (kΩ) (Typ)	R_3 (kΩ) (Typ)
BD15FD0	10.0	10.2	15.0
BD18FD0		14.2	
BD25FD0		23.6	
BD30FD0		29.5	20.0
BD33FD0		33.5	
BD50FD0		56.1	
BD80FD0	5.0	47.9	
BD90FD0		54.5	
BDJ2FD0		74.5	
BDJ5FD0	4.0	75.4	
BDJ6FD0		80.6	

BD00FD0W

Vo Terminal



ADJ Terminal

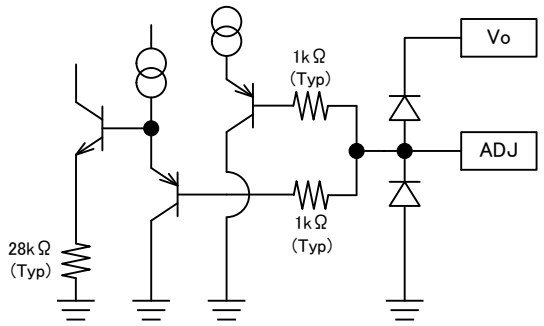
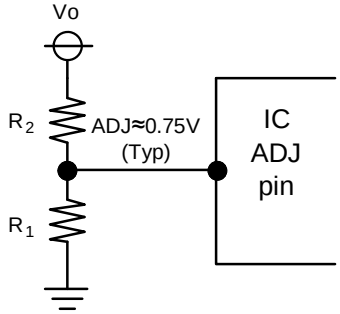


Figure 33. I/O equivalence circuit

Output Voltage Configuration Method (BD00FD0WHFP/FP2)

Please connect resistors R_1 and R_2 (which determines the output voltage) as shown in Figure 34.
Please be aware that the offset due to the current that flows from the ADJ terminal becomes large when resistor values are large. Due to this, resistance ranging from 5kΩ to 10kΩ is highly recommended for R_1.



$$Vo \approx ADJ \times (R_1+R_2)/R_1$$

Figure 34. Output Voltage Configuration

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Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 114.3mm x 76.2mm x 1.57mmt(1S) / 114.3mm x 76.2mm x 1.60mmt(2S2P) glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

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Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):
When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.
Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

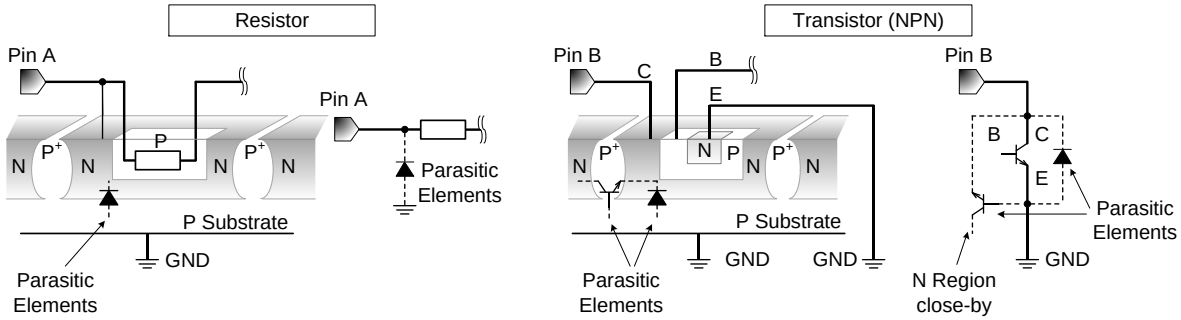


Figure 35. Example of monolithic IC structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated over current protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

14. Vcc Pin

Insert a capacitor (Vo ≥ 5.0V : capacitor ≥ 1μF, 1.5V < Vo ≤ 5.0V : capacitor ≥ 2.2μF) between the Vcc and GND pins. Choose the capacitance according to the line between the power smoothing circuit and the Vcc pin. Selection of the capacitance also depends on the application. Verify the application and allow for sufficient margins in the design. We recommend using a capacitor with excellent voltage and temperature characteristics.

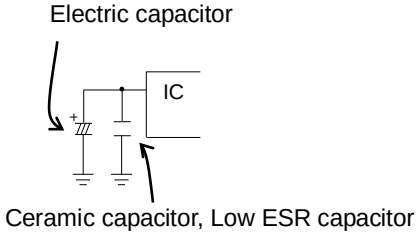


Figure 36. Input Capacitor

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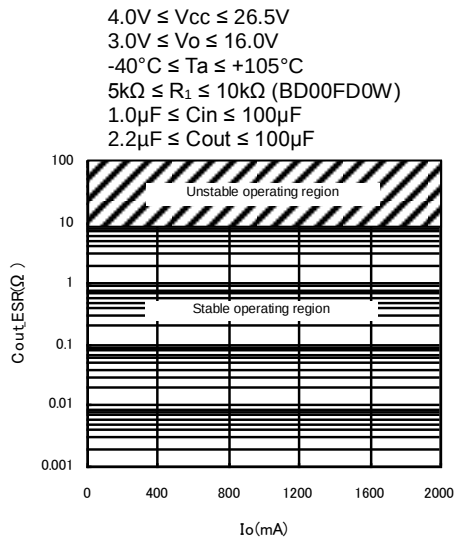
Operational Notes – continued

15. Output Pin

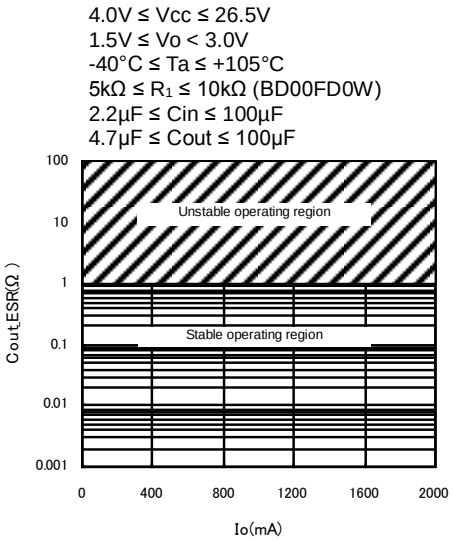
In order to prevent oscillation, a capacitor needs to be placed between the output pin and GND pin. We recommend a capacitor with a capacitance of more than 2.2μF(Min) (3.0V ≤ Vo ≤ 16.0V). Electrolytic, tantalum and ceramic capacitors can be used. We recommend a capacitor with a capacitance of more than 4.7μF(Min) (1.5V ≤ Vo < 3.0V). Ceramic capacitors can be used. When selecting the capacitor ensure that the capacitance of more than 2.2μF(Min)(3.0V ≤ Vo ≤ 16.0V) or more than 4.7μF(Min)(1.5V ≤ Vo < 3.0V) is maintained at the intended applied voltage and temperature range. Due to changes in temperature, the capacitance can fluctuate possibly resulting in oscillation. For selection of the capacitor refer to the Cout ESR vs Io data. The stable operation range given in the reference data is based on the standalone IC and resistive load. For actual applications the stable operating range is influenced by the PCB impedance, input supply impedance and load impedance. Therefore verification of the final operating environment is needed.

When selecting a ceramic type capacitor, we recommend using X5R, X7R or better with excellent temperature and DC-biasing characteristics and high voltage tolerance.

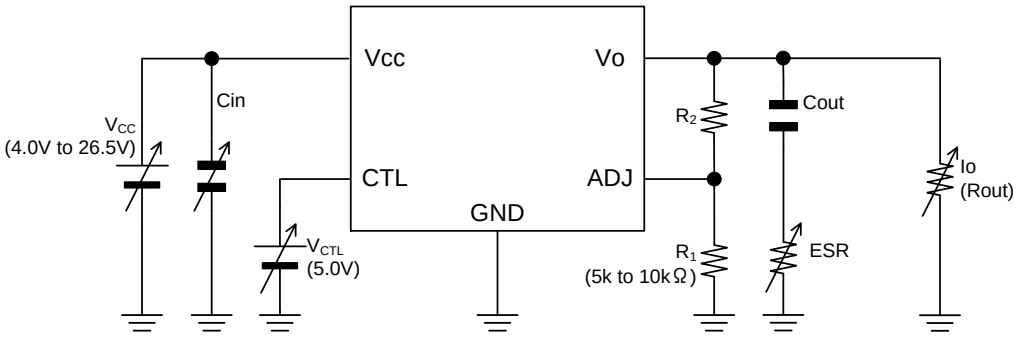
Also, in case of rapidly changing input voltage and load current, select the capacitance in accordance with verifying that the actual application meets with the required specification.



Cout ESR vs Io
3.0V ≤ Vo ≤ 16.0V



Cout ESR vs Io
1.5V ≤ Vo < 3.0V



Measurement circuit (BD00FD0W)

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Operational Notes – continued

16. CTL Pin

Do not set the voltage level on the IC's enable pin in between VthH and VthL. Do not leave it floating or unconnected, otherwise, the output voltage would be unstable.

17. Rapid variation in Vcc Voltage and load Current CTL Pin

In case of a rapidly changing input voltage, transients in the output voltage might occur due to the use of a MOSFET as output transistor. Although the actual application might be the cause of the transients, the IC input voltage, output current and temperature are also possible causes. In case problems arise within the actual operating range, use countermeasures such as adjusting the output capacitance.

18. Minute variation in output voltage

In case of using an application susceptible to minute changes to the output voltage due to noise, changes in input and load current, etc., use countermeasures such as implementing filters.

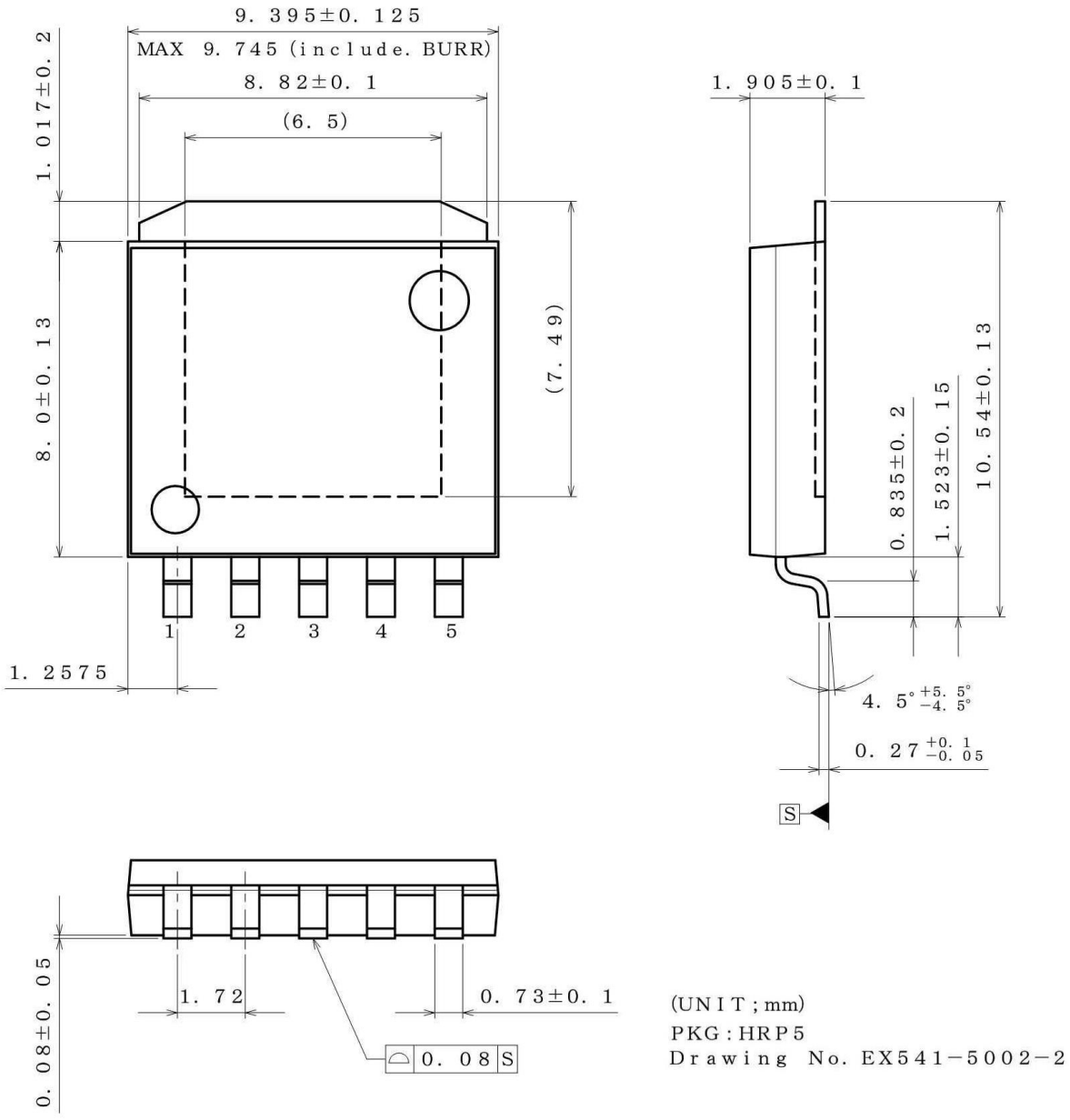
19. Regarding the Input Pin and Vcc voltage

In some applications, the Vcc and pin potential might be reversed, possibly resulting in circuit internal damage or damage to the elements. For example, while the external capacitor is charged, the Vcc shorts to the GND. Use a capacitor with a capacitance with less than 1000µF. We also recommend using reverse polarity diodes in series or a bypass between all pins and the Vcc pin.

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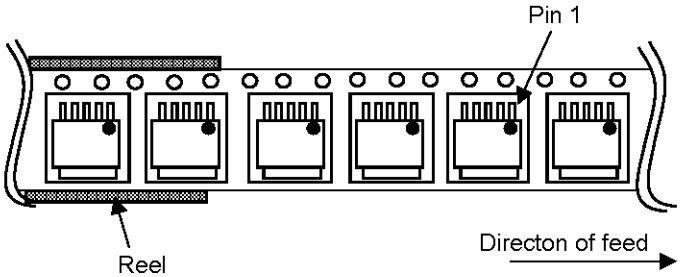
Physical Dimension, Tape and Reel Information

Package Name	HRP5



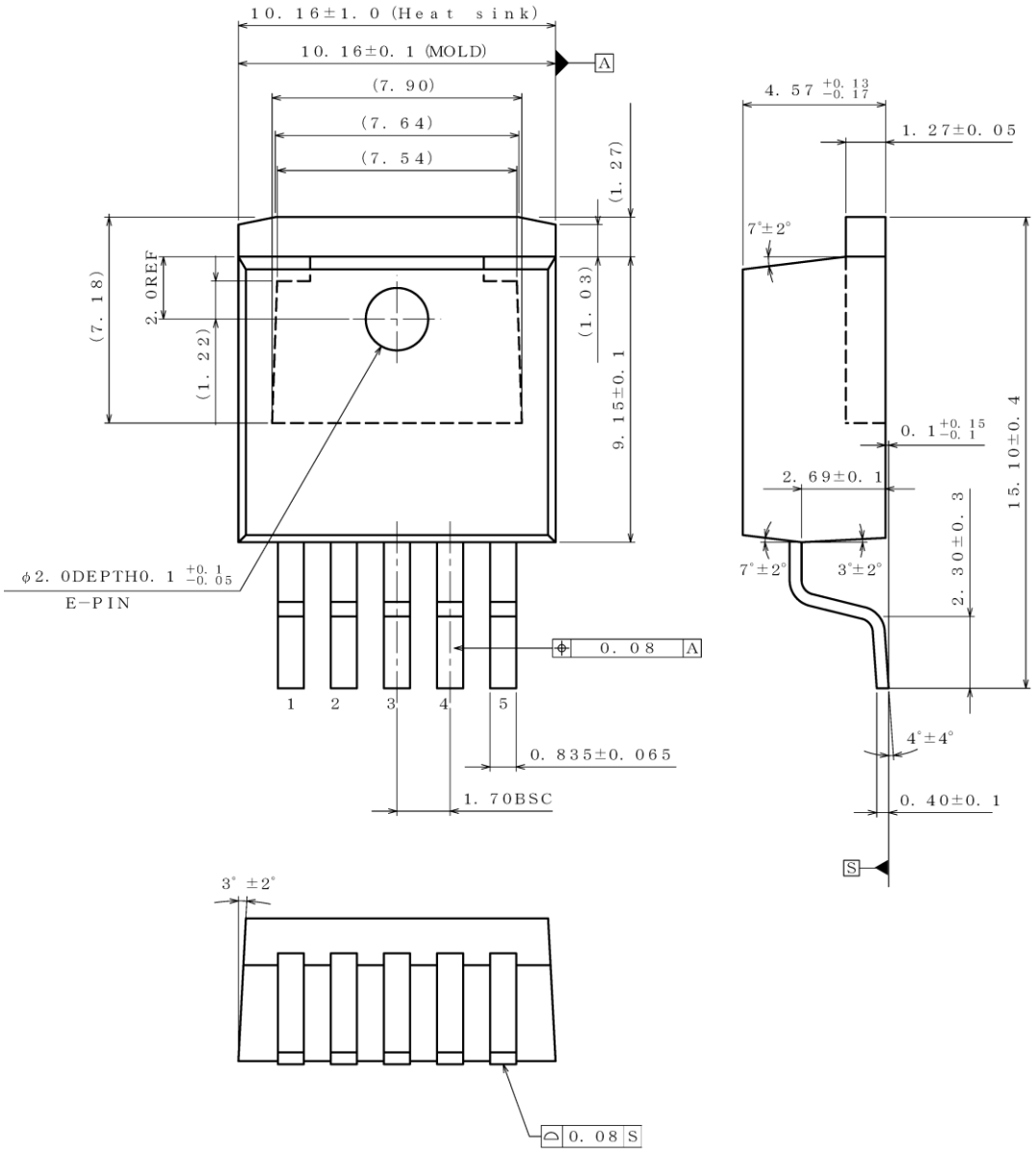
< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	TR The direction is the pin 1 of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand



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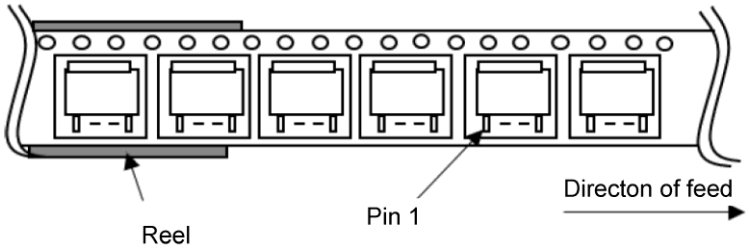
Package Name	TO263-5



(UNIT : mm)
PKG : TO263-5
Drawing No. EX573-5002

< Tape and Reel Information >

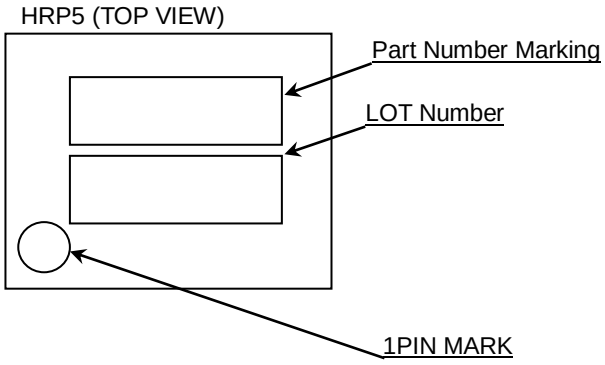
Tape	Embossed carrier tape
Quantity	500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the lower left when you hold reel on the left hand and you pull out the tape on the right hand



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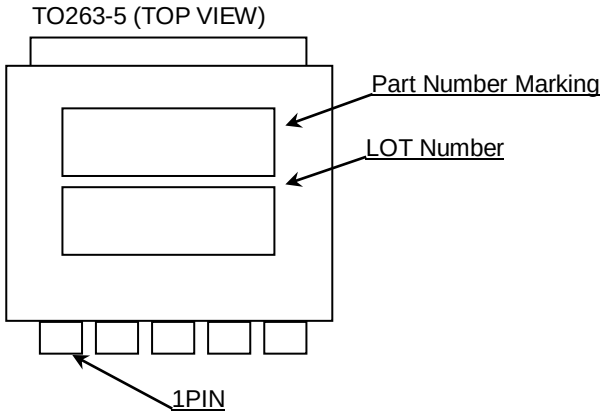
Marking Diagrams

HRP5



Output Voltage[V]	Part Number Marking
Variable	D00FD0WHFP
1.5	D15FD0WHFP
1.8	D18FD0WHFP
2.5	D25FD0WHFP
3.0	D30FD0WHFP
3.3	D33FD0WHFP
5.0	D50FD0WHFP
8.0	D80FD0WHFP
9.0	D90FD0WHFP
12.0	DJ2FD0WHFP
15.0	DJ5FD0WHFP
16.0	DJ6FD0WHFP

TO263-5



Output Voltage[V]	Part Number Marking
Variable	00FD0WFP2
1.5	15FD0WFP2
1.8	18FD0WFP2
2.5	25FD0WFP2
3.0	30FD0WFP2
3.3	33FD0WFP2
5.0	50FD0WFP2
8.0	80FD0WFP2
9.0	90FD0WFP2
12.0	J2FD0WFP2
15.0	J5FD0WFP2
16.0	J6FD0WFP2

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Revision History

Date	Revision	Changes
21.Mar.2017	001	New Release
15.Mar.2018	002	TO263-5 package added
09.Sep.2019	003	Figure 12 changed Notation variation fixed

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JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

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1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
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   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

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4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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