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CAT6219

LDO Regulator - CMOS

500 mA

Description

The CAT6219 is a 500 mA CMOS low dropout regulator that provides fast response time during load current and line voltage changes.

The quick-start feature allows the use of an external bypass capacitor to reduce the overall output noise without affecting the turn-on time of just 150 μs.

With zero shutdown current and low ground current of 55 μA typical, the CAT6219 is ideal for battery-operated devices with supply voltages from 2.3 V to 5.5 V. An internal under voltage lockout circuit disables the output at supply voltages under 2.15 V typical.

The CAT6219 offers 1% initial accuracy and low dropout voltage, 300 mV typical at 500 mA. Stable operation is provided with a small value ceramic capacitor, reducing required board space and component cost.

Other features include current limit and thermal protection.

The LDO is available in fixed and adjustable output in the low profile (1 mm max height) 5−lead TSOT23, 6−pad 1.5 mm x 1.5 mm WDFN and in the 6−pad 2 mm x 2 mm TDFN packages.

Features

- Guaranteed 500 mA Peak Output Current
- Low Dropout Voltage of 300 mV Typical at 500 mA
- Stable with Ceramic Output Capacitor
- External 10 nF Bypass Capacitor for Low Noise
- Quick−start Feature
- Under Voltage Lockout
- No−load Ground Current of 55 μA Typical
- Full−load Ground Current of 85 μA Typical
- ±1.0% Initial Accuracy ($V_{OUT} \geq 2.0$ V)
- ±2.0% Accuracy Over Temperature ($V_{OUT} \geq 2.0$ V)
- “Zero” Current Shutdown Mode
- Fold−back Current Limit
- Thermal Protection
- 5−lead TSOT−23, 6−pad WDFN and TDFN Packages
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Cellular Phones
- Battery−powered Devices
- Consumer Electronics

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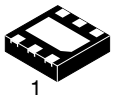
http://onsemi.com



TSOT−23
TD SUFFIX
CASE 419AE

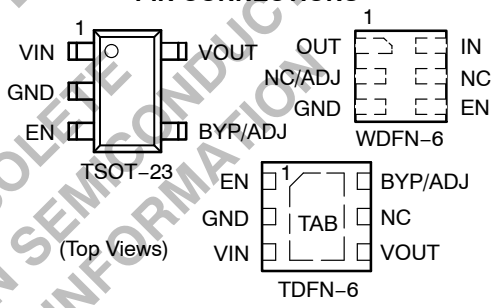


WDFN−6
MV2 SUFFIX
CASE 511BJ

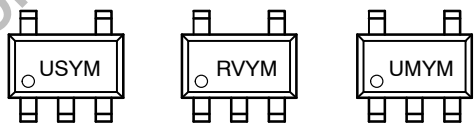


TDFN−6
VP5 SUFFIX
CASE 511AH

PIN CONNECTIONS



MARKING DIAGRAMS

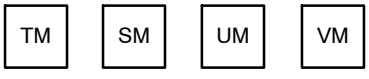


US = CAT6219−125, CAT6219−250, CAT6219−300 Device Code
RV = CAT6219−180, CAT6219−280, CAT6219−285, CAT6219−330 Device Code
UM = CAT6219−ADJ Device Code
Y = Production Year (last digit)
M = Production Month: 1 − 9, A, B, C



(TDFN)

AB = CAT6219180, CAT6219VP5 Device Code
Y = Production Year (last digit)
M = Production Month: 1 − 9, A, B, C



(WDFN)

T = CAT6219−285MV2 Device Code
S = CAT6219−280MV2 Device Code
U = CAT6219−330MV2 Device Code
V = CAT6219−ADJMV2 Device Code
M = Date Code

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

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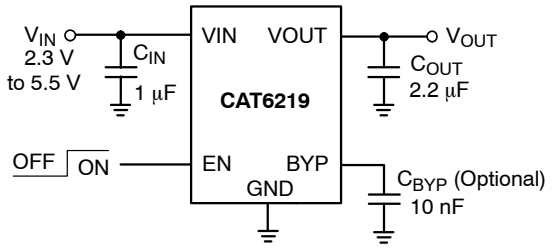


Figure 1. Typical Application Circuit

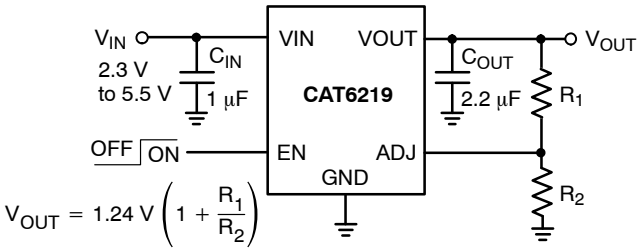


Figure 2. Adjustable Output LDO

Table 1. PIN DESCRIPTIONS

Name	Function
VIN	Supply voltage input.
GND	Ground reference.
EN	Enable input (active high); a 2.5 MΩ pull−down resistor is provided.
BYP	Optional bypass capacitor connection for noise reduction and PSRR enhancing.
ADJ	Adjustable input. Feedback pin connected to resistor divider.
VOUT	LDO Output Voltage.
TAB	To be connected to the ground plane on PCB

Pin Function

VIN is the supply pin for the LDO. A small 1 μF ceramic bypass capacitor is required between the V_{IN} pin and ground near the device. When using longer connections to the power supply, C_{IN} value can be increased without limit. The operating input voltage range is from 2.3 V to 5.5 V.

EN is the enable control logic (active high) for the regulator output. It has a 2.5 MΩ pull−down resistor, which assures that if EN pin is left open, the circuit is disabled.

VOUT is the LDO regulator output. A small 2.2 μF ceramic bypass capacitor is required between the VOUT pin and ground. For better transient response, its value can be increased to 4.7 μF.

The capacitor should be located near the device. For the SOT23-5 package, a continuous 500 mA output current may turn-on the thermal protection. A 250 Ω internal shutdown switch discharges the output capacitor in the no-load condition.

GND is the ground reference for the LDO. The pin must be connected to the ground plane on the PCB.

BYP is the reference bypass pin. An optional 0.01 μF capacitor can be connected between BYP pin and GND to reduce the output noise and enhance the PSRR at high frequency.

ADJ is the adjustable input pin for the adjustable LDO. The pin is connected to the resistor voltage divider.

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Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
V_{IN}	0 to 6.5	V
V_{EN}, V_{OUT}	−0.3 to V_{IN} + 0.3	V
Junction Temperature, T_J	+150	°C
Power Dissipation, P_D	Internally Limited (Note 1)	mW
Storage Temperature Range, T_S	−65 to +150	°C
Lead Temperature (soldering, 5 sec.)	260	°C
ESD Rating (Human Body Model)	3	kV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. RECOMMENDED OPERATING CONDITIONS (Note 2)

Parameter	Range	Unit
V_{IN}	2.3 to 5.5	V
V_{EN}	0 to V_{IN}	V
Junction Temperature Range, T_J	−40 to +125	°C
Package Thermal Resistance, θ_{JA} SOT23−5 TDFN−6	235 206	°C/W

NOTE: Typical application circuit with external components is shown above.

1. The maximum allowable power dissipation at any T_A (ambient temperature) is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown.
2. The device is not guaranteed to work outside its operating rating.

Table 4. ELECTRICAL OPERATING CHARACTERISTICS (Note 3)
(V_{IN} = V_{OUT} + 1.0 V, V_{EN} = High, I_{OUT} = 100 μA, C_{IN} = 1 μF, C_{OUT} = 2.2 μF, ambient temperature of 25°C (over recommended operating conditions unless specified otherwise). **Bold numbers** apply for the entire junction temperature range.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{OUT-ACC}$	Output Voltage Accuracy	Initial accuracy for V_{OUT} ≥ 2.0 V (Note 6)	−1.0		+1.0	%
			−2.0		**+2.0**	
TC_{OUT}	Output Voltage Temp. Coefficient			40		ppm/°C
V_{R-LINE}	Line Regulation	V_{IN} = V_{OUT} + 1.0 V to 5.5 V	−0.2	±0.1	+0.2	%/V
			−0.4		**+0.4**	
V_{R-LOAD}	Load Regulation	I_{OUT} = 100 μA to 500 mA		1	1.5	%
					2	
V_{DROP}	Dropout Voltage (Note 4)	I_{OUT} = 500 mA		300	400	mV
					500	
I_{GND}	Ground Current	I_{OUT} = 0 μA		55	75	μA
					90	
		I_{OUT} = 500 mA		85		
I_{GND-SD}	Shutdown Ground Current	V_{EN} < 0.4 V			1	μA
					2	
PSRR	Power Supply Rejection Ratio	f = 1 kHz, C_{BYP} = 10 nF		64		dB
		f = 20 kHz, C_{BYP} = 10 nF		54		
I_{SC}	Output short circuit current limit	V_{OUT} = 0 V		200		mA
T_{ON}	Turn−On Time	C_{BYP} = 10 nF		150		μs
e_N	Output Noise Voltage (Note 5)	BW = 10 Hz to 100 kHz		45		μVrms
R_{OUT-SH}	Shutdown Switch Resistance			250		Ω
R_{EN}	Enable pull−down resistor			2.5		MΩ
V_{UVLO}	Under voltage lockout threshold			2.15		V
ESR	C_{OUT} equivalent series resistance		5		500	mΩ
V_{ADJ}	Adjustable input voltage	I_{OUT} = 100 μA	1.2	1.24	1.27	V
ENABLE INPUT						
V_{HI}	Logic High Level	V_{IN} = 2.3 to 5.5 V	**1.8**			V
		V_{IN} = 2.3 to 5.5 V, 0°C to +125°C junction temperature	1.6			
V_{LO}	Logic Low Level	V_{IN} = 2.3 to 5.5 V			**0.4**	V
I_{EN}	Enable Input Current	V_{EN} = 0.4 V		0.15	**1**	μA
		V_{EN} = V_{IN}		1.5	**4**	
THERMAL PROTECTION						
T_{SD}	Thermal Shutdown			160		°C
T_{HYS}	Thermal Hysteresis			10		°C

3. Specification for 2.80 V output version unless specified otherwise.
4. Dropout voltage is defined as the input−to−output differential at which the output voltage drops 2% below its nominal value. During test, the input voltage stays always above the minimum 2.3 V.
5. Specification for 1.8 V output version.
6. For V_{OUT} < 2.0 V, the initial accuracy is ±2% and across temperature ±3%.

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TYPICAL CHARACTERISTICS (shown for 2.80 V output option)

(V_{IN} = 3.85 V, I_{OUT} = 100 μA, C_{IN} 1 μF, = C_{OUT} = 2.2 μF, C_{BYP} = 10 nF, T_A = 25°C unless otherwise specified.)

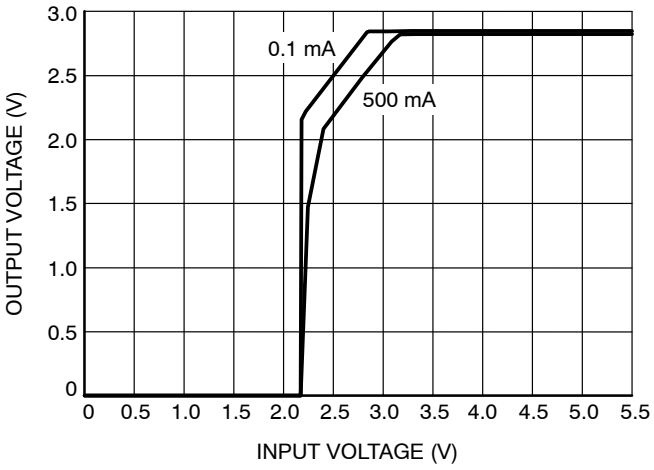


Figure 3. Dropout Characteristics

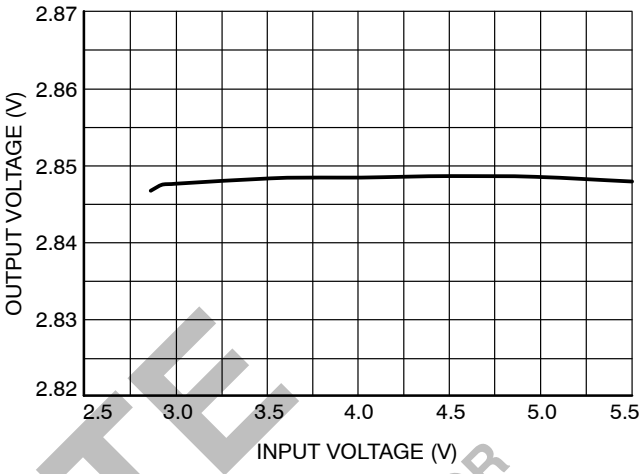


Figure 4. Line Regulation

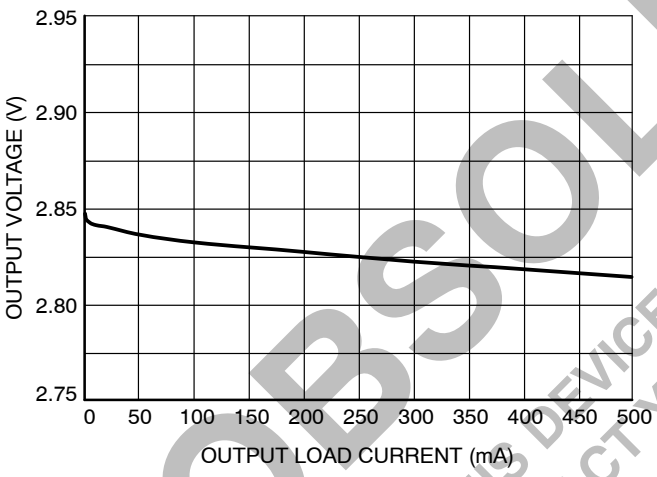


Figure 5. Load Regulation

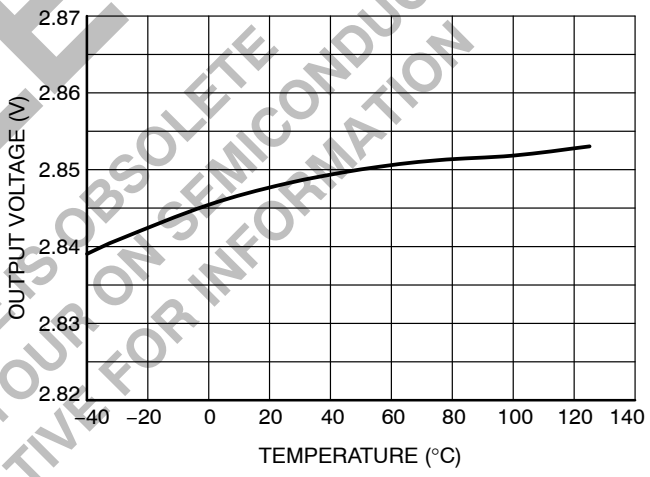


Figure 6. Output Voltage vs. Temperature

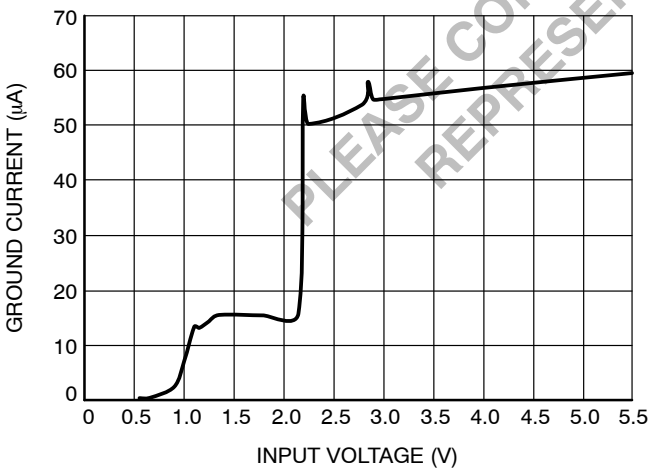


Figure 7. Ground Current vs. Input Voltage

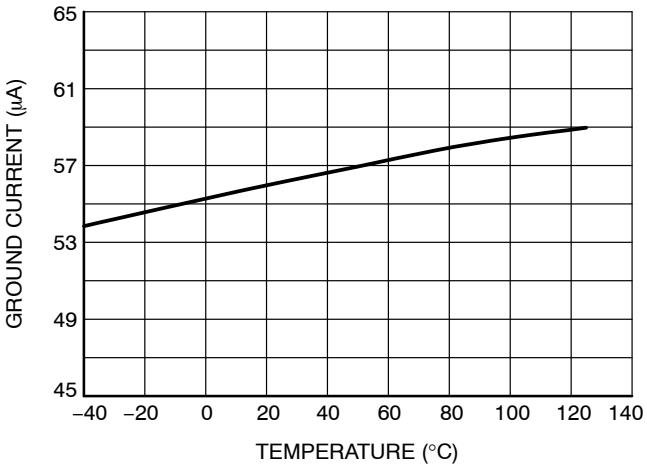


Figure 8. Ground Current vs. Temperature

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TYPICAL CHARACTERISTICS (shown for 2.80 V output option)

(V_{IN} = 3.85 V, I_{OUT} = 100 μA, C_{IN} 1 μF, = C_{OUT} = 2.2 μF, C_{BYP} = 10 nF, T_A = 25°C unless otherwise specified.)

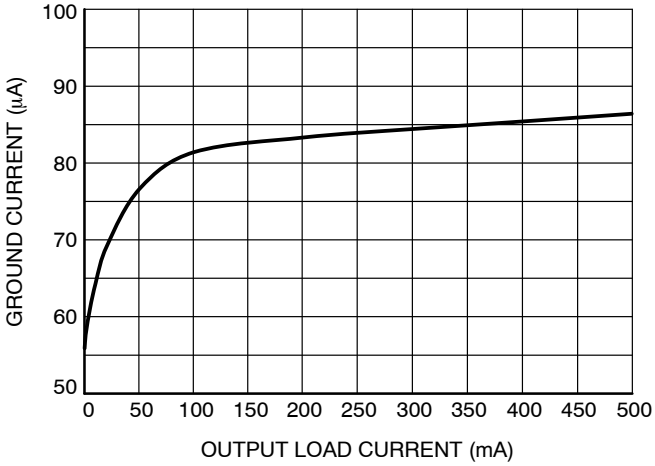


Figure 9. Ground Current vs. Load Current

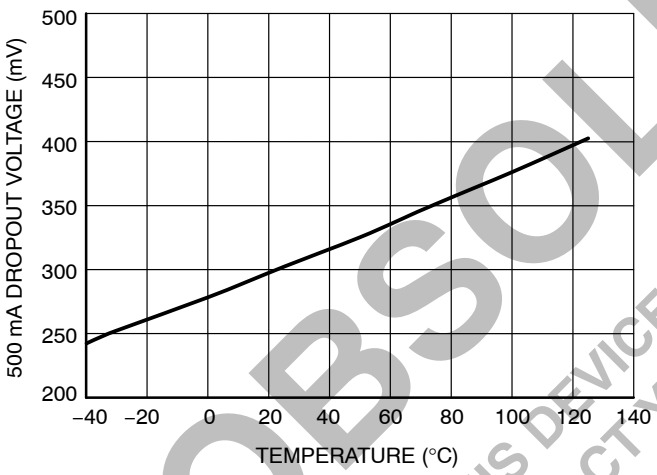


Figure 10. Dropout vs. Temperature (500 mA Load)

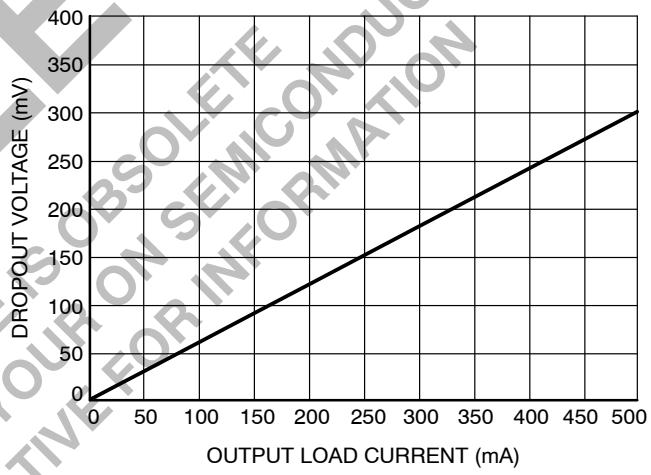


Figure 11. Dropout vs. Load Current

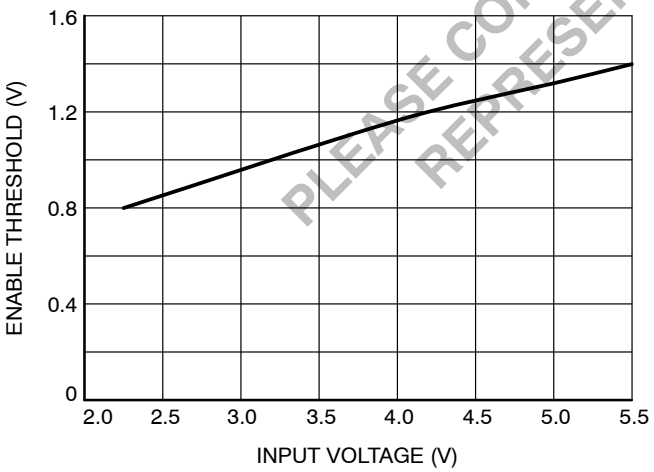


Figure 12. Enable Threshold vs. Input Voltage

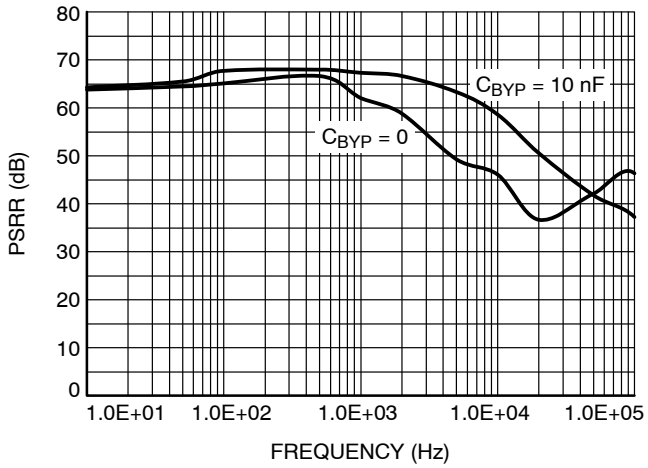


Figure 13. PSRR vs. Frequency (10 mA Load)

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TRANSIENT CHARACTERISTICS (shown for 2.80 V output option)

(V_{IN} = 3.85 V, I_{OUT} = 100 μA, C_{IN} 1 μF, = C_{OUT} = 2.2 μF, C_{BYP} = 10 nF, T_A = 25°C unless otherwise specified.)

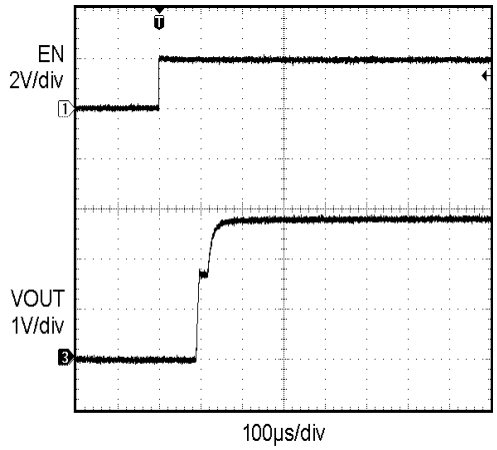


Figure 14. Enable Turn−on (100 μA Load)

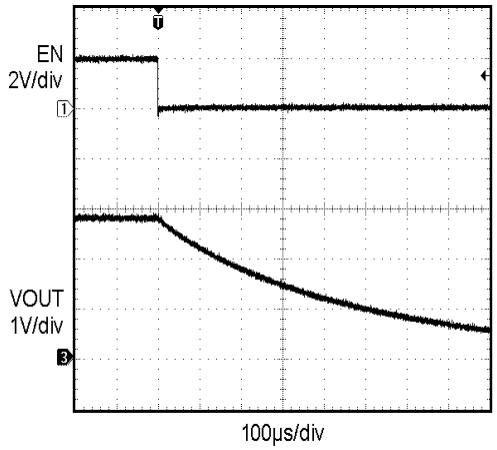


Figure 15. Enable Turn−off (100 μA Load)

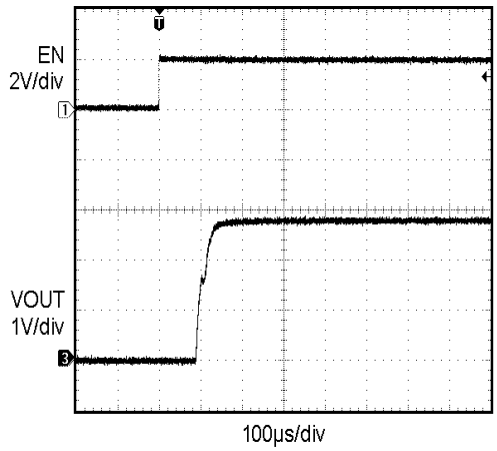


Figure 16. Enable Turn−on (500 mA Load)

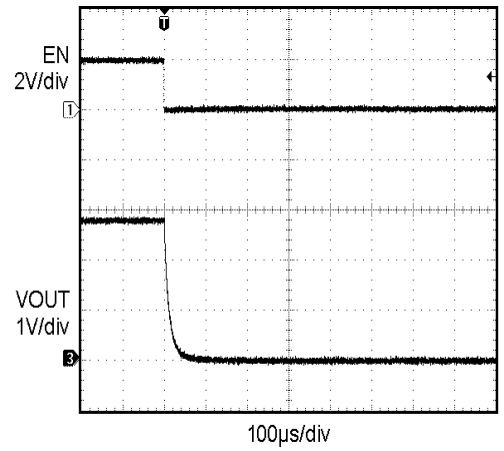


Figure 17. Enable Turn−off (500 mA Load)

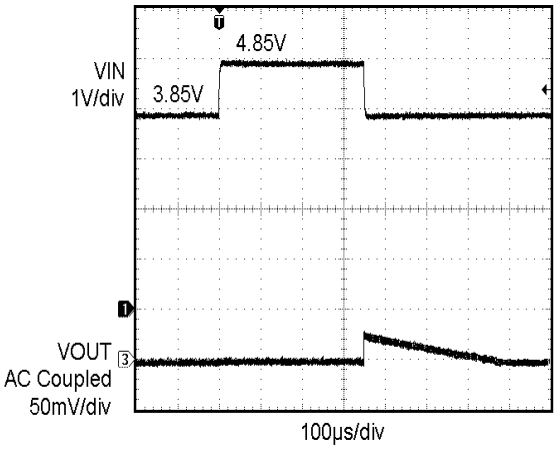


Figure 18. Line Transient Response (3.85 V to 4.85 V)

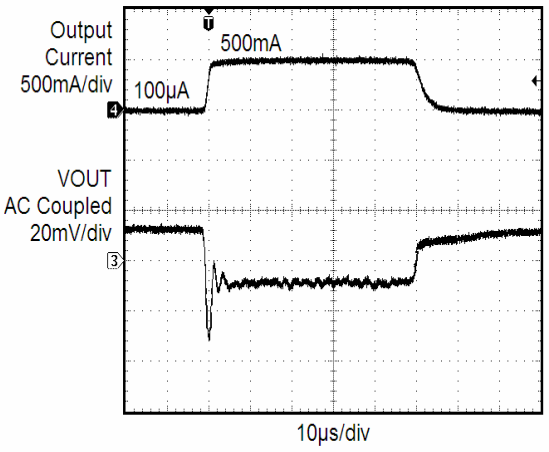


Figure 19. Load Transient Response (0.1 mA to 500 mA)

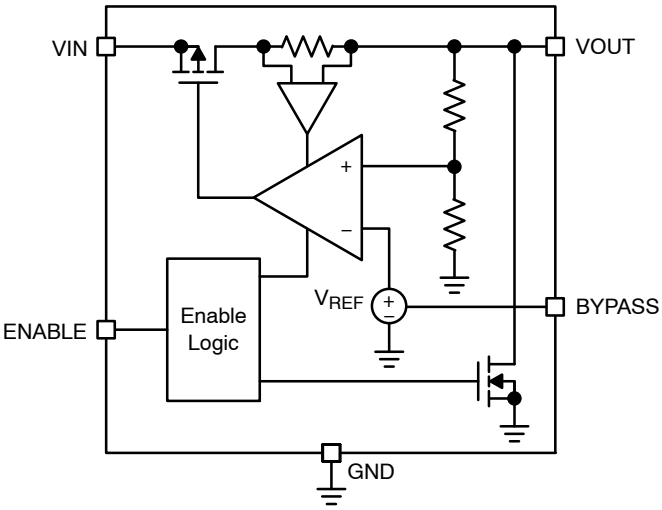


Figure 20. Block Diagram – Fixed Voltage

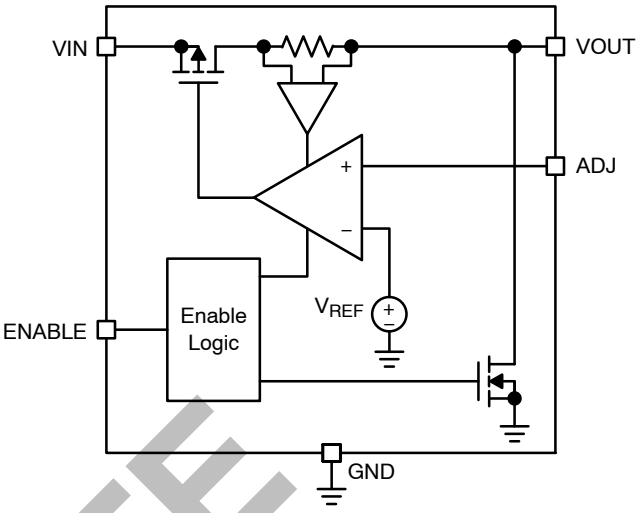
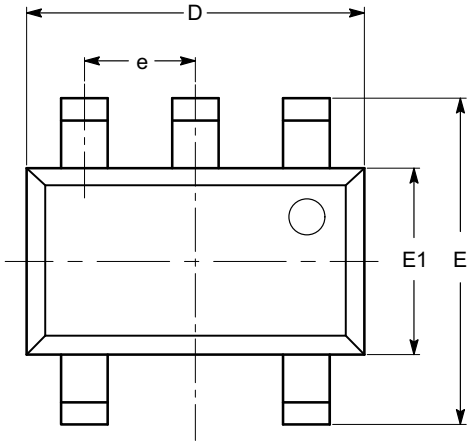


Figure 21. Block Diagram – Adjustable Voltage

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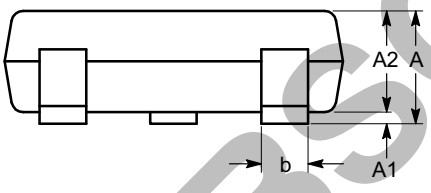
PACKAGE DIMENSIONS

TSOT−23, 5 LEAD
CASE 419AE−01
ISSUE O

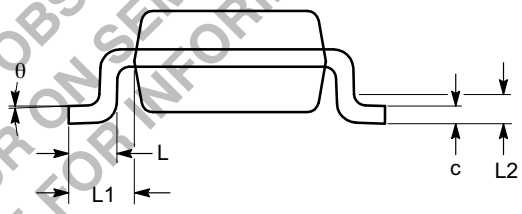


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.00
A1	0.01	0.05	0.10
A2	0.80	0.87	0.90
b	0.30		0.45
c	0.12	0.15	0.20
D	2.90 BSC		
E	2.80 BSC		
E1	1.60 BSC		
e	0.95 TYP		
L	0.30	0.40	0.50
L1	0.60 REF		
L2	0.25 BSC		
θ	0°		8°



SIDE VIEW



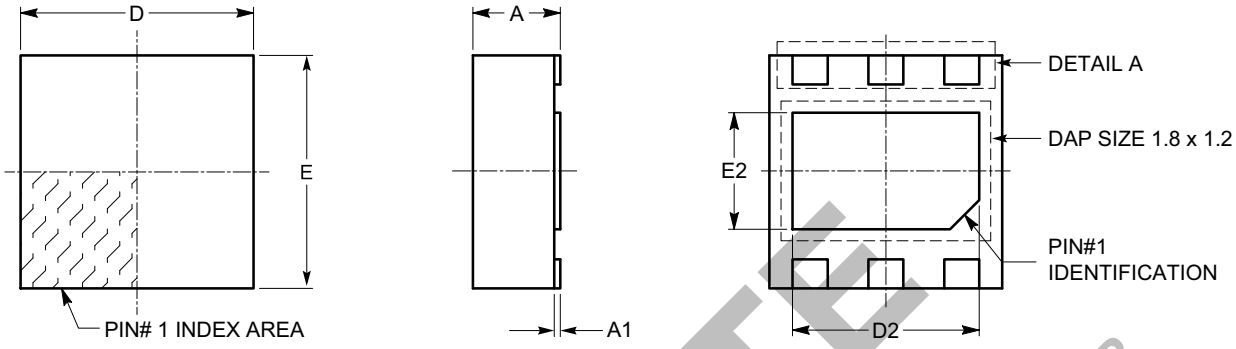
END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-193.

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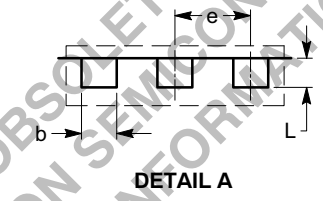
PACKAGE DIMENSIONS

TDFN6, 2x2
CASE 511AH−01
ISSUE A

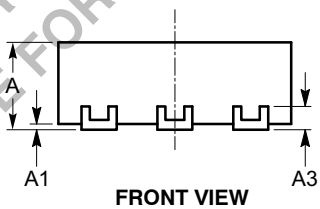


TOP VIEW **SIDE VIEW** **BOTTOM VIEW**

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.25	0.30	0.35
D	1.90	2.00	2.10
D2	1.50	1.60	1.70
E	1.90	2.00	2.10
E2	0.90	1.00	1.10
e		0.65 TYP	
L	0.15	0.25	0.35



DETAIL A



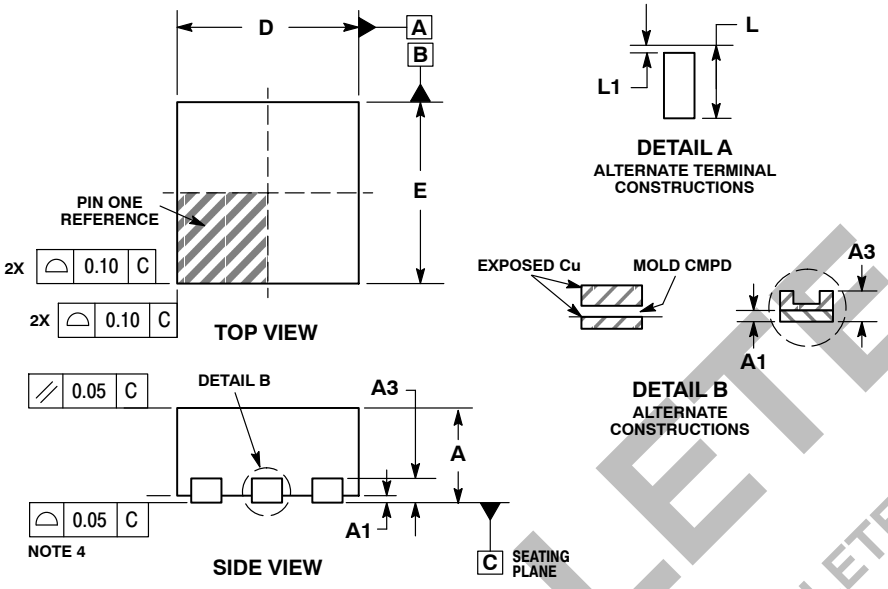
FRONT VIEW

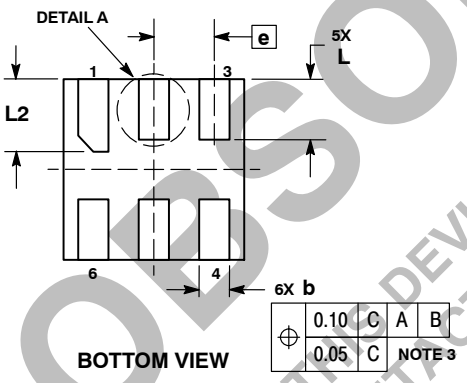
Notes:
(1) All dimensions are in millimeters.
(2) Complies with JEDEC standard MO-229.

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PACKAGE DIMENSIONS

WDFN6 1.5x1.5, 0.5P
CASE 511BJ−01
ISSUE B





NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	1.50 BSC	
E	1.50 BSC	
e	0.50 BSC	
L	0.40	0.60
L1	---	0.15
L2	0.50	0.70

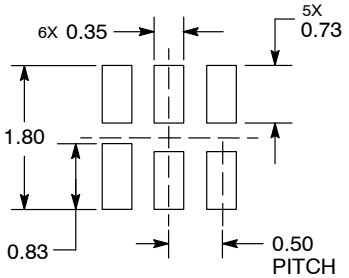
GENERIC MARKING DIAGRAM*



X = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(*Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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ORDERING INFORMATION (Notes 7 – 9)

Device Order Number	Specific Device Marking	Package Type	V_{OUT} Voltage (V)	Lead Finish	Shipping (Note 10)
CAT6219−125TDGT3	US	TSOT−23−5	1.25	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT6219−180TDGT3	RV		1.80		
CAT6219−250TDGT3	US		2.50		
CAT6219−280TDGT3	RV		2.80		
CAT6219−285TDGT3	RV		2.85		
CAT6219−300TDGT3	US		3.00		
CAT6219−330TDGT3	RV		3.30		
CAT6219ADJTD−GT3	UM		Adjustable		
CAT6219ADJVP5GT4	AF	TDFN−6 (2.0 x 2.0)	Adjustable		Tape & Reel, 4,000 Units / Reel
CAT6219180VP5GT4	AB		1.80		
CAT6219VP5330GT4	AB		3.30		
CAT6219−280MV2T3	S	WDFN−6 (1.5 x 1.5)	2.80		Tape & Reel, 3,000 Units / Reel
CAT6219−285MV2T3	T		2.85		
CAT6219−330MV2T3	U		3.30		
CAT6219ADJMV2−T3	V		Adjustable		

7. All packages are RoHS−compliant (Lead−free, Halogen−free).
8. The standard lead finish is NiPdAu pre−plated (PPF) lead frames.
9. For other voltage options, please contact your nearest ON Semiconductor Sales office.
10. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
11. For detailed information and a breakdown of device nomenclature and numbering systems, please see the ON Semiconductor Device Nomenclature document, TND310/D, available at www.onsemi.com

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