TP65H050G4YS

650V SuperGaN® FET in TO-247-4 (source tab)

Description

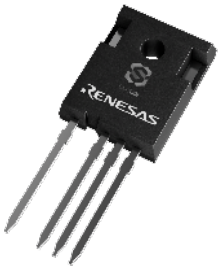
The TP65H050G4YS 650V, 50mΩ gallium nitride (GaN) FET is a normally-off device using Renesas's Gen IV platform. It combines a state-of-the-art high voltage GaN HEMT with a low voltage silicon MOSFET to offer superior reliability and performance.

The Gen IV SuperGaN® platform uses advanced epi and patented design technologies to simplify manufacturability while improving efficiency over silicon via lower gate charge, output capacitance, crossover loss, and reverse recovery charge.

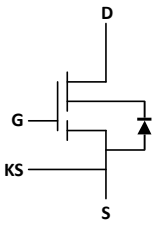
Benefits

- Superior normally off architecture with D-mode GaN HEMT
- Compatible with standard silicon drivers
- Enhanced noise immunity with a 4V threshold voltage with no negative gate drive required
- Enables high-efficiency, high power density, and reliable power conversion
- Facilitates cost-effective GaN adoption reducing system size, weight, and costs

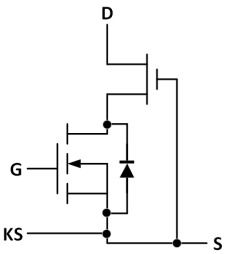
Product and Schematic Diagrams



TP65H050G4YS TO-247-4



Cascode Schematic Symbol



Cascode Device Structure

Features

- Ultra-fast switching Gen IV GaN technology
- JEDEC-qualified GaN technology
- Dynamic $R_{DS(on)eff}$ production tested
- Reduced crossover loss
- Negligible Qrr
- RoHS compliant and Halogen-free packaging

Applications

- AI datacenter and telecom power supplies
- E-mobility charging
- PV inverter
- UPS
- BESS

Specifications

V_{DS} (V)	650
$V_{DSS(TR)}$(V) maximum	800
$R_{DS(on)}$ (mΩ) maximum [1]	60
Q_{OSS} (nC) typical	112
Q_G (nC) typical	15.3

1. Dynamic $R_{DS(on)}$ (see Figure 17 and Figure 18)

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Contents

1. Pin Information 3
1.1 Pin Assignments 3
1.2 Pin Descriptions 3
2. Specifications 4
2.1 Absolute Maximum Ratings 4
2.2 Thermal Specifications 4
2.3 Electrical Specifications – Forward Device 5
2.4 Electrical Specifications – Reverse Device 6
3. Typical Performance Graphs 7
4. Test Circuits and Waveforms 10
5. Package Outline Drawings 11
6. Related Information 12
7. Ordering Information 12
8. Revision History 12

Figures

Figure 1. Pin Assignments 3
Figure 2. Typical Output Characteristics, T_J = 25°C Parameter: V_{GS} 7
Figure 3. Typical Output Characteristics, T_J = 150°C Parameter: V_{GS} 7
Figure 4. Typical Transfer Characteristics V_{DS} = 20V, Parameter: T_J 7
Figure 5. Normalized On-resistance I_D = 22A, V_{GS} = 10V 7
Figure 6. Typical Capacitance V_{GS} = 0V, f = 500kHz 8
Figure 7. Typical C_{OSS} Stored Energy 8
Figure 8. Typical Q_{OSS} 8
Figure 9. Typical Gate Charge 8
Figure 10. Power Dissipation 9
Figure 11. Current Derating 9
Figure 12. Forward Characteristics of Rev. Diode 9
Figure 13. Transient Thermal Resistance 9
Figure 14. Safe Operating Area T_C = 25°C 10
Figure 15. Switching Time Test Circuit 10
Figure 16. Switching Time Waveform 10
Figure 17. Dynamic $R_{DS(on)eff}$ Test Circuit 10
Figure 18. Dynamic $R_{DS(on)eff}$ Waveform 10
Figure 19. TO-247-4 Package Outline Drawing 11

1. Pin Information

1.1 Pin Assignments

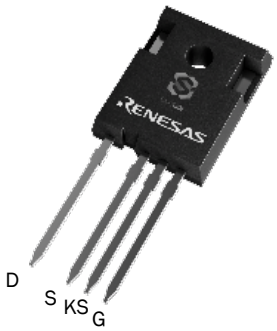


Figure 1. Pin Assignments

1.2 Pin Descriptions

Pin Name	Description
D	Drain.
S	Source.
KS	Kelvin source.
G	Gate.

2. Specifications

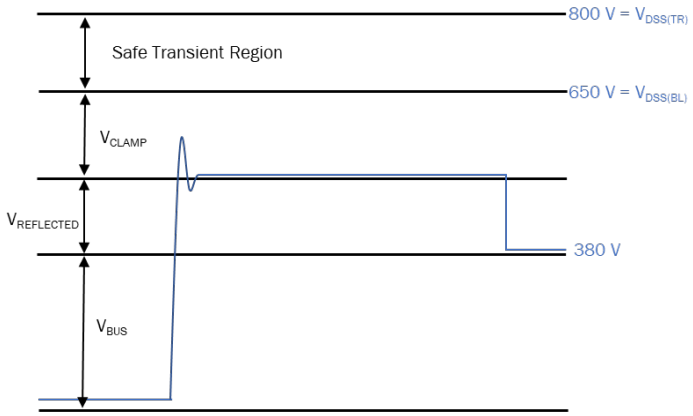
2.1 Absolute Maximum Ratings

T_c = 25°C unless otherwise stated.

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Symbol	Parameter	Limit Value	Unit
V_{DSS}	Drain to source voltage (T_J = -55°C to 150°C)	650	V
$V_{DSS(TR)}$	Transient drain to source voltage [1]	800	
V_{GSS}	Gate to source voltage	+20	
P_D	Maximum power dissipation at T_C = 25°C	132	W
I_D	Continuous drain current at T_C = 25°C	35	A
	Continuous drain current at T_C = 100°C	22	A
I_{DM}	Pulsed drain current (pulse width: 10µs)	150	A
T_J	Junction operating temperature	-55 to +150	°C
T_S	Storage temperature	-55 to +150	°C
T_{SOLD}	Reflow soldering temperature [2]	260	°C
-	Mounting torque	70	N cm

1. In off-state, spike duty cycle D < 0.01, spike duration < 30µs, non-repetitive.
2. For 10 sec., 1.6mm from the case.



Primary Switch Voltage Stress (264 V AC)

2.2 Thermal Specifications

Symbol	Condition	Typical Value	Unit
$R_{\Theta JC}$	Junction-to-case	0.95	°C/W
$R_{\Theta JA}$	Junction-to-ambient	40	

2.3 Electrical Specifications – Forward Device

T_J = 25°C unless otherwise stated.

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
$V_{DSS(BL)}$	Maximum drain-source voltage	V_{GS} = 0V	650	-	-	V
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 0.7mA	3.3	4	4.8	V
$\Delta V_{GS(th)}/T_J$	Gate threshold voltage temperature coefficient		-	-6.2	-	mV/°C
$R_{DS(on)eff}$	Drain-source on-resistance [1]	V_{GS} = 10V, I_D = 22A, T_J = 25°C	-	50	60	mΩ
		V_{GS} = 10V, I_D = 22A, T_J = 150°C	-	105	-	
I_{DSS}	Drain-to-source leakage current	V_{DS} = 650V, V_{GS} = 0V, T_J = 25°C	-	4	40	μA
		V_{DS} = 650V, V_{GS} = 0V, T_J = 150°C	-	15	-	
I_{GSS}	Gate-to-source forward leakage current	V_{GS} = 20V	-	-	100	nA
	Gate-to-source reverse leakage current	V_{GS} = -20V	-	-	-100	
C_{ISS}	Input capacitance	V_{GS} = 0V, V_{DS} = 400V, *f* = 1MHz	-	1000	-	pF
C_{OSS}	Output capacitance		-	110	-	
C_{RSS}	Reverse transfer capacitance		-	2.7	-	
$C_{O(er)}$	Output capacitance, energy related [2]	V_{GS} = 0V, V_{DS} = 0V to 400V	-	164	-	pF
$C_{O(tr)}$	Output capacitance, time related [3]		-	280	-	
Q_G	Total gate charge	V_{DS} = 400V, V_{GS} = 0V to 10V, I_D = 22A	-	15.3	-	nC
Q_{GS}	Gate-source charge		-	6	-	
Q_{GD}	Gate-drain charge		-	5	-	
Q_{OSS}	Output charge	V_{GS} = 0V, V_{DS} = 0V to 400V	-	112	-	nC
$t_{D(on)}$	Turn-on delay	V_{DS} = 400V, V_{GS} = 0V to 10V, I_D = 22A, $R_{G(ON)}$ = 47Ω, $R_{G(OFF)}$ = 39Ω, Z_{FB} = 240Ω at 100MHz (see Figure 15)	-	40	-	ns
t_R	Rise time		-	5	-	
$t_{D(off)}$	Turn-off delay		-	40	-	
t_F	Fall time		-	8	-	

1. Dynamic $R_{DS(on)}$ 100% tested; see Figure 17 and Figure 18 for conditions.
2. Equivalent capacitance to give same stored energy from 0V to 400V.
3. Equivalent capacitance to give same charging time from 0V to 400V.

2.4 Electrical Specifications – Reverse Device

T_J = 25°C unless otherwise stated.

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
I_S	Reverse current	V_{GS} = 0V, T_C = 100°C, ≤ 25% duty cycle	-	-	22	A
V_{SD}	Reverse voltage [1]	V_{GS} = 0V, I_S = 22A	-	2.2	-	V
		V_{GS} = 0V, I_S = 11A	-	1.6	-	

1. Includes dynamic $R_{DS(on)}$ effect.

Note: Reverse recovery charge is negligible, enabled by the LV Si FET technology.

3. Typical Performance Graphs

T_C = 25°C unless otherwise stated.

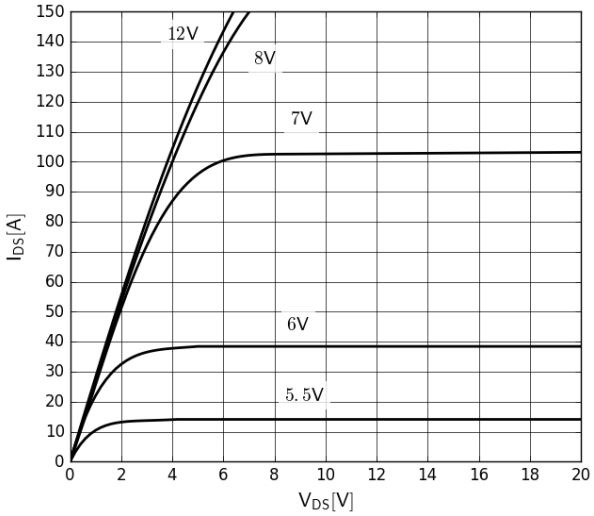


Figure 2. Typical Output Characteristics, T_J = 25°C

Parameter: V_{GS}

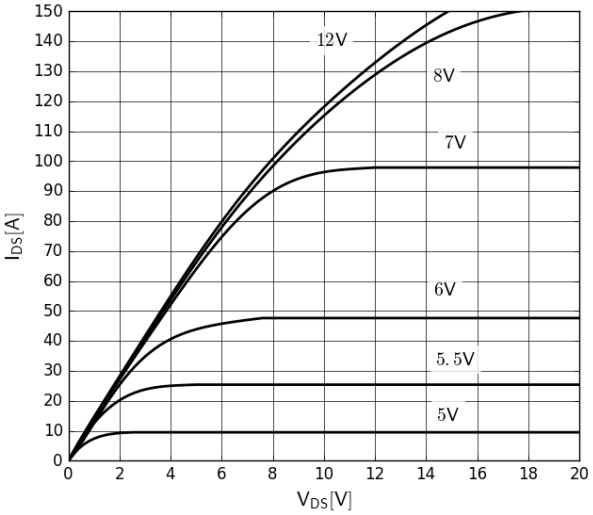


Figure 3. Typical Output Characteristics, T_J = 150°C

Parameter: V_{GS}

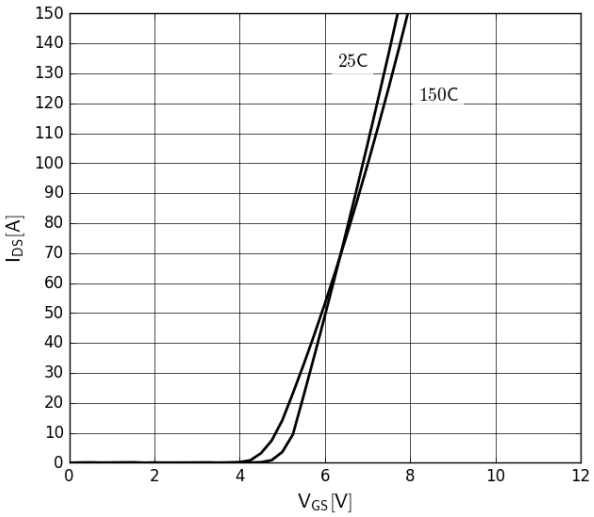


Figure 4. Typical Transfer Characteristics

V_{DS} = 20V, Parameter: T_J

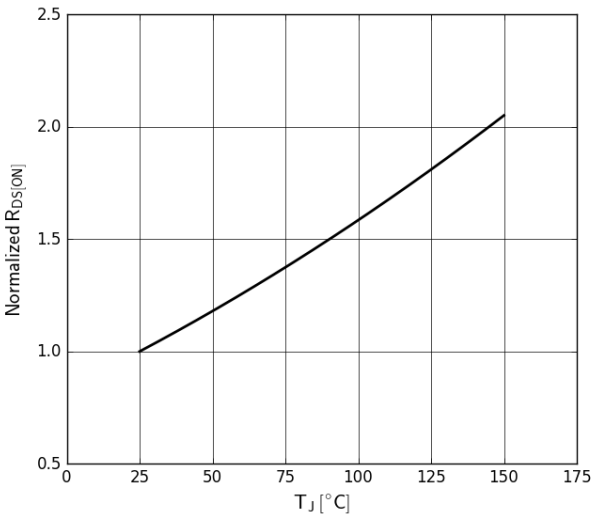


Figure 5. Normalized On-resistance

I_D = 22A, V_{GS} = 10V

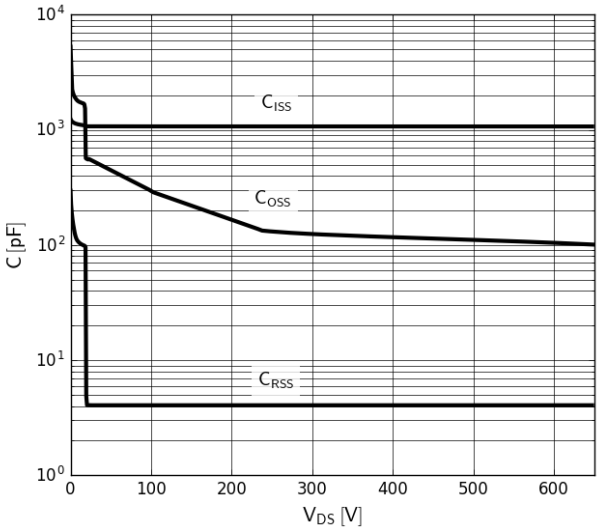


Figure 6. Typical Capacitance

V_{GS} = 0V, f = 500kHz

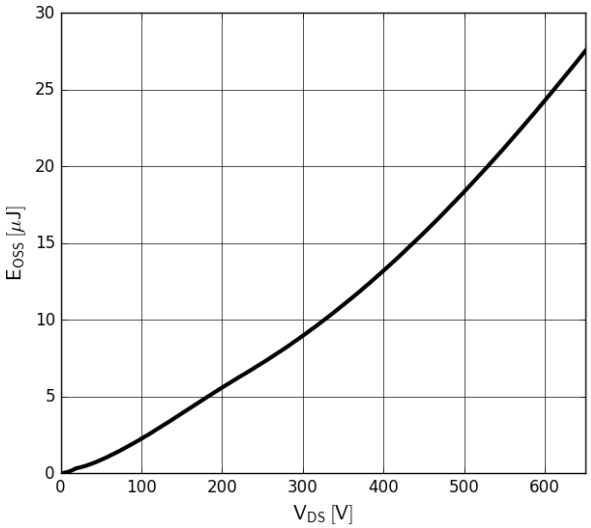


Figure 7. Typical C_{OSS} Stored Energy

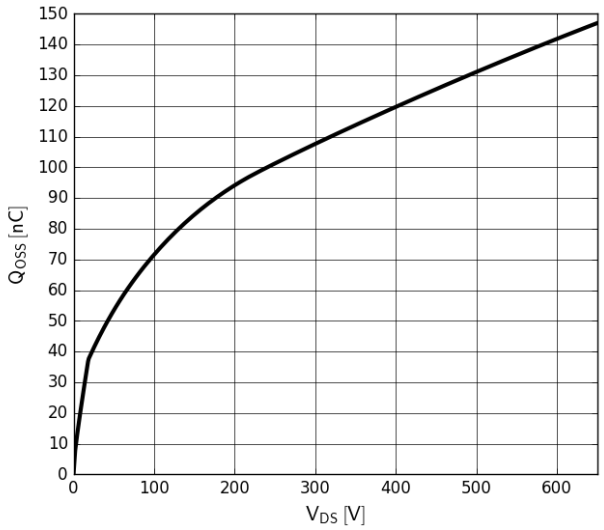


Figure 8. Typical Q_{OSS}

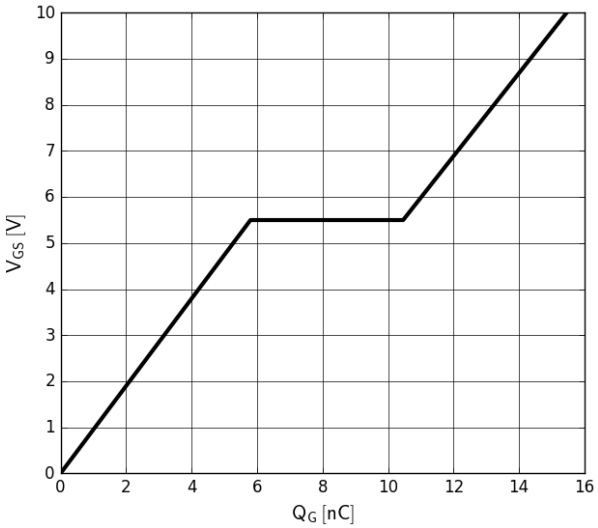


Figure 9. Typical Gate Charge

I_{DS} = 22A, V_{DS} = 400V

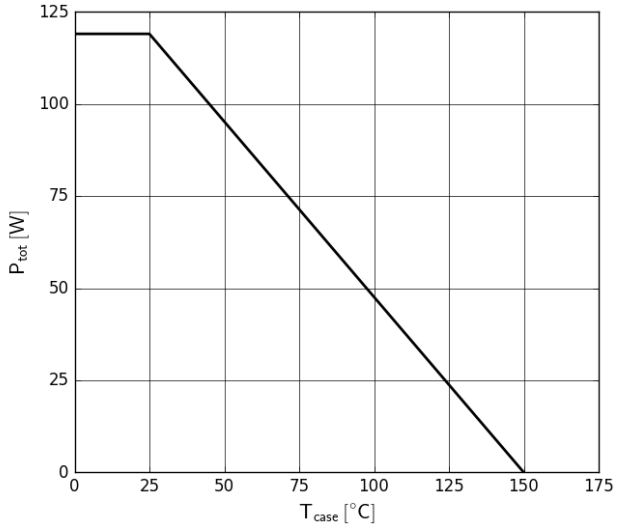


Figure 10. Power Dissipation

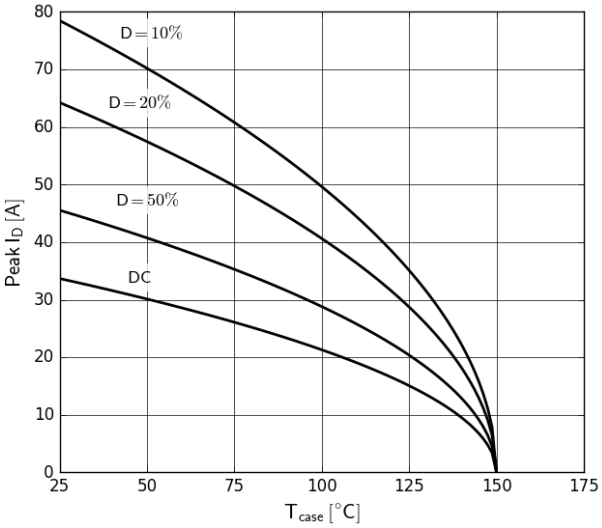


Figure 11. Current Derating

Pulse width ≤ 10µs, V_{GS} ≥ 10V

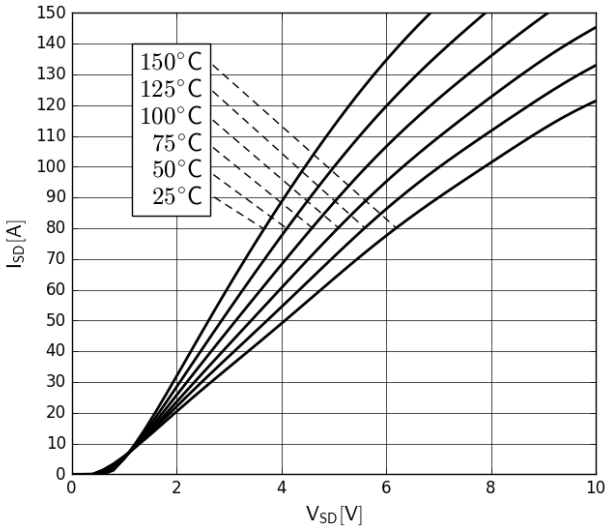


Figure 12. Forward Characteristics of Rev. Diode

$I_S = f(V_{SD})$, Parameter: T_J

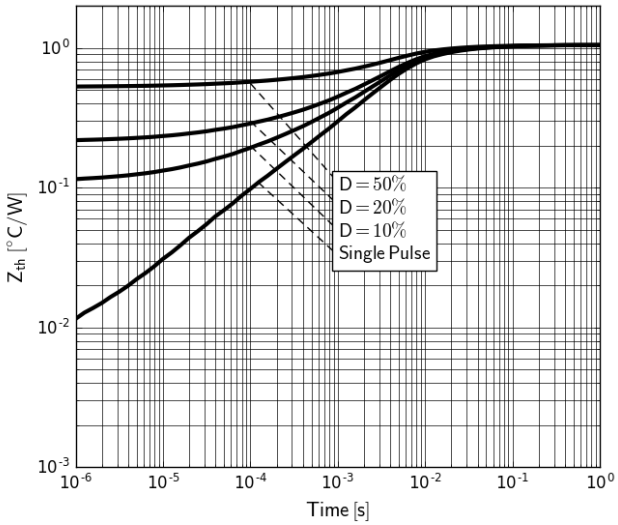


Figure 13. Transient Thermal Resistance

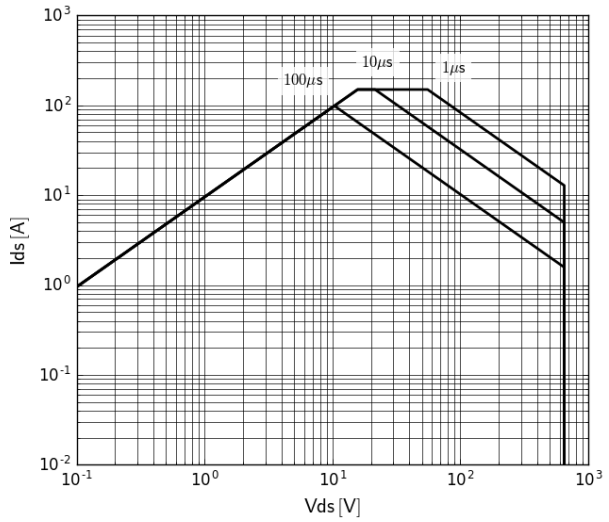


Figure 14. Safe Operating Area T_C = 25°C

4. Test Circuits and Waveforms

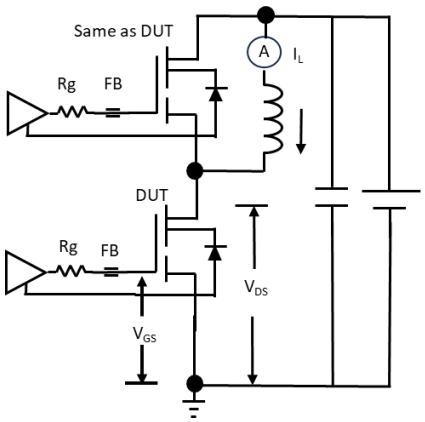


Figure 15. Switching Time Test Circuit

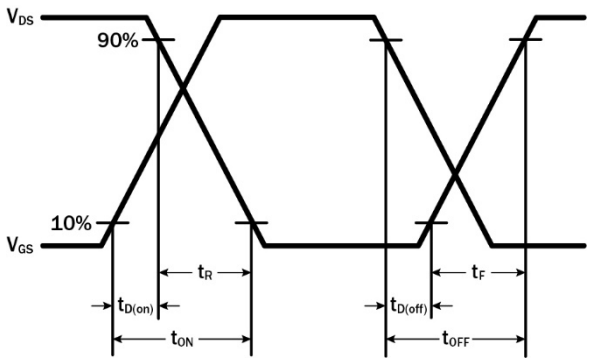


Figure 16. Switching Time Waveform

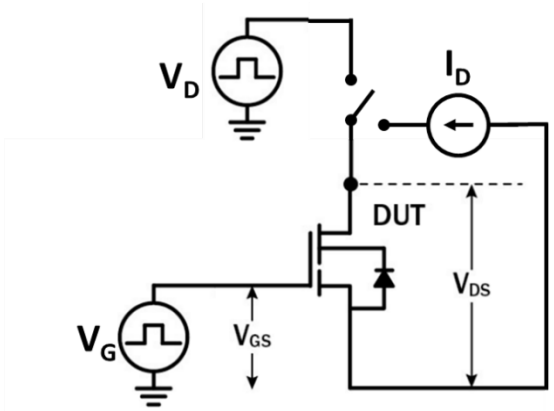


Figure 17. Dynamic $R_{DS(on)eff}$ Test Circuit

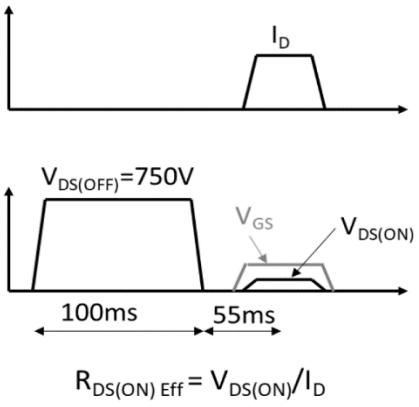
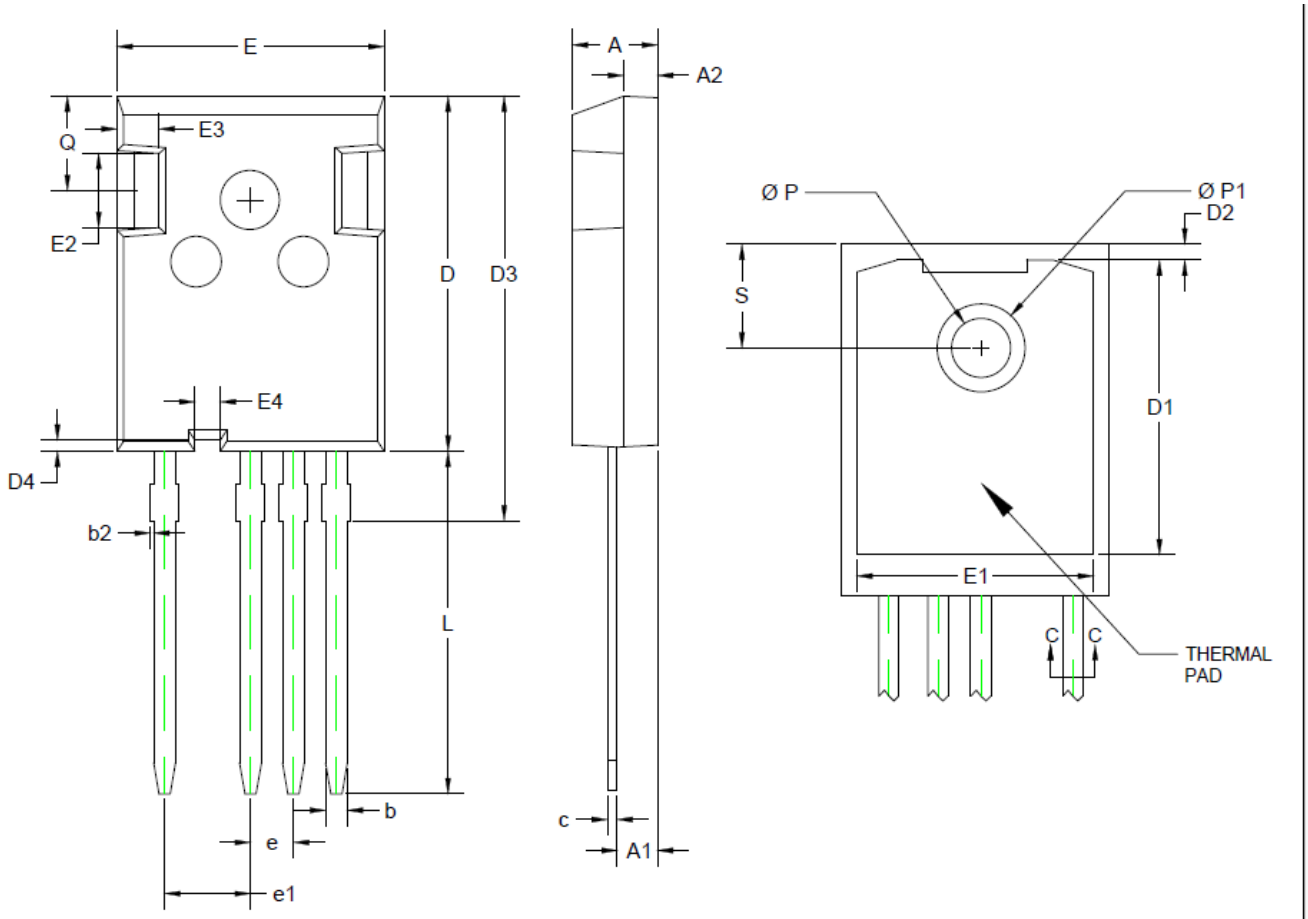
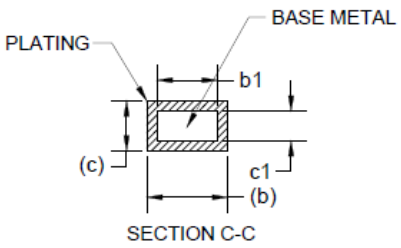


Figure 18. Dynamic $R_{DS(on)eff}$ Waveform

5. Package Outline Drawings





SECTION C-C

NOTES:

1. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 MM (0.005") PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREME OF THE PLASTIC BODY.

2. THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS D1 & E1.

3. OUTLINE CONFORMS TO JEDEC TO-247AD.

SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.90	5.00	5.10	0.192	0.196	0.201
A1	2.31	2.41	2.51	0.090	0.094	0.099
A2	1.90	2.00	2.10	0.074	0.078	0.083
b	1.16	-	1.29	0.045	-	0.051
b1	1.15	1.20	1.25	0.045	0.047	0.050
b2	0	-	0.20	0	-	0.008
c	0.59	-	0.66	0.023	-	0.027
c1	0.58	0.60	0.62	0.022	0.023	0.025
D	20.90	21.00	21.10	0.822	0.826	0.831
D1	16.25	16.55	16.85	0.639	0.651	0.664
D2	1.05	1.20	1.35	0.041	0.047	0.054
D3	24.97	25.12	25.27	0.983	0.988	0.995
D4	0.55	0.65	0.75	0.021	0.025	0.030
E	15.70	15.80	15.90	0.618	0.622	0.627
E1	13.10	13.30	13.50	0.515	0.523	0.532
E2	4.90	5.00	5.10	0.192	0.196	0.201
E3	2.40	2.50	2.60	0.094	0.098	0.103
E4	1.40	1.50	1.60	0.055	0.059	0.064
e	2.44	2.54	2.64	0.096	0.100	0.105
e1	4.98	5.08	5.18	0.196	0.200	0.205
L	19.80	19.92	20.10	0.779	0.784	0.792
P	3.50	3.60	3.70	0.137	0.141	0.146
P1	-	-	7.40	-	-	0.292
Q	5.60	-	6.00	0.220	-	0.237
S	6.15 BSC			0.242 BSC		

TO-247 4L TP65HXXXG4YS

transphorm

Figure 19. TO-247-4 Package Outline Drawing

6. Related Information

All technical documents for Renesas GaN Power devices are accessible from the GaN Power Solutions page.

7. Ordering Information

Part Number	Package Description	Package Configuration
TP65H050G4YS	TO-247-4	Source tab

8. Revision History

Revision	Date	Description
2.01	Dec 9, 2025	Corrected Pin Assignments labeling.
2.00	Nov 26, 2025	Updated the document's formatting; no technical changes were completed.
1.00	Dec 14, 2023	Initial release.

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Entegreden kapasitöre tüm elektronik komponent kategorileri.

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